3A, 18V, 340KHz Synchronous Rectified Step-Down Converter

FEATURES

- 3A Continuous Output Current
- Wide 4.75V to 18V Operating Input Range
- Integrated 85mΩ Power MOSFET Switches
- Output Adjustable from 0.925V to 15V
- Up to 95% Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 340KHz Frequency
- Cycle-by-Cycle Over Current Protection
- Input Under Voltage Lockout
- Thermally Enhanced 8-Pin SOP Package

ESOP-8

ORDERING INFORMATION

DEVICE	Package Type	MARKING	Packing	Packing Qty
HG1484ME/TR	ESOP-8	HG1484	REEL	2500pcs/Reel

DESCRIPTION

The HG1484 is a monolithic synchronous buck regulator. The device integrates top and bottom 85mΩ MOSFETS that provide 3A of continuous load current over a wide operating input voltage of 4.75V to 18V. Current mode control provides fast transient response and cycle-by-cycle current limit.
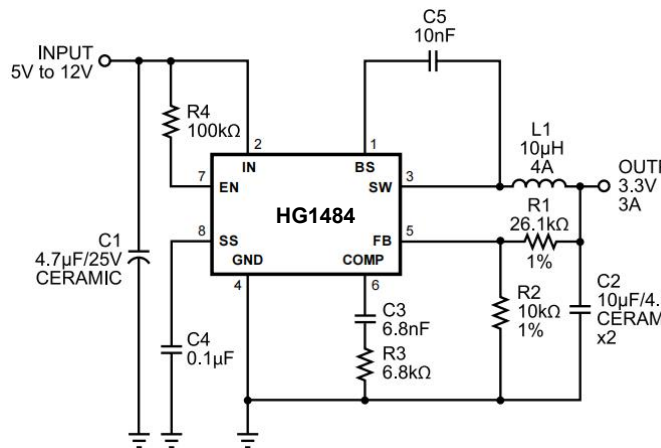
An adjustable soft-start prevents inrush current at turn-on and in shutdown mode, the supply current drops below 1μA.

The HG1484 is PIN compatible to the MP1484 and MP1484 2A/18V/Synchronous Step-Down Converter.
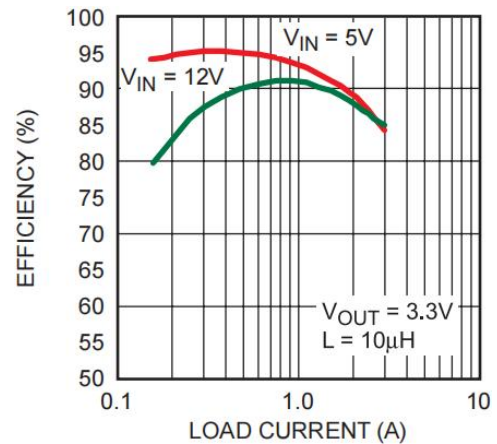
APPLICATIONS

- FPGA, ASIC, DSP Power Supplies
- LCD TV
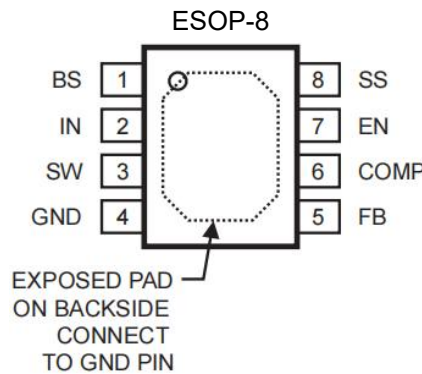- Green Electronics/Appliances
- Notebook Computers

TYPICAL APPLICATION

Efficiency vs Load Current

PACKAGE REFERENCE

ESOP-8

EXPOSED PAD
ON BACKSIDE
CONNECT
TO GND PIN

PIN FUNCTIONS

Pin #	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01µF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches.Drive IN with a 4.75V to 18V power source. See *Input Capacitor*.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connectthe output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground (Connect the exposed pad to Pin 4).
5	FB	Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage. The feedback threshold is 0.925V. See*Setting the Output Voltage*.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND. In some cases, an additional capacitor from COMP toGND is required. See *Compensation Components*.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off. Attach to IN with a 100kΩ pull up resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GNDto set the soft-start period. A 0.1µF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, leave SS unconnected.

ABSOLUTE MAXIMUM RATINGS [1]

Condition	Min	Max	Unit
Supply Voltage V_{IN}	-0.3	+24	V
Switch Voltage V_{SW}	-1	V_{IN}+0.3	V
Boost Voltage V_{BS}	$V_{SW} - 0.3$	$V_{SW} + 6$	V
All Other Pins	-0.3	+6	V
Junction Temperature	-	150	℃
Lead Temperature，10s	-	245	℃
Storage Temperature	-65	+150	℃

RECOMMENDED OPERATING CONDITIONS [2]

Condition	Min	Max	Unit
Input Voltage V_{IN}	4.75	18	V
Output Voltage V_{OUT}	0.925	15	V
Ambient Operating Temp	-20	+85	℃

THERMAL RESISTANCE [3]

Condition	θ_{JA}	θ_{JC}	Unit
ESOP8 (Exposed Pad)	50	10	℃/W

Notes:

1) Exceeding these ratings may damage the device.

2) The device is not guaranteed to function outside of its operating conditions.

3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Shutdown Supply Current		V_{EN} = 0V		0.3	3.0	µA
Supply Current		V_{EN} = 2.0V, V_{FB} = 1.0V		1.3	1.5	mA
Feedback Voltage	V_{FB}	4.75V V_{IN} 18V	0.900	0.925	0.950	V
Feedback Overvoltage Threshold				1.1		V
Error Amplifier Voltage Gain [4]	A_{EA}			400		V/V
Error Amplifier Transconductance	G_{EA}	I_C = 10µA		820		µA/V
High-Side/Low-Side Switch On-Resistance [4]				85		mΩ
High-Side Switch Leakage Current		V_{EN} = 0V, V_{SW} = 0V		0	10	µA
Upper Switch Current Limit		Minimum Duty Cycle	3.8	5.3		A
Lower Switch Current Limit		From Drain to Source		0.9		A
COMP to Current Sense Transconductance	G_{CS}			5.2		A/V
Oscillation Frequency	F_{osc1}		300	340	380	KHz
Short Circuit Oscillation Frequency	F_{osc2}	V_{FB} = 0V		110		KHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 1.0V		90		%
Minimum On Time [4]	T_{ON}			220		ns
EN Shutdown Threshold Voltage		V_{EN} Rising	1.1	1.5	2.0	V
EN Shutdown Threshold Voltage Hysterisis				220		mV
EN Lockout Threshold Voltage			2.2	2.5	2.7	V
EN Lockout Hysterisis				210		mV
Input Under Voltage LockoutThreshold		V_{IN} Rising	3.80	4.05	4.40	V
Input Under Voltage LockoutThreshold Hysteresis				210		mV
Soft-Start Current		V_{SS} = 0V		6		µA
Soft-Start Period		C_{SS} = 0.1µF		15		ms
Thermal Shutdown [4]				160		°C

Note:

4) Guaranteed by design, not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

C1 = 4.7µF, C2 = 2 x 10µF, L= 10µH, C_{SS}= 0.1µF, T_A = +25°C, unless otherwise noted.

Steady State Test Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A
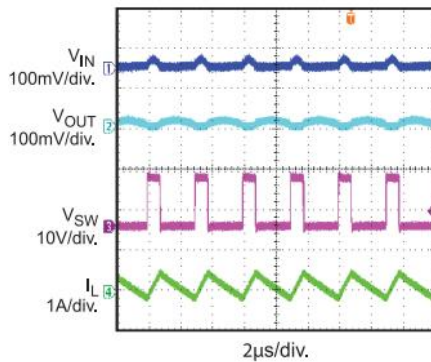
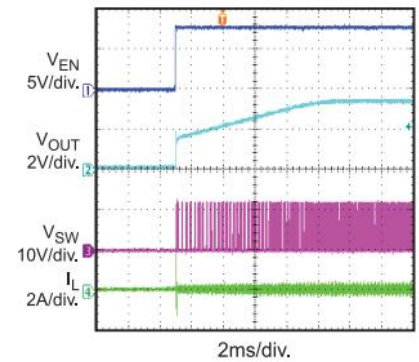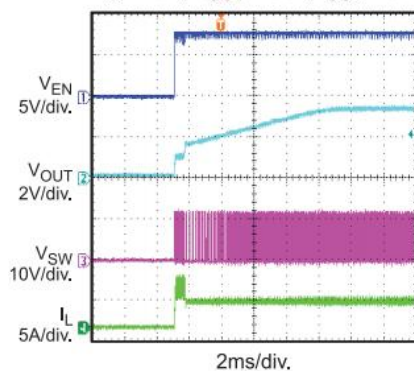**Steady State Test Waveforms**

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A
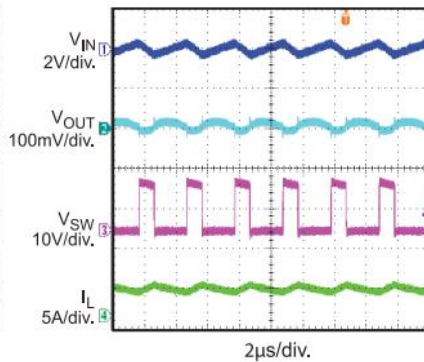
Startup through Enable Waveforms
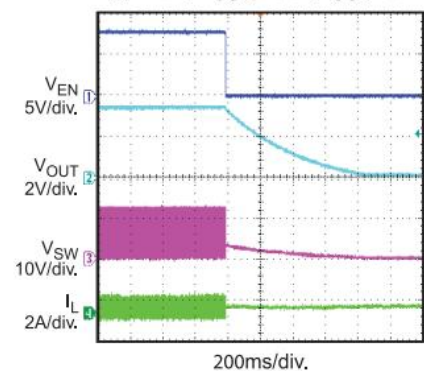
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 0A

Startup Through Enable Waveforms
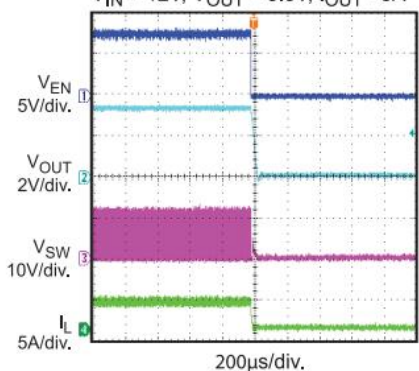
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 3A

Shutdown Through Enable Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} =0A

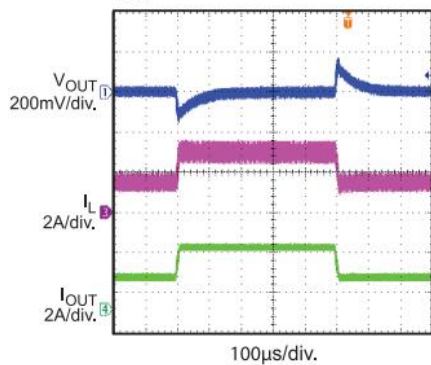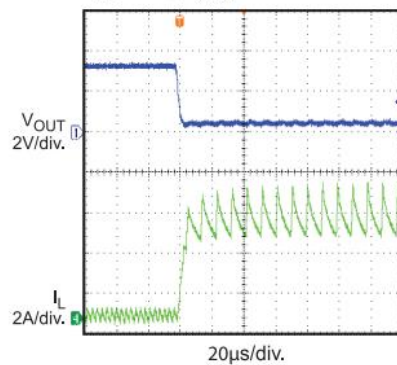**Shutdown Through Enable Waveforms**

V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} =3A

Load Transient Test Waveforms
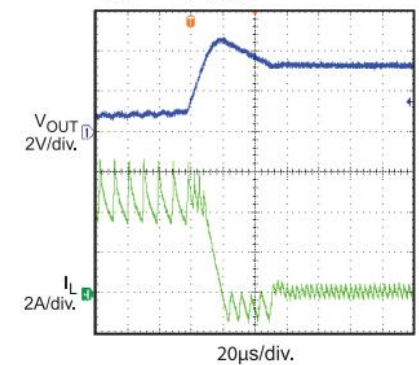
V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 1.5A to 3A

Short Circuit Test Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V

Short Circuit Recovery Waveforms

V_{IN} = 12V, V_{OUT} = 3.3V

OPERATION

FUNCTIONAL DESCRIPTION

The HG1484 regulates input voltages from 4.75V to 18V down to an output voltage as low as 0.925V, and supplies up to 3A of load current.

The HG1484 uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal transconductance error amplifier. The voltage at the COMP pin is compared to the switch current (measured internally) to control the output voltage. The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the FB pin voltage exceeds 20% of the nominal regulation value of 0.925V, the over voltage comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.
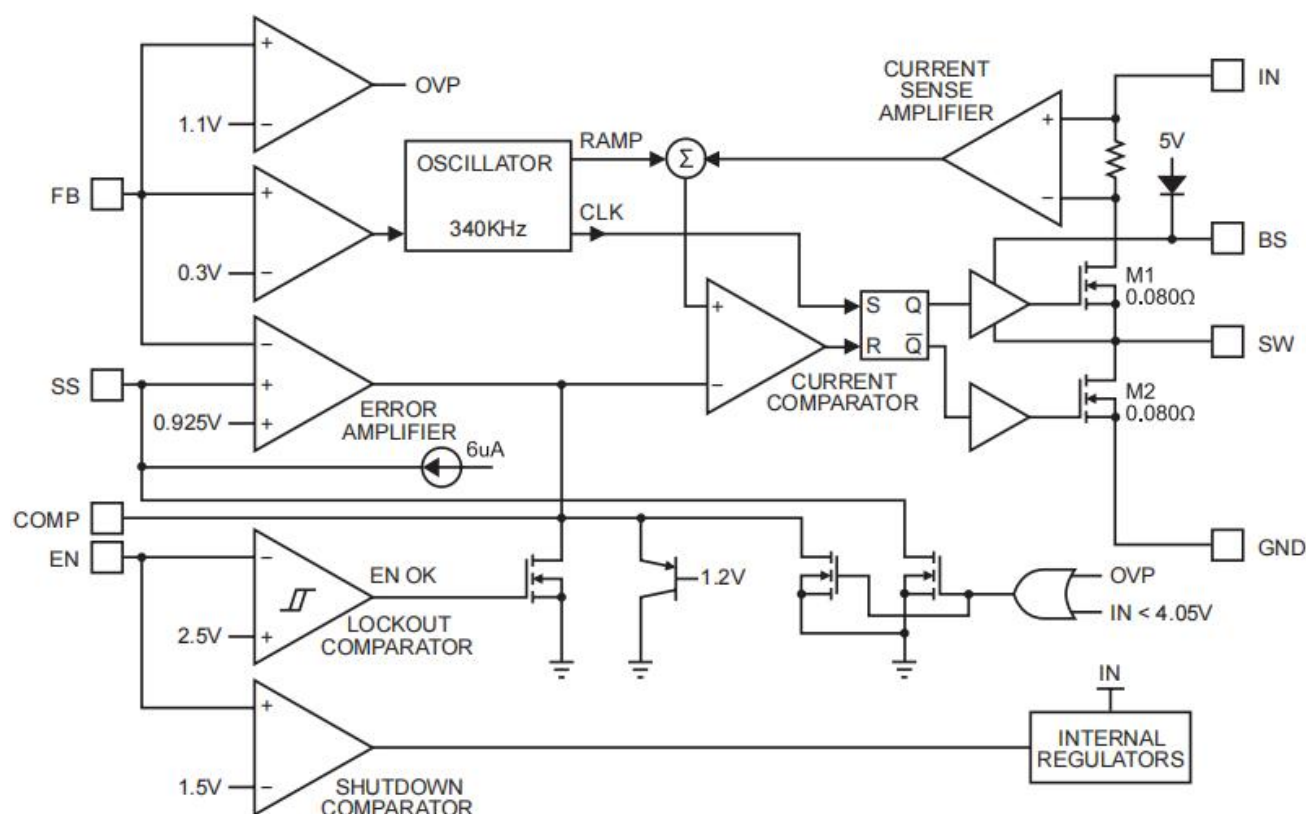

Figure 1—Functional Block Diagram

APPLICATIONS INFORMATION COMPONENT SELECTION

Setting the Output Voltage

The output voltage is set using a resistive voltage divider connected from the output voltage to FB. The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R2}{R1 + R2}$$

Thus the output voltage is:

$$V_{OUT} = 0.925 \times \frac{R1 + R2}{R2}$$

R2 can be as high as 100kΩ, but a typical value is 10kΩ. Using the typical value for R2, R1 is determined by:

$$R1 = 10.81 \times (V_{OUT} - 0.925)(K\Omega)$$

For example, for a 3.3V output voltage, R2 is 10kΩ, and R1 is 26.1kΩ. Table 1 lists recommended resistance values of R1 and R2 for standard output voltages.

Table 1—Recommended Resistance Values

VOUT	R1	R2
1.8V	9.53kΩ	10kΩ
2.5V	16.9kΩ	10kΩ
3.3V	26.1kΩ	10kΩ
5V	44.2kΩ	10kΩ
12V	121kΩ	10kΩ

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will in turn result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining inductance is to allow the peak-to- peak ripple current to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit.

The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where ILOAD is the load current.

The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Table 2—Diode Selection Guide

Part Number	Voltage/CurrentRating	Vendor
B130	30V, 1A	Diodes, Inc.
SK13	30V, 1A	Diodes, Inc.
MBRS130	30V, 1A	InternationalRectifier

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{C1} = I_{LOAD}/2$. For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1µF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C1 \times f_s} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C1 is the input capacitance value.

OUTPUT CAPACITOR

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Under typical application conditions,a minimum ceramic capacitor value of 20 µF is recommended on the output. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times CS}\right)$$

Where C2 is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance which is the main cause for the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The HG1484 can be optimized for a wide range of capacitance and ESR values.

COMPENSATION COMPONENTS

HG1484 employs current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the COMP pin. COMP is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to govern the characteristics of the control system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}}$$

Where V_{FB} is the feedback voltage (0.925V), A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value.

The system has two poles of importance. One is due to the compensation capacitor (C3) and the output resistor of the error amplifier, and the other is due to the output capacitor and the load resistor. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2\pi \times C2 \times R_{LOAD}}$$

Where GEA is the error amplifier transconductance.

The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2\pi \times C2 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good standard is to set the crossover frequency below one-tenth of the switching frequency.

To optimize the compensation components, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency.

Determine R3 by the following equation:

$$R3 = \frac{2\pi \times C2 \times f_c}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} < \frac{2\pi \times C2 \times 0.1 \times f_s}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where fC is the desired crossover frequency which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero (fZ1) below one-forth of the crossover frequency provides sufficient phase margin.

Determine C3 by the following equation:

$$C3 > \frac{4}{2\pi \times R3 \times f_c}$$

Where R3 is the compensation resistor.

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

$$\frac{1}{2\pi \times C2 \times R_{ESR}} < \frac{f_s}{2}$$

If this is the case, then add the second compensation capacitor (C6) to set the pole fP3 at the location of the ESR zero. Determine C6 by the equation:

$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

EXTERNAL BOOTSTRAP DIODE

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BS diode are:

- VOUT is 5V or 3.3V:and

- Duty cycle is high:$D = \frac{V_{OUT}}{V_{IN}} > 65\%$

In these cases, an external BS diode is recommended from the output of the voltage regulator to BS pin, as shown in Fig.2
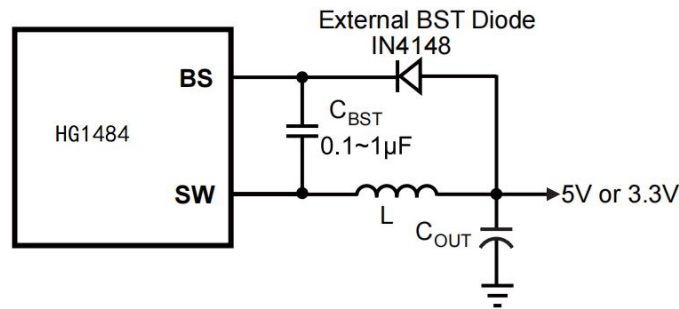

Figure 2—Add Optional External Bootstrap Diode to Enhance Efficiency

The recommended external BS diode is IN4148, and the BS cap is 0.1~1μF.
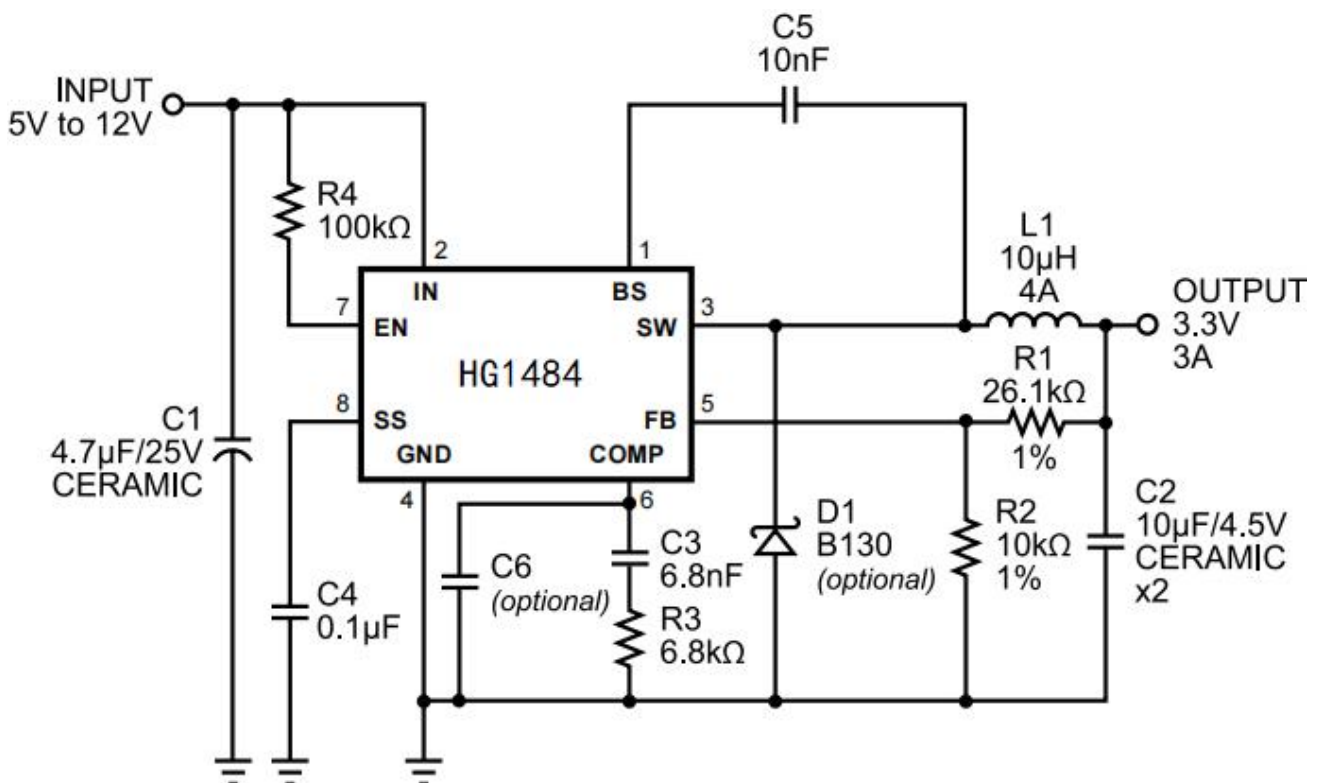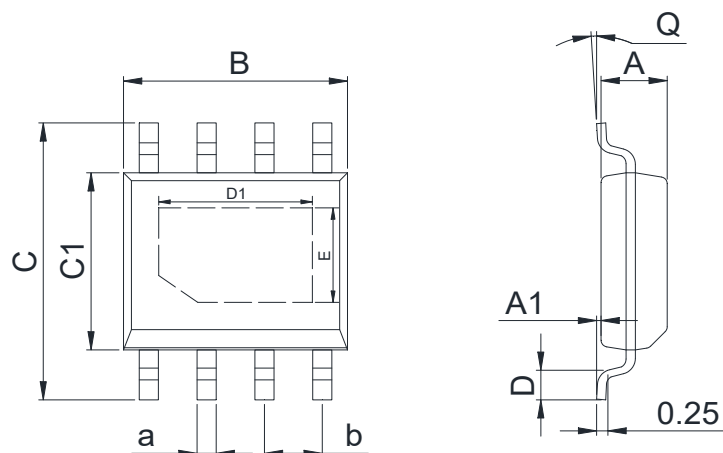
TYPICAL APPLICATION CIRCUIT

Figure 3—HG1484 with 3.3V Output, 2X10μF Ceramic Output Capacitor

PHYSICAL DIMENSIONS

ESOP-8

Dimensions In Millimeters(ESOP-8)										
Symbol:	A	A1	B	C	C1	D	D1	E	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	3.20	2.31	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	3.40	2.51	8°	0.45	

REVISION HISTORY

DATE	REVISION	PAGE
2016-3-5	New	1-14
2023-7-24	Update encapsulation type、Update Lead Temperature	1、3

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