4Gb SLC NAND FLASH
HYN4G08UHTCC1

Feature Summary

■ **Single-level Cell(SLC) Technology**

■ **OPEN NAND FLASH INTERFACE(ONFI)1.0 COMPLIANT**

■ **POWER SUPPLY VOLTAGE**
- VCC/VCCQ = 2.7V ~ 3.6V

■ **MEMORY CELL ARRAY (with SPARE)**
- Page size : (2K+128 spare) bytes
- Block size : (128K+8K) bytes
- Device size :4,096 blocks

■ **PAGE READ / PROGRAM**
- Random Read Time (tR)
  2KB Page : 45us(Typ) / 400us (Max)
- Sequential Access Time : 20ns(Min)
- Page Program Time : 350us(Typ)

■ **BLOCK ERASE**
- Block Erase Time: 4ms(Typ) / 10ms(Max)

■ **PACKAGE**
- Package type : TSOP
- Chip count : SDP
- Pin Count : 48
- size : 12mm x 20mm x 1.2mm
- Lead/Halogen Free

■ **ELECTRONIC SIGNATURE**
- 1st cycle : Manufacturer Code
- 2nd cycle : Device Code
- 3rd cycle : Internal chip number, Cell Type
- 4th cycle : Page size, Block size, Spare size, Organization
- 5th cycle : Multi-plane information

■ **OPERATING TEMPERATURE**
- -40℃ to 85℃

■ **RELIABILITY**
- 50,000 Program / Erase cycles
  (with 1 bit/512 Byte ECC)

■ **DATA RETENTION**
- 10 years

1. SUMMARY DESCRIPTION

Heyangtek HYN4G08UHTCC1 series are offered in 3.3 Vcc and VccQ Power Supply, and with x8 I/O interface. Its NAND cell provides the most cost-effective solution for the solid state mass storage market. The memory is divided into blocks that can be erased independently so it is possible to preserve valid data while old data is erased. In default, the device page size is (2,048 + 128 spare) bytes.

Each block can be programmed and erased up to 50,000 cycles with ECC (error correction code) on. To extend the lifetime of Nand Flash devices, the implementation of an ECC is mandatory.
The chip supports CE# don't care function. This function allows the direct download of the code from the NAND Flash memory device by a microcontroller, since the CE# transitions do not stop the read operation.

Program operation with multi-plane structure allows to program 2 pages at a time (one per each plane) when using of 2,048 bytes of page size, or to erase 2 blocks at a time (one per each plane). As a consequence, multi-plane architecture holds reduced program/erase time compared to operation at single-plane architecture. Both single and multi-plane operations are supported both with traditional and ONFI 1.0 protocols.

Data in the page can be read out at 20ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. This interface allows a reduced pin count and easy migration towards different densities without any rearrangement of footprint. Commands, Data and Addresses are synchronously introduced using CE#, WE#, ALE and CLE input pin.
The on-chip Program/Erase Controller automates all read, program and erase functions including pulse repetition, where required, and internal verification and margining of data.

A write protect pin is available to provide hardware protection against program and erase operations. This device features an open-drain ready/busy output identifying if the program/erase/read controller is currently active. The use of an open-drain output allows the ready/busy pins from several memories to connect to a single pullup resistor.

1.1. Pin Define

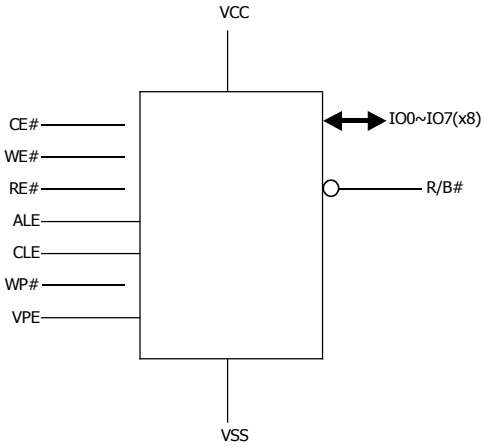


Figure 1 : Pin diagram(SDP)

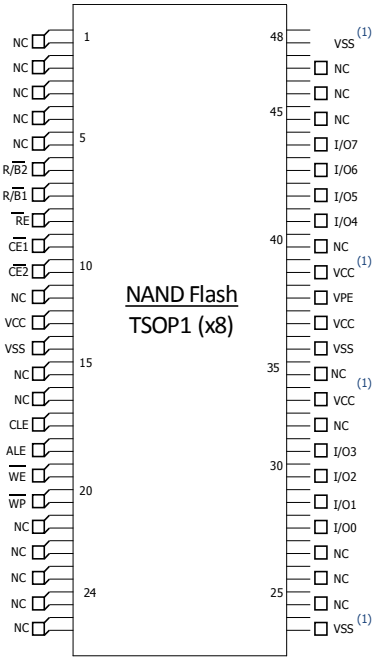


Figure 2 : 48-pin TSOP

Note 1:
These pins should be connected to power supply or ground (as designated), however, they might not be bonded internally.

1.2. Pin Description

Pin Name	Description
I/O 0 - I/O 07 (X8)	**DATA INPUTS/OUTPUTS** The I/O pins are used to COMMAND LATCH cycle, ADDRESS INPUT cycle, and DATA in-out cycles during read / write operations. The I/O pins float to High-Z when the device is deselected or the outputs are disabled.
CLE	**COMMAND LATCH ENABLE** This input activates the latching of the I/O inputs inside the Command Register on the Rising edge of Write Enable (WE#).
ALE	**ADDRESS LATCH ENABLE** This input activates the latching of the I/O inputs inside the Address Register on the Rising edge of Write Enable (WE#).
CE#	**CHIP ENABLE** This input controls the selection of the device. When the device is busy, CE# high does not deselect the memory. The device goes into Stand-by mode when CE# goes High during the device is in Ready state. The CE# signal is ignored when device is in Busy state, and will not enter Standby mode even if the CE# goes high.
WE#	**WRITE ENABLE** This input acts as clock to latch Command, Address and Data. The I/O inputs are latched on the rise edge of WE#.
RE#	**READ ENABLE** The RE# input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of RE# which also increments the internal column address by one.
WP#	**WRITE PROTECT** The WP# pin, when Low, provides a hardware protection against undesired write and erase operations. Hardware Write Protection is activated when the Write Protect pin is low. In this condition, program/erase operation cannot be started not to alter the content of the memory. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up phases.
VPE	**Volatile Protection Enable** The Volatile Protection Enable input, when high during power-on, provides block granularity hardware protection against undesired data modification (program/erase). This input has a weak internal pull-down (IPD) to disable the volatile protection features if the input is left floating.
R/B#	**READY / BUSY** The Ready/Busy output is an Open Drain pin that signals the state of the memory.
V_{CC}	**SUPPLY VOLTAGE** The VCC supplies the power for all the operations. (Read, Write, and Erase).
V_{SS}	**GROUND**
NC	**NO CONNECTED**

Table 1 : Signal descriptions

Note:
A 0.1uF capacitor should be connected between the Vcc Supply Voltage pin and the Vss Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations.

1.3. Package Dimensions

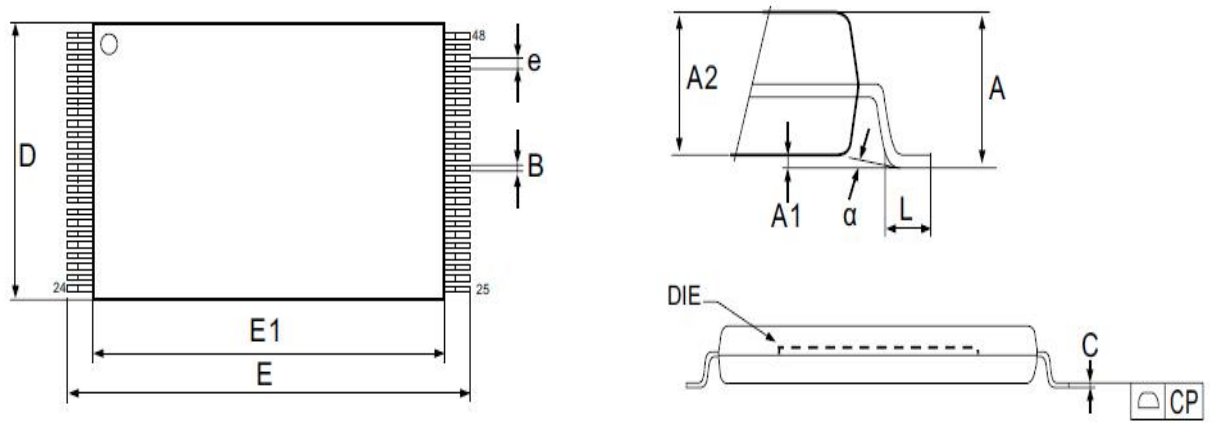


Figure 3 : 48-pin TSOP

Symbol	milimeters		
	Min	Typ	Max
A			1.200
A1	0.050		0.150
A2	0.980		1.030
B	0.170		0.250
C	0.100		0.200
CP			0.100
D	11.910	12.000	12.120
E	19.900	20.000	20.100
E1	18.300	18.400	18.500
e		0.500	
L	0.500		0.680
alpha	0		5

Table 2 : Package Mechanical Data

1.4. Functional Block Diagram

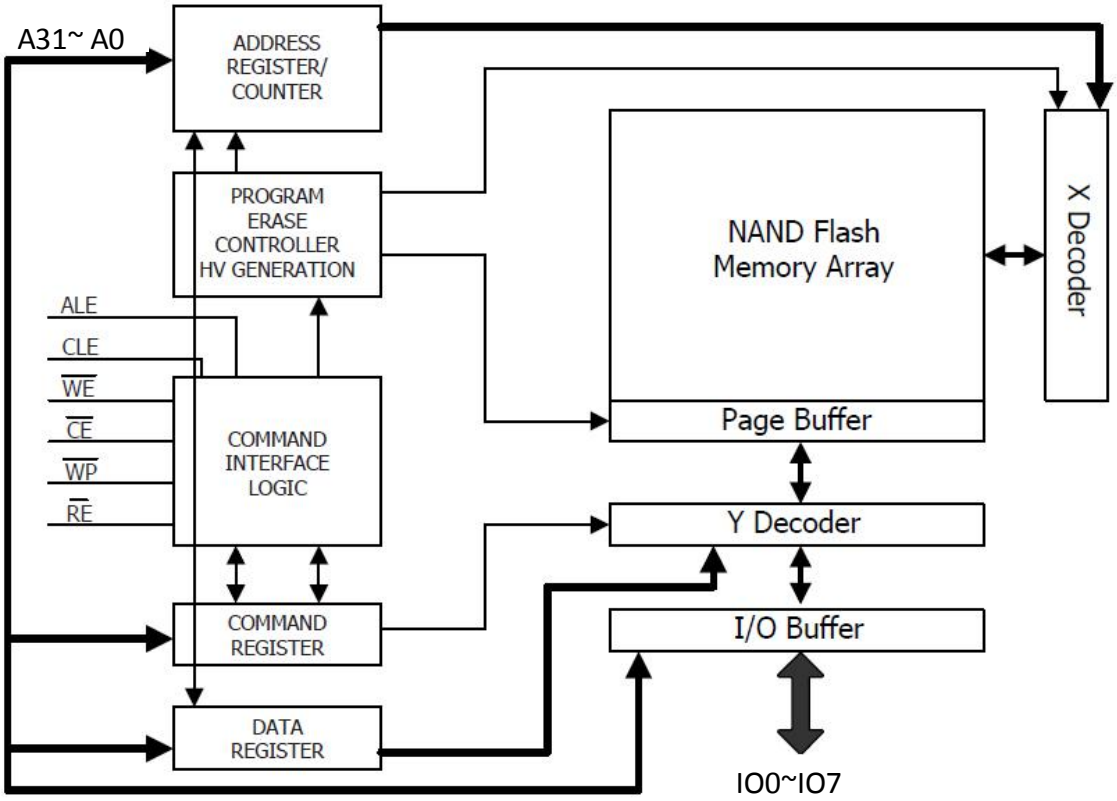


Figure 4 : Block diagram(SDP)

1.5. Memory Organization

A device contains one or more targets. A target is controlled by one CE# signal. A target is organized into one or more logical units (LUNs).
A logical unit (LUN) is the minimum unit that can independently execute commands and report status.

A block is the smallest erasable unit of data within the Flash array of a LUN. There is no restriction on the number of blocks within the LUN. A block contains a number of pages.

A page is the smallest addressable unit for read and program operations. A page consists of a number of bytes.

Each LUN shall have at least one page register. A page register is used for the temporary storage of data before it is moved to a page within the Flash array or after it is moved from a page within the Flash array.

The byte location within the page register is referred to as the column.

1.5.1. Addressing

1.5.1.1 Column and Row Addressing

There are two address types used: the column address and the row address. The column address is used to access bytes within a page, i.e. the column address is the byte offset into the page. The row address is used to address pages, blocks, and LUNs.

When both the column and row addresses are required to be issued, the column address is always issued first in one or more 8-bit address cycles. The row addresses follow in one or more 8-bit address cycles. There are some functions that may require only row addresses, such as Block Erase. In this case the column addresses shall not be issued.

For both column and row addresses the first address cycle always contains the least significant address bits and the last address cycle always contains the most significant address bits. If there are bits in the most significant cycles of the column and row addresses that are not used then they are required to be cleared to zero.

The row address structure is shown in Figure 6 "Row Addess Layout" with the least significant row address bit to the right and the most significant row address bit to the left.

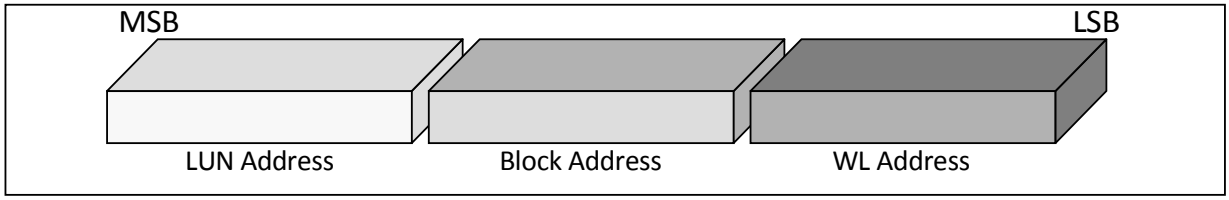


Figure 6 : Row Address Layout

The page address is set by the least significant row address bits, and the LUN address is set by the most significant row address bit(s). The block address is between a page address and a LUN address.

A host shall not access an address of a page or block beyond maximum Page Address or block address. The Addressing of this device is shown in Table of "Memory addressing".

1.5.2 Array Organization

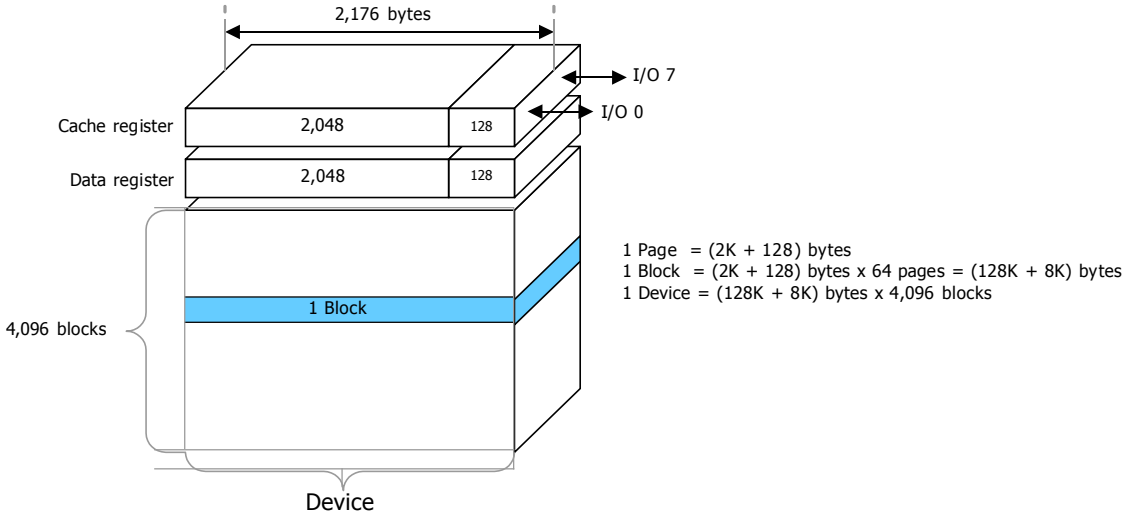


Figure 7 : Array organization

Bus cycle	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L(1)	L(1)	L(1)	L(1)
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27
5th(*) Cycle	A28	A29	A30	A31	L	L	L	L

Table 3 : Address Cycle Map

As far as the address bits are concerned, the following rules apply:
A0 - A11 : column address in the page
A12 - A17 : page address in the block
A18 - A31 : block address

Notes:
1. L must be set to Low.
2. The device ignores any additional address input cycle than required.
3. 1st & 2nd cycle are Column Address, 3rd to 5th cycle are Row Address

Row Address	Block Number	DQ2
000000h ~ 00003Fh	Block 0	Main Block (4,096Blocks)
000040h ~ 00007Fh	Block 1	
000080h ~ 0000BFh	Block 2	
0000C0h ~ 0000FFh	Block 3	
000100h ~ 00013Fh	Block 4	
000140h ~ 00017Fh	Block 5	
...	...	
03FF00h ~ 03FF3Fh	Block 4092	
03FF40h ~ 03FF7Fh	Block 4093	
03FF80h ~ 03FFBFh	Block 4094	
03FFC0h ~ 03FFFFh	Block 4095	

Table 4 : Block Arrangement

1.5.3. Valid Blocks

	Symbol	Page Size	Min	Max	Unit
Valid Block Number	N_{VB}	2KB	4016	4096	Blocks

Table 5 : Valid Blocks Number

Notes:
1. The 1st block , 1st chip per CE is guaranteed to be a valid block at the time of shipment.
2. Invalid blocks are one that contains one or more bad bits. The device may contain bad blocks upon shipment.

1.6. Command Set

FUNCTION	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	Acceptable while accessed LUN is busy	Acceptable while other LUNs are busy
RESET	FFh	-	-	-	Yes	Yes
GET FEATURE	EEh	-	-	-	-	-
SET FEATURE	EFh	-	-	-	-	-
READ STATUS	70h	-	-	-	Yes	Yes
READ STATUS ENHANCED	78h	-	-	-	Yes	Yes
RANDOM DATA INPUT	85h	-	-	-	-	Yes
RANDOM DATA OUTPUT	05h	E0h	-	-	-	Yes
PAGE READ	00h	30h	-	-	-	Yes
PAGE PROGRAM	80h	10h	-	-	-	Yes
PAGE RE-PROGRAM	8Bh	10h	-	-	-	Yes
BLOCK ERASE	60h	D0h	-	-	-	Yes
READ FOR COPY-BACK	00h	35h	-	-	-	Yes
COPY-BACK PROGRAM	85h	10h	-	-	-	Yes

Table 6 : Command Set

CLE	ALE	CE#	WE#	RE#	WP#	MODE	
H	L	L	Rising	H	X	Read Mode	Command Input
L	H	L	Rising	H	X		Address Input (5 Cycles)
H	L	L	Rising	H	H	Write Mode	Command Input
L	H[1)]	L	Rising	H	H		Address Input (5 Cycles)
L	L	L	Rising	H	H	Data Input	
L	L[1)]	L	H	Falling	X	Sequential Read and Data Output	
X	X	L[1)]	H	H	X	Data Output (suspended)	
L	L	L	H[3)]	H[3)]	X	During Read (Busy)	
X	X[1)]	X	X	X	H	During Program (Busy)	
X	X	X	X	X	H	During Erase (Busy)	
X	X	X	X	X	L	Write Protect	
X	X	H	X	X	0V/Vcc[2)]	Stand-By	

Table 7 : Mode Selection

Notes:
1. X can be VIL or VIH. H = Logic level HIGH. L = Logic level LOW.
2. WP# should be biased to CMOS high or CMOS low for stand-by mode.
3. WE# and RE# during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out. In this time, only Reset, Read Status, and multi-plane Read Status can be inputted to the device.

2. BUS OPERATION

There are six standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby. Typically glitches less than 5ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

2.1. Command Input

Command Input bus operation is used to give a command to the memory device. Command are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. During program/erase operations, the Write Protect pin must be high. See Figure 8 and "5.6. AC Timing Characteristics" for details of the timings requirements.

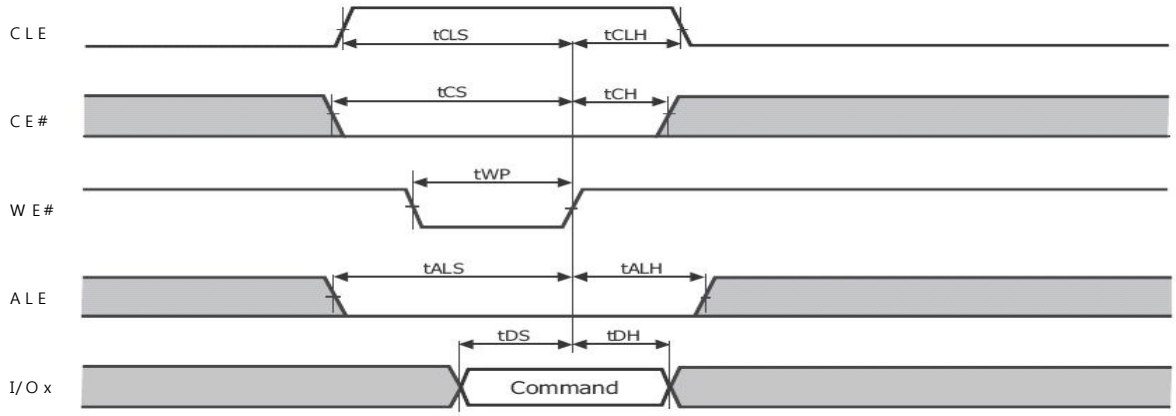


Figure 8 : Command latch timings

2.2. Address Input

Address Input bus operation allows the insertion of the memory address. 5 clock cycles are needed to input the addresses. (refer to "1.5.1 Addressing"). Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for the program/erase commands, the Write Protect pin must be high. See Figure 11 and "5.6. AC Timing Characteristics" for details of the timings requirements.

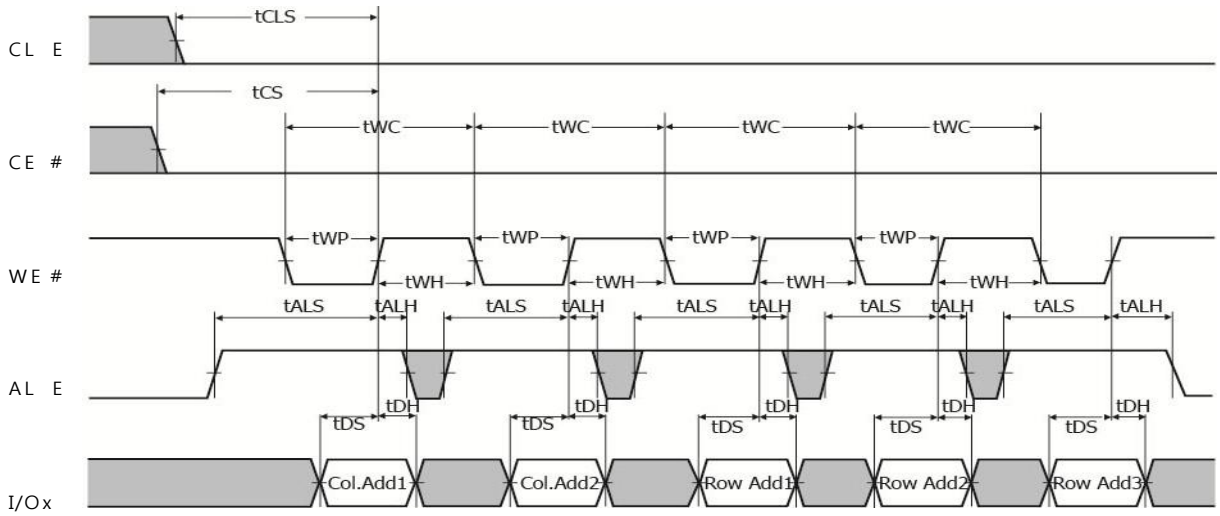


Figure 9 : Address latch timings

2.3. Data Input

Data Input bus operation allows to feed the data to be programmed. The data insertion is done in serial order by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable. See Figure 10 and "5.6. AC Timing Characteristics" for details of the timings requirements.

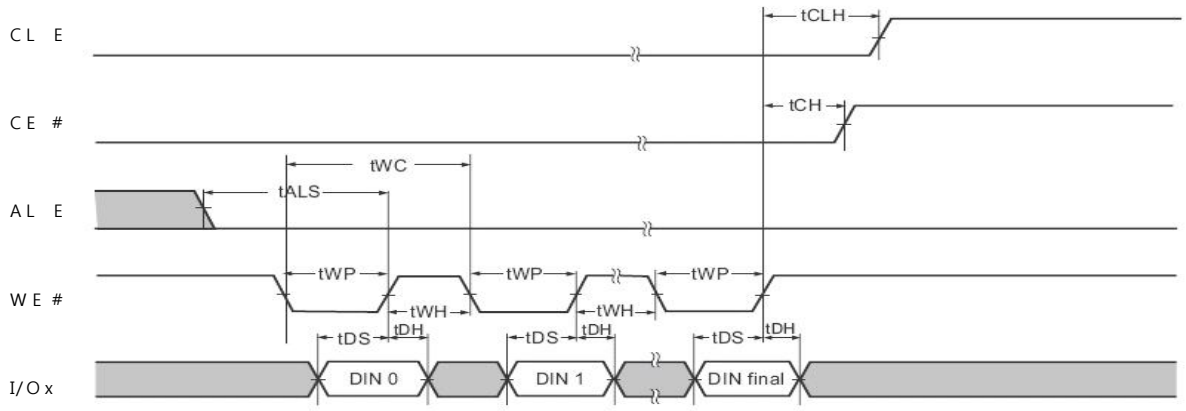


Figure 10 : Data Input cycle timings

Note:
Data Input cycle is accepted to data register on the rising edge of WE#, when CLE and CE# and ALE are low, and device is not Busy state.

2.4. Data Output

Data Output bus operation allows to read data from the memory array and to check the status register content and the ID data. Data can be serially shifted out by toggling the Read Enable pin with Chip Enable low, Write Enable High, Address Latch Enable low, and Command Latch Enable low. See Figure 11 to Figure 15 and "5.6. AC Timing Characteristics" for details of the timings requirements.

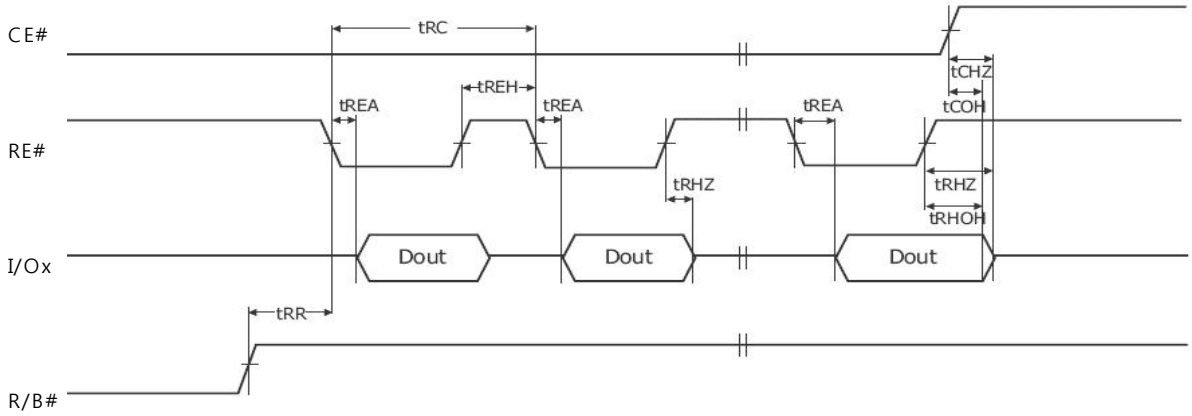


Figure 11 : Data output cycle timings (CLE=L, WE#=H, ALE=L, WP#=H)

Notes:
1. Transition is measured +/-200mV from steady state voltage with load. This parameter is sampled and not 100% tested. (t_{CHZ}, t_{RHZ})
2. t_{RHOH} starts to be valid when frequency is lower than 33 MHz. t_{RLOH} is valid when frequency is higher than 33 MHz

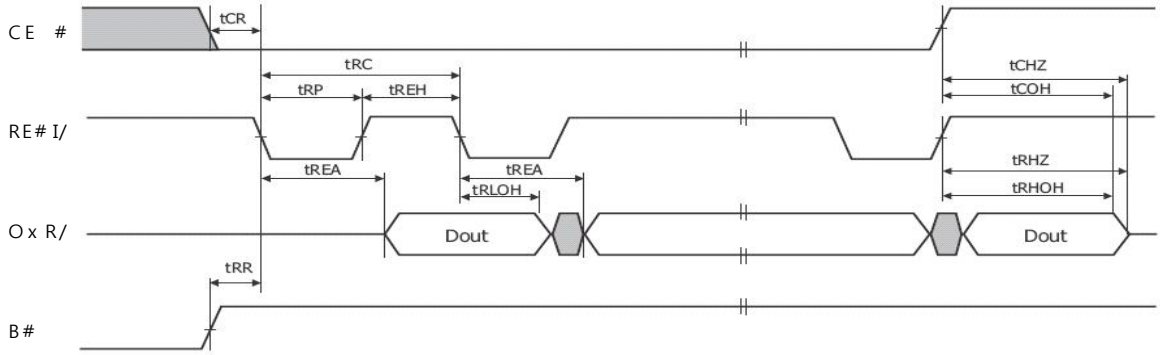


Figure 12 : Data output cycle timings (EDO type, CLE=L, WE#=H, ALE=L)

Notes:
1. Transition is measured +/-200mV from steady state voltage with load. This parameter is sampled and not 100% tested. (t_{CHZ}, t_{RHZ})
2. t_{RLOH} is valid when frequency is higher than 33 MHz. t_{RHOH} starts to be valid when frequency is lower than 33 MHz.

3. Device Operation

3.1. Reset

The device offers a reset feature, executed by writing FFh to the command register. If the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value E0h when WP# is high. If the device is already in reset state a new reset command will not be accepted by the command register. The RB# pin transitions to low for t_{RST} after the Reset command is written. Refer to Figure 13 for further details.

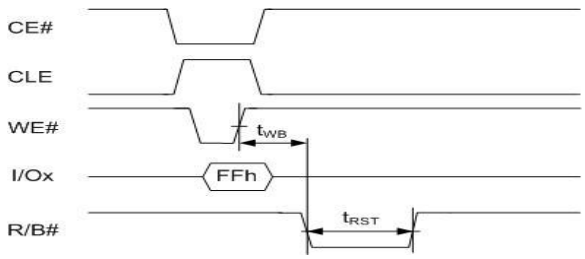


Figure 13 : Reset timings

3.2. Read ID

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h.
The 5-byte Read ID configuration are supported: The device operating mode (5-byte) is selected through cam setting.

3.2.1. Legacy Read ID

Five read cycles sequentially output the manufacturer code (01h), and the device code and 3rd, 4th, and 5th cycle ID, respectively. The command register remains in Read ID mode until further commands are issued to it.

Parameter	Symbol
Device Identifier Byte	Description
1st	Manufacturer Code
2nd	Device Identifier
3rd	Internal chip number, Cell Type
4th	Page size, Block size, Spare Size, Organization
5th	Multi-plane information

Table 8 : "Legacy" Read ID bytes meaning

3.2.2. Read ID Data Table (5cycle)

Density	Voltage (Vcc/VccQ)	Bus Width	Page Size	Manufacture Code	Device Code	3rd	4th	5th
4 Gbit	3.3V	X8	2KB	01h	DCh	00h	05h	04h

Table 9 : "Legacy" Read ID for supported configurations

3rd Byte of Device Identifier Description

3 rd cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
Cell Type	2 Level Cell					0	0		
Reserved	0	0	0	0	0				

Table 10 : Legacy Read ID 3rd byte description

4th Byte of Device Identifier Description

4 th cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size	2KB							0	1
(not including Spare Area)	4KB							1	0
Block Size	128KB	0		0	0				
(not including Spare Area)	256KB	0		0	1				
Spare Area Size	128B					0	1		
	256B					1	0		
Number of IO	X8		0						

Table 11 : Legacy Read ID 4th byte description

5th Byte of Device Identifier Description

5 th cycle	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Reserved		0	0	0	0			0	0

Table 12 : Legacy Read ID 5th byte description

3.3. Read Status

The device contains a Status Register which may be read to find out whether read, program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to be toggled for updated status. Refer to Figure 14 for specific timings requirements. The com- mand register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

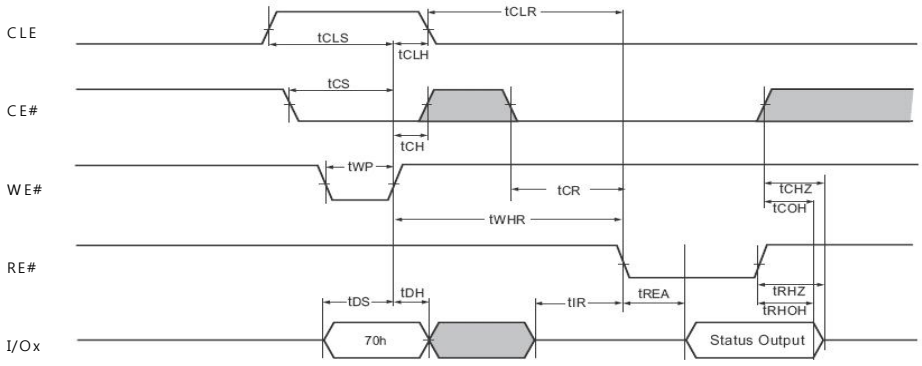


Figure 14 : Read Status timings

Refer to Table 17 for specific Status Register definition. The command register remains in Status Read mode until further commands are issue.

	Value Definition	Block Erase	Page Program	Page Read	OTP Block Protect
DQ0	Pass : "0" Fail : "1"	Pass / Fail	Pass / Fail	Not Use	Not Use
DQ1	Reserved	Not Use	Not Use	Not Use	Not Use
DQ2	Reserved	Not Use	Not Use	Not Use	Not Use
DQ3	Reserved	Not Use	Not Use	Not Use	Not Use
DQ4	(Flag 1) Page Recommended to Rewrite : "1" Page Normal/On-die ECC disabled : "0" (Flag 2) Page Uncorrectable : "1" Page Normal/On-die ECC disabled : "0"	Not Use	Not Use	Flag 1 (default) or Flag 2	Not Use
DQ5	Busy : "0" Ready : "1"	Not Use	Program in progress/ Completed	Not Use	Not Use
DQ6	Busy : "0" Ready : "1"	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy
DQ7	Protected : "0" Not Protected : "1"	Write Protect	Write Protect	Write Protect	Write Protect

Table 17 : Read Status Register Coding

Notes:

1. DQ0 : This bit is only valid for Program and Erase operations. If cleared to zero, then the last command was successful. If set to one, then the last command failed. For two plane operation, it indicates that one or both planes failed. The Read Status Enhanced (78h) operation can be used to determine with plane the operation failed. If a block is protected, this bit should fail
2. DQ4 : If the internal ECC is On, this bit indicates if the last pare read contained ECC errors. It is supported in two modes of Flag 1(default) or Flag 2, which is selectable usingfeature register address 90h bit [4]. These registers can be modified using the Set Feature command.
   - Flag 1 : The Flag indicate if one page has a high ECC error count and recommending to rewrite the page, when internal ECC disabled. If set to one, it is recommended to rewrite the entire page.
   - Flag 2 : If internal ECC is Off, this bit indicates ECC Pass/Fail. If set to one, it is ECC Fail and page is uncorrectable.
3. DQ5 : If set to one then there is no array operation in progress. If cleared to zero, then there is a command being progressed.
4. DQ7 : If set to one, then the device is not write protected. If cleared to zero, then the device is write protected. This bit shall always be valid regardless of state of the R/B#. For Status Enhanced command, signal follows WP pin.

3.4. Read Status Enhanced

Read Status Enhanced is an additional feature used to retrieve the status value for a previous operation in the following cases- on a specific die of a multi-dice stack configurations (single CE#), in case of concurrent operations When 4Gbit dies are stacked(*) to form 8Gbit DDP or 16Gbit QDP (single CE#), it is possible to run a first operation on the first 4Gbit, then activate a concurrent operation on the second (or third or fourth) device. (examples: Erase while Read, Read while Program, etc.) - on a specific plane in case of multi-plane operations in the same die.

Figure 15 defines the Read Status Enhanced behavior and timings. The plane and die address must be specified in the command sequence in order to retrieve the status of the die and the plane of interest. Read Status Enhanced command only shows block status of previously accessed block before issuing the command.

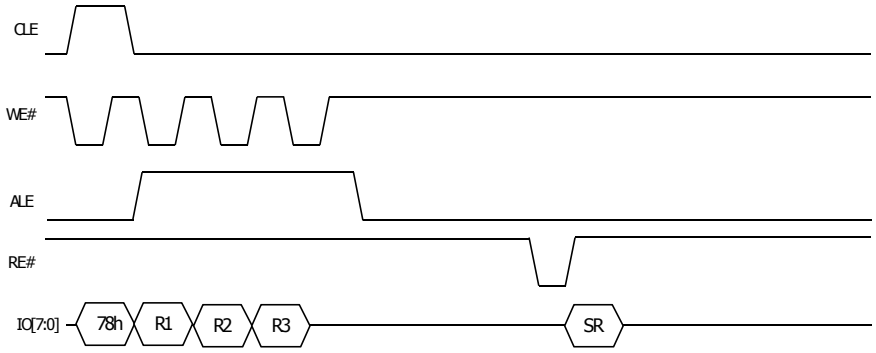


Figure 15 : Read Status Enhanced cycle

	Value Definition	Block Erase	Page Program	Page Read	OTP Block Protect
DQ0	Pass : "0" Fail : "1"	Pass / Fail	Pass / Fail	Not Use	Not Use
DQ1	Reserved	Not Use	Not Use	Not Use	Not Use
DQ2	Reserved	Not Use	Not Use	Not Use	Not Use
DQ3	OTP Not Protected : "0" OTP Protected : "1"	Not Use	Not Use	Not Use	Not Protected/ Protected
DQ4	(Flag 1) Page Recommended to Rewrite : "1" Page Normal/On-die ECC disabled : "0" (Flag 2) Page Uncorrectable : "1" Page Normal/On-die ECC disabled : "0"	Not Use	Not Use	Flag 1 (default) or Flag 2	Not Use
DQ5	Busy : "0" Ready : "1"	Not Use	Program in progress/ Completed	Not Use	Not Use
DQ6	Busy : "0" Ready : "1"	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy
DQ7	Protected : "0" Not Protected : "1"	Write Protect/ PBP/VBP	Write Protect/ PBP/VBP	Write Protect/ PBP/VBP	Write Protect/ PBP/VBP

Table 18 : Read Status Enhanced Register Coding

Notes:
DQ4, DQ5 defines ECC status.

3.5. Set Feature

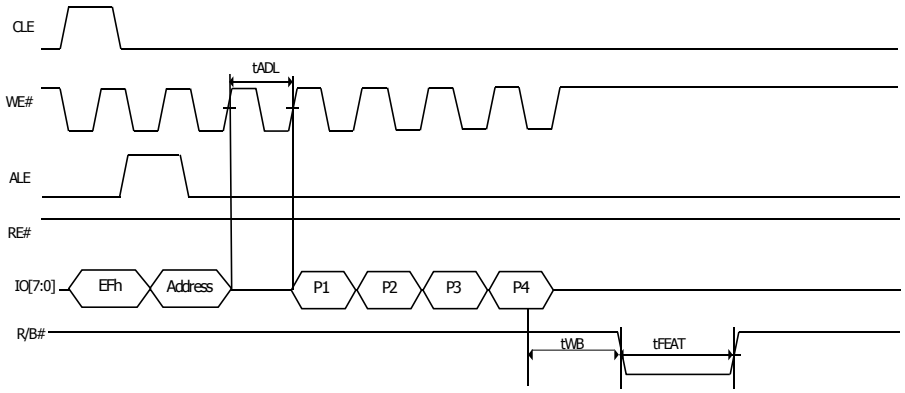


Figure 16 : Set Feature timing

3.6. Get Feature

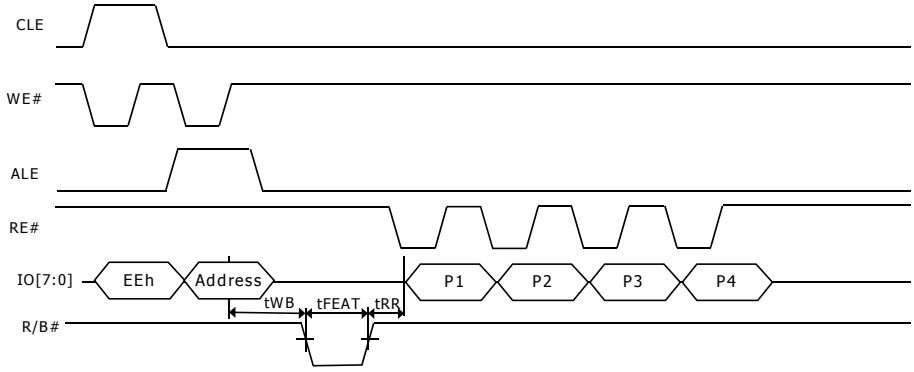


Figure 17 : Get Feature timing

Bits	Field Name	Function	Default State	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	Reserved	Reserved	0	
4	On-die ECC Status Description Select	On-die ECC Read Status Option Select	0	0: Flag1 1: Flag2
3	ECC_EN	ECC enable	1	1 : On-die ECC enabled (Default) 0 : On-die ECC disabled
2	Reserved	Reserved	0	
1	OTP Protection	OTP Area Protect	00	00 : OTP is not selected (Default) 01 : OTP Area Entry 11 : OTP Protection (Lock)
0	Normal vs. OTP operation	Normal (Array Operation)		

Table 19 : Feature Address 90h - Array Operation Mode (P1 register)

Notes:
1. P2/P3/P4 are 00h.
2. A software Reset command (FFh) will alter the content of the 90h feature register.
3. Bit4 of Feature Address 90h allows user to select if Read Status DQ4 shows Flag1 (default) or Flag2.
(Flag 1) Page Recommended to Rewrite : "1"/Page Normal/On-die ECC disabled : "0"
(Flag 2) Page Uncorrectable : "1"/Page Normal/On-die ECC disabled : "0"

Bits	Field Name	Function	Default State	Description
7	Reserved	Reserved	0	
6	Reserved	Reserved	0	
5	Reserved	Reserved	0	
4	Reserved	Reserved	0	
3	I/O Drive Strength	I/O Strength Selection	0000	0000: Full Strength (Default). 18Ω output impedance 0001: 75% of Full Strength, 25Ω output impedance 0010: 50% of Full Strength, 35Ω output impedance 0011: 25% of Full Strength, 50Ω output impedance
2				
1				
0				

Table 20 : Feature Address 80h - Programmable I/O Strength Mode (P1 register)

Notes:
1. P2/P3/P4 are 00h.
2. A software Reset command (FFh) does not alter the content of the 80h feature register.

3.7. DQ Driver Strength

The device may be configured with multiple driver strengths with Set Features command. Device supports Underdrive, Nominal, Overdrive1, and Overdrive2 options and each settings comply with the output driver requirements followed in this section.

Setting	Driver Strength	Vcc
18 Ohms	2.0x = 18 Ohms	3.3V
25 Ohms	1.4x = 25 Ohms	
35 Ohms	1.0x = 35 Ohms	
50 Ohms	0.7x = 50 Ohms	

Table 21 : I/O Drive Strength Settings

Output Strength	Rpd/Rpu	Vout to VSS	Minimum	Nominal	Maximum	Unit
Underdrive	Rpd	0.2 x Vcc	18.4	45.0	80.0	Ohm
		0.5 x Vcc	25.0	50.0	100.0	
		0.8 x Vcc	32.0	57.0	136.0	
	Rpu	0.2 x Vcc	32.0	57.0	136.0	
		0.5 x Vcc	25.0	50.0	100.0	
		0.8 x Vcc	18.4	45.0	80.0	
Nominal	Rpd	0.2 x Vcc	12.8	32.0	58.0	
		0.5 x Vcc	18.0	35.0	70.0	
		0.8 x Vcc	23.0	40.0	95.0	
	Rpu	0.2 x Vcc	23.0	40.0	95.0	
		0.5 x Vcc	18.0	35.0	70.0	
		0.8 x Vcc	12.8	32.0	58.0	
Overdrive1	Rpd	0.2 x Vcc	9.3	22.3	40.0	
		0.5 x Vcc	12.6	25.0	50.0	
		0.8 x Vcc	16.3	29.0	68.0	
	Rpu	0.2 x Vcc	16.3	29.0	68.0	
		0.5 x Vcc	12.6	25.0	50.0	
		0.8 x Vcc	9.3	19.0	40.0	
Overdrive2	Rpd	0.2 x Vcc	7.0	16.2	28.7	
		0.5 x Vcc	9.0	18.0	36.0	
		0.8 x Vcc	11.8	21.0	50.0	
	Rpu	0.2 x Vcc	11.8	21.0	50.0	
		0.5 x Vcc	9.0	18.0	36.0	
		0.8 x Vcc	7.0	14.0	28.7	

Table 22 : Output Drive Strength Impedance Values

Test conditions for impedance value verifications are listed on Table 23.

Condition	Temperature	Vcc	Process
Minimum Impedance	T_{OPER}(Min)	3.6V	Fast-Fast
Nominal Impedance	+25℃	3.3V	Typical-Typical
Maximum Impedance	T_{OPER}(Max)	2.7V	Slow-Slow

Table 23 : Test Conditions for Impedance Values

The pull-up and pull-down impedance mismatch requirements are defined in Table 24. Impedance mismatch is the absolute value between pull-up and pull-down impedances. Both are measured at the same temperature and voltage. The testing conditions that shall be used to verify the impedance mismatch requirements are Vcc = Vcc (min), Vout = Vcc x 0.5 and T_A is across the full operating range.

Drive Strength	Minimum	Maximum	Unit
Overdrive2	0	6.3	Ohms
Overdrive1	0	8.8	Ohms
Nominal	0	12.3	Ohms
Underdrive	0	17.5	Ohms

Table 24 : Pull-up and Pull-down Output Impedance Mismatch

3.8. Page Read

This operation is initiated by writing 00h and 30h to the command register along with five address cycles. Two types of operations are available: random read, serial page read. The random read mode is enabled when the page address is changed. The 4,352 bytes of data within the selected page are transferred to the data registers in less than 400us. The system controller may detect the completion of this data transfer (tR) by ana- lyzing the output of R/B# pin. Once the data in a page is loaded into the data registers, they may be read out in 20ns cycle time by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address. The device may output random data in a page instead of the sequential data by writing random data out- put command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command.
Random data output can be operated multiple times regardless of how many times it is done in a page.
Check Figure 18 to Figure 20 as references.

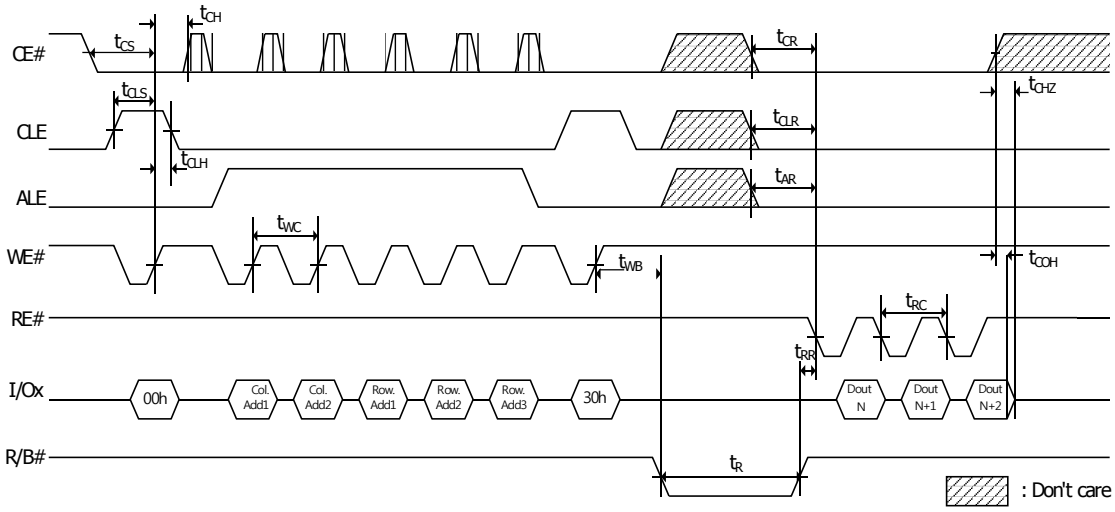


Figure 18 : Page Read Operation Timings (Intercepted by CE#)

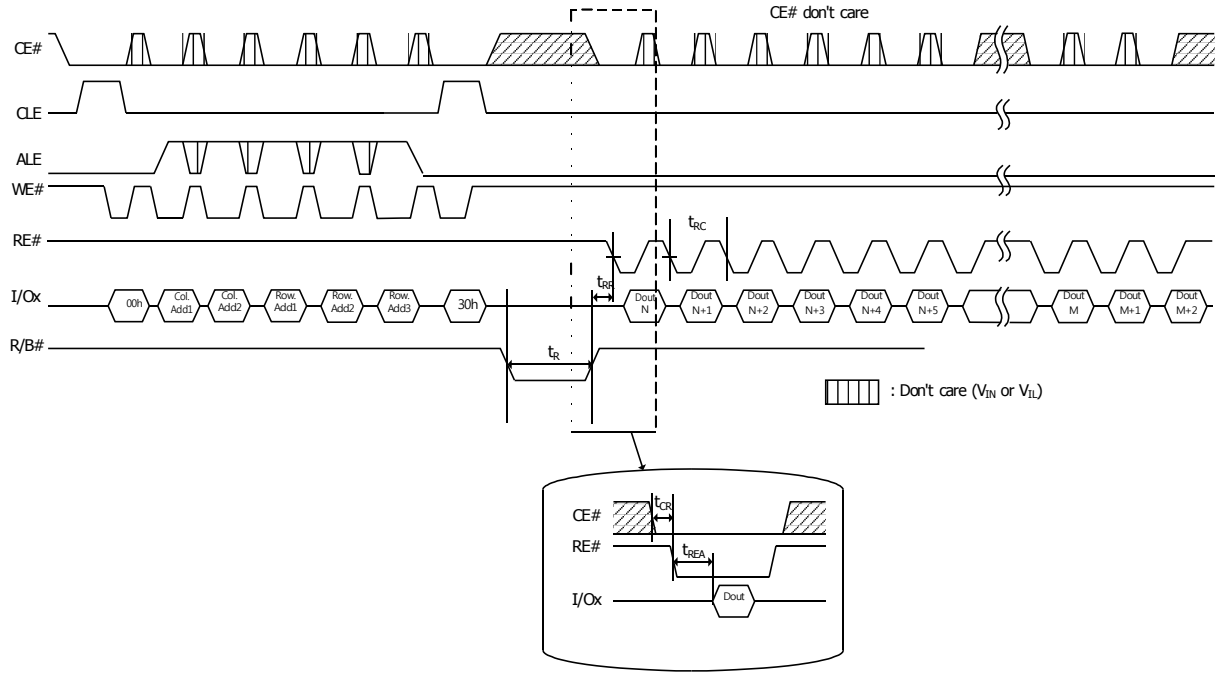


Figure 19 : Page Read Operation Timings with CE# don't care

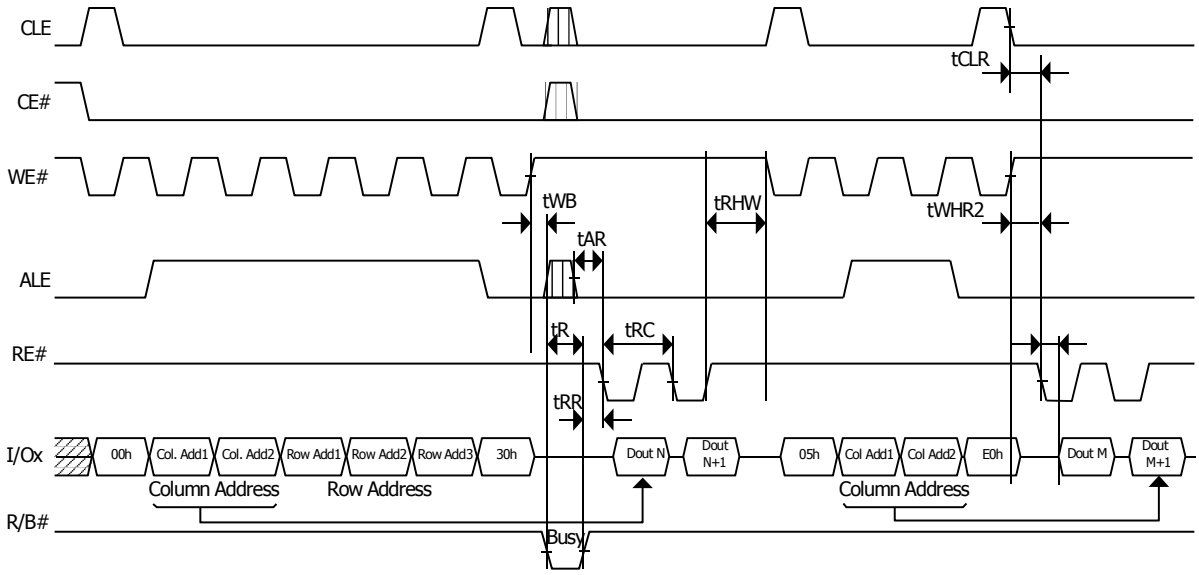


Figure 20 : Random Data Output timings

3.9. Page Program

A page program cycle consists of a serial data loading period in which up to 4,352 bytes of data may be loaded into the data register, followed by a non-volatile program- ming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the five cycle address inputs and then serial data. The words other than those to be programmed do not need to be loaded. The device sup- ports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The Page Program confirm command (10h) initiates the programming process. The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) or Reset command are valid during pro- gramming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is writ- ten to the command register. Figure 21 to Figure 23 detail the sequence. The device is programmed basi- cally by page, but it also allows multiple partial page programming of a word up to consecutive bytes up to 4,352 bytes in a single page program cycle. The basic unit of Program operation is 32bytes per 1 ECC chunk and Program input shall made if and only if 32bytes or more input data detected.
The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. Consequent input of to be programmed main data following with ECC user spare is not allowed. Main data shall be stored in main data region, and then use Random Data Input to change column to the address of user spare for programming of corresponding user spare of input data. Both main data and user spare shall be input for NOP operation; if only user spare input without main data par- tially programmed (NOP) at the same time, data is no longer guaranteed.

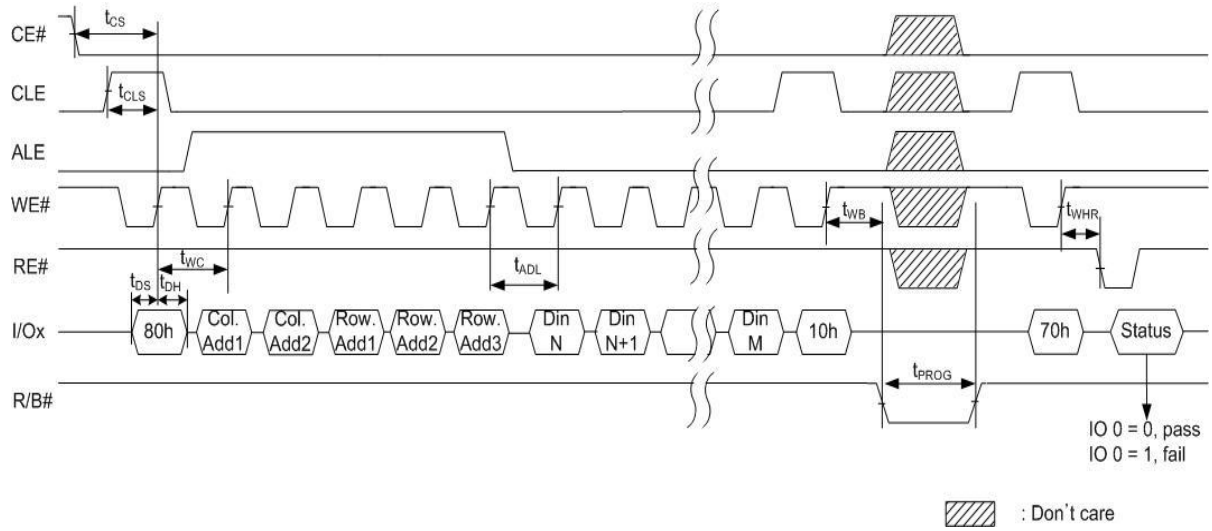


Figure 21 : Page Program Operation Timings

Note:
t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

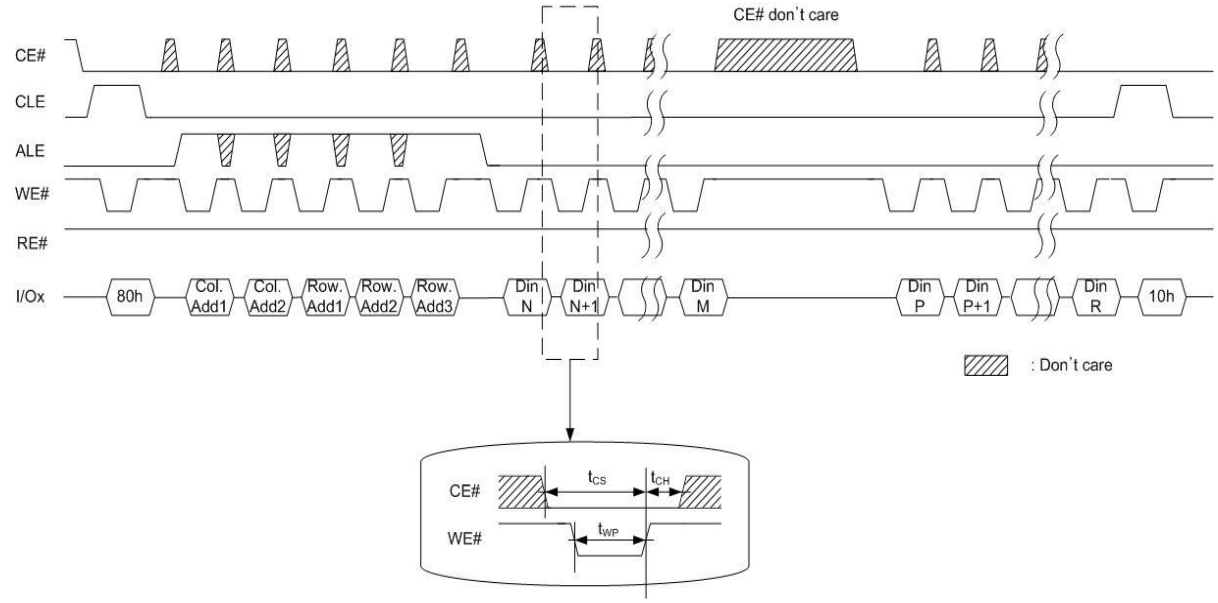


Figure 22 : Page Program Operation Timings with CE# don't care

Note:
t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.

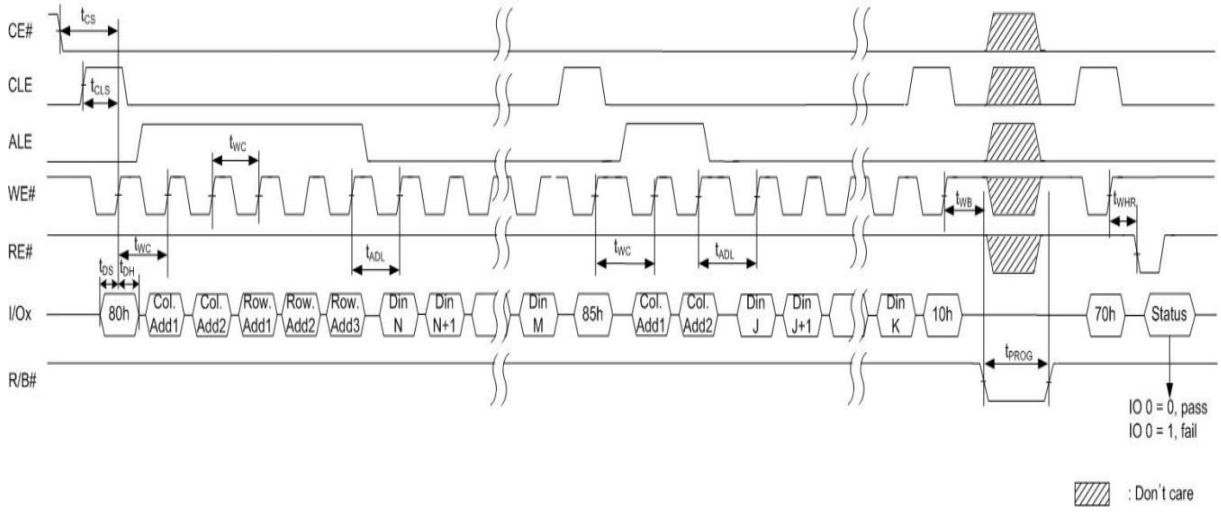


Figure 23 : Random Data Input Timings

Notes:
1. t_{ADL} is the time from the WE# rising edge of final address cycle to the WE# rising edge of first data cycle.
2. Random data input can be performed in a page.

3.9.1. Guidance to User Spare Program

The number of consecutive partial page programming operations within the same page must not exceed 4.

During NOP program, data that is designated to user spare area shall use random data input to change column address. Because NOP is allowed in maximum of 4 times, user spare area is also divided into 4 regions to match up to each NOP area. Main data is divided using NOP, and randomized while programming the data. Although user spare that is included in each NOP is also randomized, randomization done between main data and user spare are different as below Figure 24. Therefore, for each NOP, column address change shall be kept to match up correct NOP with NOP user spare.

At first, input 512 bytes of data for NOP0, then user spare data for NOP0 shall be inputted after changing of column address using Random Data Input. After programming of data, using of Random Data Input to return back to starting address of NOP1 main data shall be done. Secondly, input 512 bytes of NOP1 data, using Random Data Input to chagnge column address to user spare data for NOP1 inputting. After programming of user spare data for NOP1, return back to starting address of NOP2 main data starting address. NOP2 and NOP3 shall follow same manner as above.

If user decide to follow same order as programming order during data out, read out NOP0 area first, then using of Random Data Output to change column address to read out NOP0 user spare area shall be followed.

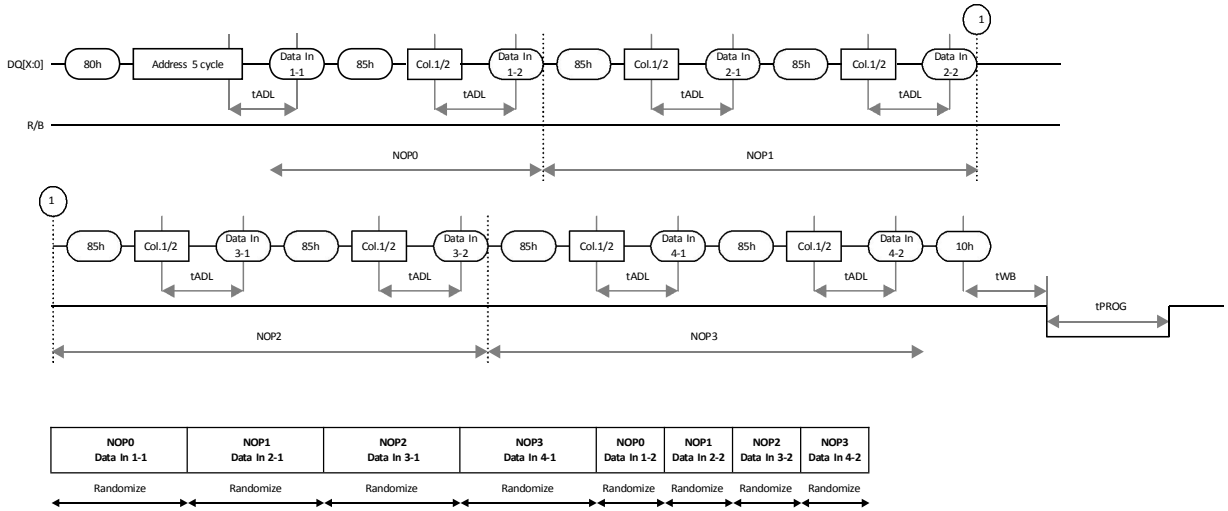


Figure 24 : Random Data Input Timings

NOP0	Column (Hex)	NOP1	Column (Hex)	NOP2	Column (Hex)	NOP3	Column (Hex)
Chunk0	000 ~ 01F	Chunk0	400 ~ 41F	Chunk0	800 ~ 81F	Chunk0	C00 ~ C1F
Chunk1	020 ~ 03F	Chunk1	420 ~ 43F	Chunk1	820 ~ 83F	Chunk1	C20 ~ C3F
Chunk2	040 ~ 05F	Chunk2	440 ~ 45F	Chunk2	840 ~ 85F	Chunk2	C40 ~ C5F
Chunk3	060 ~ 07F	Chunk3	460 ~ 47F	Chunk3	860 ~ 87F	Chunk3	C60 ~ C7F
Chunk4	080 ~ 09F	Chunk4	480 ~ 49F	Chunk4	880 ~ 89F	Chunk4	C80 ~ C9F
Chunk5	0A0 ~ 0BF	Chunk5	4A0 ~ 4BF	Chunk5	8A0 ~ 8BF	Chunk5	CA0 ~ CBF
Chunk6	0C0 ~ 0DF	Chunk6	4C0 ~ 4DF	Chunk6	8C0 ~ 8DF	Chunk6	CC0 ~ CDF
Chunk7	0E0 ~ 0FF	Chunk7	4E0 ~ 4FF	Chunk7	8E0 ~ 8FF	Chunk7	CE0 ~ CFF
Chunk8	100 ~ 11F	Chunk8	500 ~ 51F	Chunk8	900 ~ 91F	Chunk8	D00 ~ D1F
Chunk9	120 ~ 13F	Chunk9	520 ~ 53F	Chunk9	920 ~ 93F	Chunk9	D20 ~ D3F
Chunk10	140 ~ 15F	Chunk10	540 ~ 55F	Chunk10	940 ~ 95F	Chunk10	D40 ~ D5F
Chunk11	160 ~ 17F	Chunk11	560 ~ 57F	Chunk11	960 ~ 97F	Chunk11	D60 ~ D7F
Chunk12	180 ~ 19F	Chunk12	580 ~ 59F	Chunk12	980 ~ 99F	Chunk12	D80 ~ D9F
Chunk13	1A0 ~ 1BF	Chunk13	5A0 ~ 5BF	Chunk13	9A0 ~ 9BF	Chunk13	DA0 ~ DBF
Chunk14	1C0 ~ 1DF	Chunk14	5C0 ~ 5DF	Chunk14	9C0 ~ 9DF	Chunk14	DC0 ~ DDF
Chunk15	1E0 ~ 1FF	Chunk15	5E0 ~ 5FF	Chunk15	9E0 ~ 9FF	Chunk15	DE0 ~ DFF
Chunk16	200 ~ 21F	Chunk16	600 ~ 61F	Chunk16	A00 ~ A1F	Chunk16	E00 ~ E1F
Chunk17	220 ~ 23F	Chunk17	620 ~ 63F	Chunk17	A20 ~ A3F	Chunk17	E20 ~ E3F
Chunk18	240 ~ 25F	Chunk18	640 ~ 65F	Chunk18	A40 ~ A5F	Chunk18	E40 ~ E5F
Chunk19	260 ~ 27F	Chunk19	660 ~ 67F	Chunk19	A60 ~ A7F	Chunk19	E60 ~ E7F
Chunk20	280 ~ 29F	Chunk20	680 ~ 69F	Chunk20	A80 ~ A9F	Chunk20	E80 ~ E9F
Chunk21	2A0 ~ 2BF	Chunk21	6A0 ~ 6BF	Chunk21	AA0 ~ ABF	Chunk21	EA0 ~ EBF
Chunk22	2C0 ~ 2DF	Chunk22	6C0 ~ 6DF	Chunk22	AC0 ~ ADF	Chunk22	EC0 ~ EDF
Chunk23	2E0 ~ 2FF	Chunk23	6E0 ~ 6FF	Chunk23	AE0 ~ AFF	Chunk23	EE0 ~ EFF
Chunk24	300 ~ 31F	Chunk24	700 ~ 71F	Chunk24	B00 ~ B1F	Chunk24	F00 ~ F1F
Chunk25	320 ~ 33F	Chunk25	720 ~ 73F	Chunk25	B20 ~ B3F	Chunk25	F20 ~ F3F
Chunk26	340 ~ 35F	Chunk26	740 ~ 75F	Chunk26	B40 ~ B5F	Chunk26	F40 ~ F5F
Chunk27	360 ~ 37F	Chunk27	760 ~ 77F	Chunk27	B60 ~ B7F	Chunk27	F60 ~ F7F
Chunk28	380 ~ 39F	Chunk28	780 ~ 79F	Chunk28	B80 ~ B9F	Chunk28	F80 ~ F9F
Chunk29	3A0 ~ 3BF	Chunk29	7A0 ~ 7BF	Chunk29	BA0 ~ BBF	Chunk29	FA0 ~ FBF
Chunk30	3C0 ~ 3DF	Chunk30	7C0 ~ 7DF	Chunk30	BC0 ~ BDF	Chunk30	FC0 ~ FDF
Chunk31	3E0 ~ 3FF	Chunk31	7E0 ~ 7FF	Chunk31	BE0 ~BFF	Chunk31	FE0 ~ FFF
User Spare0 Chunk0	1000 ~ 101F	User Spare1 Chunk0	1040 ~ 105F	User Spare2 Chunk0	1080 ~ 109F	User Spare3 Chunk0	10C0 ~ 10DF
User Spare0 Chunk1	1020 ~ 103F	User Spare1 Chunk1	1060 ~ 107F	User Spare2 Chunk1	10A0 ~ 10BF	User Spare3 Chunk1	10E0 ~ 10FF

Table 25 : NOP Chunk Column Address

3.10. Page Re-program

This command allows the re-programming of the same pattern of the last (failed) page into another memory location. The command sequence initiates with re-program setup (8Bh), followed by the five cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the last page, the program confirm can be issued (10h) without any data input cycle. On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm "10h"
The device supports random data input within a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85h). Random data input may be operated multiple times regardless of how many times it is done in a page.
The "program confirm" command (10h) initiates the re-programming process.
The internal write state controller automatically executes the algorithms and controls timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the status register. The system controller can detect the completion of a program cycle by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid during programming is in progress. When the Page Program is complete, the Write Status Bit (I/O 0) may be checked. The inter- nal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

3.11. Block Erase

The Block Erase operation is done on a block basis. Block address loading is accomplished in 3 cycles initiated by an Erase Setup command (60h). Only addresses A18 to A31 are valid while A12 to A17 are ignored. The Erase Confirm command (D0h) following the block address loading initiates the internal eras- ing process. This two-step sequence of setup followed by execution command ensures that memory con- tents are not accidentally erased due to external noise conditions. At the rising edge of WE# after the erase confirm command input, the internal write controller handles erase and erase-verify. Once the erase process starts, the Read Status Register commands (70h or 78h) may be issued to read the status register. The system controller can detect the completion of an erase by monitoring the RB# output, or the Status bit (I/O 6) of the Status Register. Only the Read Status commands (70h or 78h) and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

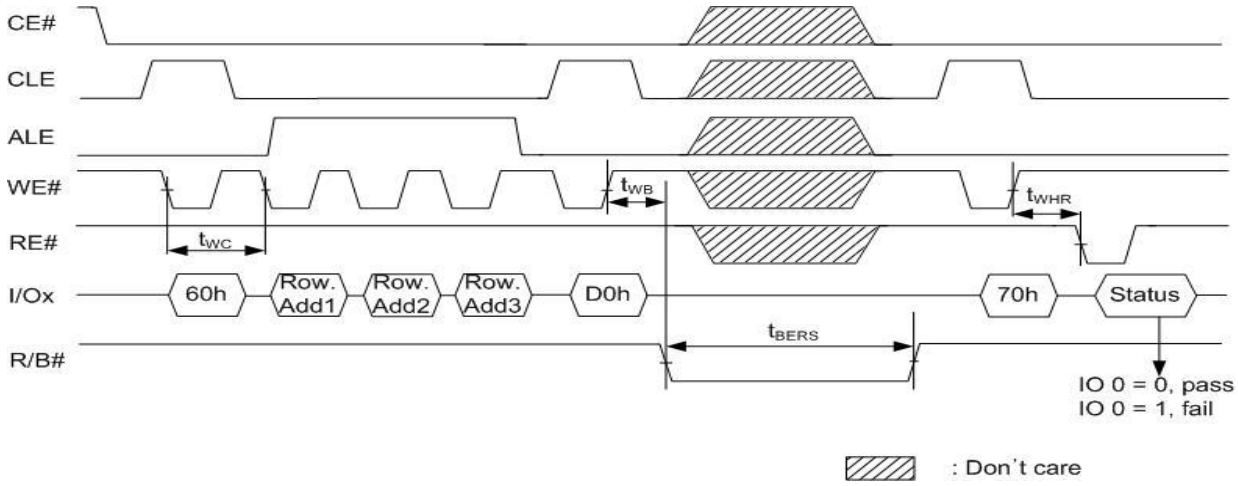


Figure 25 : Block Erase Operation Timings

3.12. Copy-back Program

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block.

The copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with "35h" command and the address of the source page moves the 4,352 bytes data into the internal data buffer. Because of copy-back read requires additional read time of 30us for 4KB Page. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or copy-back command (85h) with the address cycles of destination page may be written. The Program Confirm command (10h) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed as shown in Figure 26 "copy-back Program with Random Data Input".

When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. For this reason, one bit error correction correction is recommended for the use of Copy-Back operation. Figure 26 shows the command sequence for the copy-back operation. Please note that there are two things to do during copy-back program. First, Random Data Input (with/without data) is entered before Program Confirm command(10h) after Random Data output. Second, WP# value is don't care during Read for copy-back, while it must be set to Vcc When performing the program.

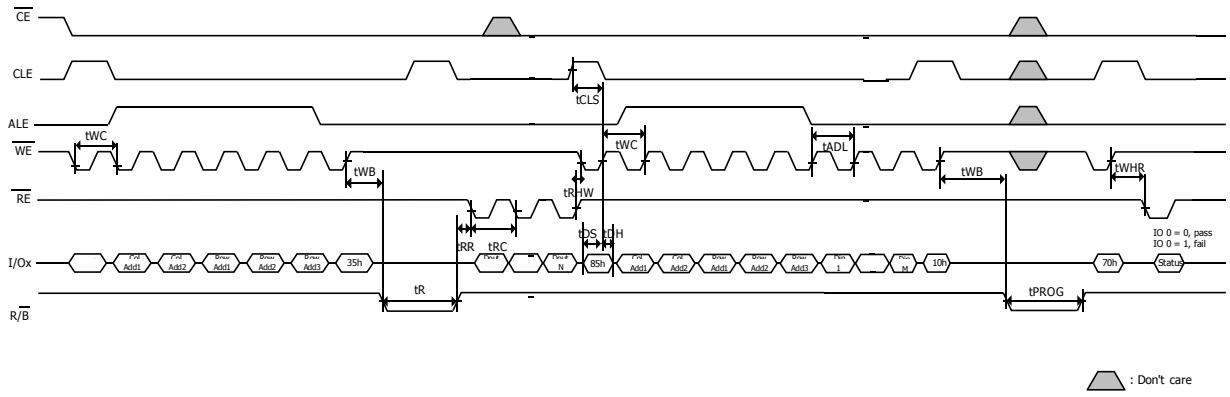


Figure 26 : Copy-back Program Operation Timing with Random Data Input

Note:
tADL is the time from the WE rising edge of final address cycle to the WE rising edge of first data cycle.

4. Other Features

4.1. Initialization (Power Up Sequence)

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{CC} is below about 1.8 V (3.3 V Device). WP# pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 100us is required before internal circuit gets ready for any command sequences as shown in Figure 27. The two-step command sequence for program/erase provides additional software protection.

Issuing of FFh command after Power Up Sequence allows Auto CAM read of the device.

The host must wait for R/B# to be valid High before issuing RESET command (FFh) to initialize any targets that share same CE#.The R/B# signal becomes valid after 100us since VCC reaches 2.7V. The RESET command (FFh) must be issued to all targets as the first command after the NAND device is powered up and R/B# becomes valid. Each target (CE) will be busy for a maximum of 2ms after the RESET command (FFh) is issued. The RESET busy time can be monitored by polling R/B# or issuing the READ STATUS (70h) command (when multi LUNs shared same CE Read Status Enhanced command should be used instead of READ STATUS). Each NAND die (LUN) may draw less than 10mA for over 1ms prior to the execution of the first RESET command (FFh) after the device is powered up. During the power up sequence including the RESET busy time, each LUN consumes a maximum current of 50mA.

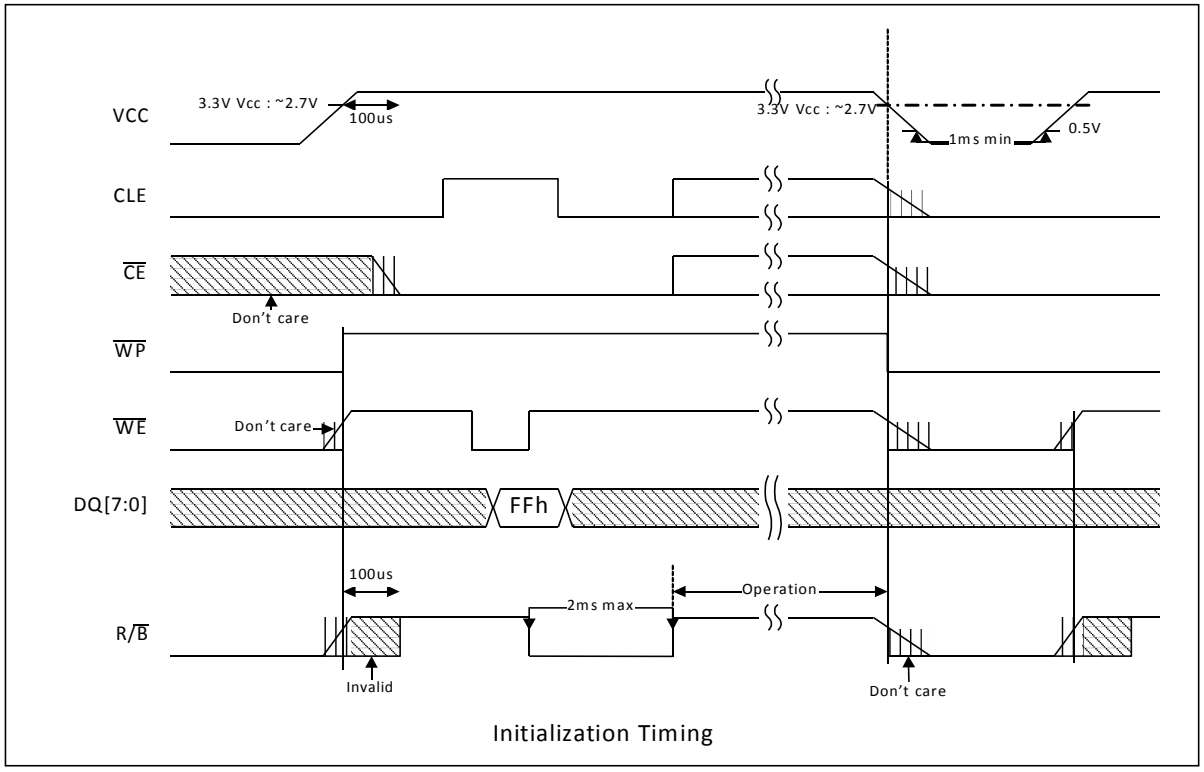


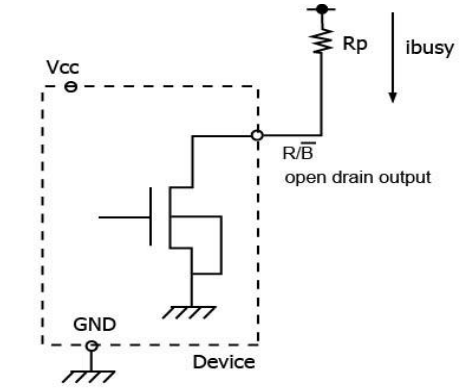
Figure 27 : Data Initialization

Notes:

1. During the initialization, the device consumes a maximum current of ICC1.
2. Once Vcc drops under 2.5V, it is recommended to drive down Vcc to below 0.5V and stay low for at least 1ms before Vcc powered up. Floating Vcc/VccQ during power-down is prohibited.

4.2. Ready / Busy

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tR (R/B#) and current drain during busy (I_{busy}), an appropriate value can be obtained with the following reference chart (Figure 28). Its value can be determined by the following guidance.



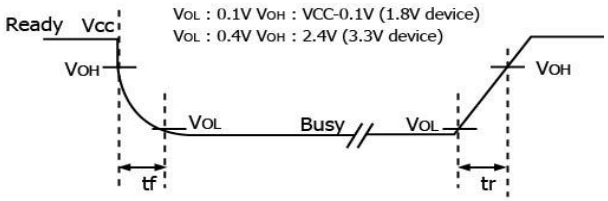


Fig. Rp vs tr, tf & Rp vs ibusy
@ Vcc = 3.3V, Ta = 25°C, CL=50pF

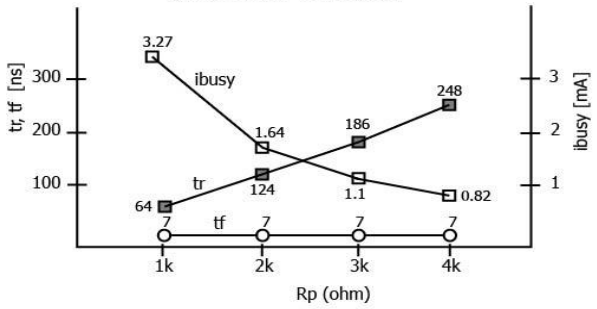
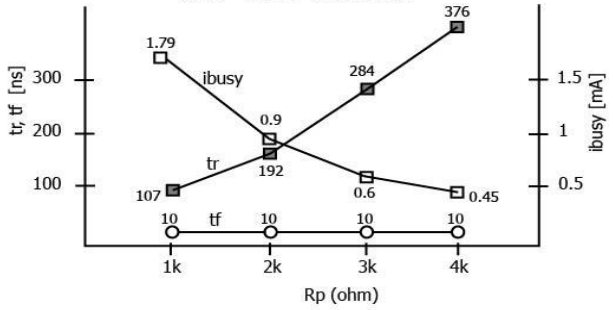


Fig. Rp vs tr, tf & Rp vs ibusy
@ Vcc = 1.8V, Ta = 25°C, CL=30pF



Rp value guidence

$$\text{Rp (min 3.3V device)} = \frac{\text{Vcc (Max.) - VOL (Max.)}}{\text{IOL + }\Sigma\text{IL}} = \frac{3.2\text{V}}{8\text{mA + }\Sigma\text{IL}}$$

$$\text{Rp (min 1.8V device)} = \frac{\text{Vcc (Max.) - VOL (Max.)}}{\text{IOL + }\Sigma\text{IL}} = \frac{1.85\text{V}}{3\text{mA + }\Sigma\text{IL}}$$

where IL is the sum of the input currnts of all devices tied to the R/$\overline{B}$ pin.

Rp(max) is determined by maximum permissible limit of tr

Figure 28 : Ready/Busy Pin Electrical Specifications

4.3. Write Protect

Hardware write protection is activated, when the Write Protect pin is low. However, during program/erase operation, Write Protect pin shall stay high not to alter the content of the memory. Write Protect pin is not latched by Write Enable to ensure the protection even during the power up.

4.3.1. Write Protect (WP#) handling

Erase and program operations are aborted if WP# is driven low during busy time, and kept low for about 100nsec. Switching WP# low during this time is equivalent to issuing a Reset command (FFh)
The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The R/B# pin will stay low for t_{RST}. At the end of this time, the command register is ready to process the next command, and the Status Register bit IO<6> will be cleared to "1", while IO<7> value will be related to the WP# value. Erase and program operations are enabled or disabled by setting WP# to high or low respectively prior to issuing the setup commands (80h or 60h).
The level of WP# shall be set tWW nsec prior to raising the WE# pin for the set up command, as explained in Figure 29~32. The Erase and Program Operations are automatically reset when WP# goes Low (t_{WW} = 100ns, min). The operations are enabled and disabled as follows.

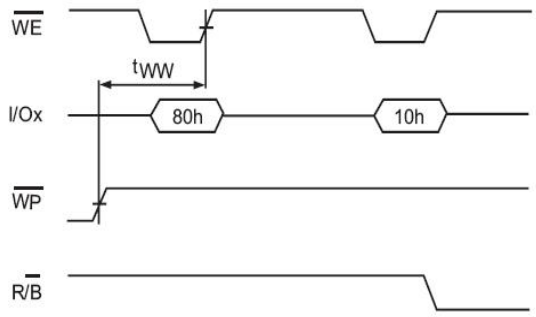


Figure 29 : Enable Program

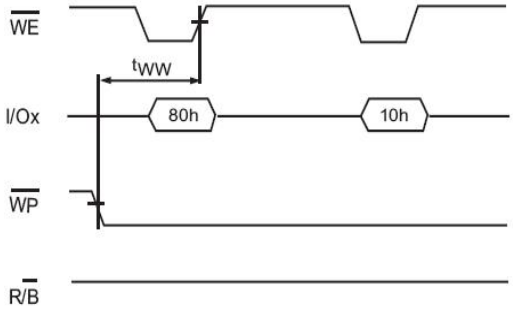


Figure 30 : Disable Program

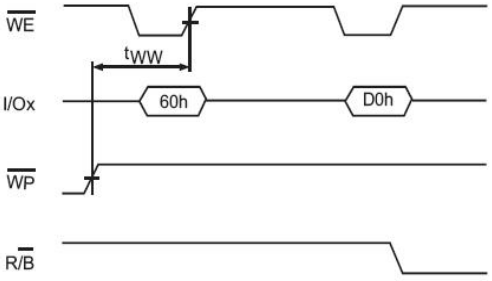


Figure 31 : Enable Erase

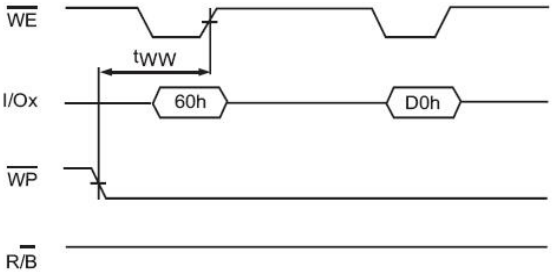


Figure 32 : Disable Erase

4.4. Standby

In Standby the device is deselected, outputs are disabled and Power Consumption is reduced.

5. Device Parameters

5.1. Absolute Maximum Rating

Symbol	Parameter	Value	Unit
		Min	
T_A (Ambient Operating Temperature)	Industrial	-40 to 85	℃
T_{BIAS}	Temperature Under Bias	-50 to 125	℃
T_{STG}	Storage Temperature	-65 to 150	℃
V_{IO}	Input or Output Voltage	-0.6 to 4.6	V
V_{CC}	Supply Voltage	-0.6 to 4.6	V

Table 31 : Absolute maximum ratings

Notes:

1. Please contact to Heyangtek office and confirm the availability of the product.
2. Minimum Voltage may undershoot to -2V during transition and for less than 20ns during transitions.
3. Except for the rating "Operating Temperature Range", stresses above those listed in the Table 31 "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

5.2. DC and Operating Characteristics

Parameter		Symbol	Test Conditions	2.7V ~ 3.6V			Units
				Min	Typ	Max	
Operating Current	Read	I_{CC1}	t_{RC}= t_{RC}(min), CE#=V_{IL}, I_{OUT}=0 mA	-	25	35	mA
	Program	I_{CC2}	Normal	-	25	35	mA
	Erase	I_{CC3}	-	-	15	30	mA
Stand-by Current (CMOS)		I_{SB}	CE#=V_{CC}-0.2 , WP#=0V/V_{CC}	-	-	100	uA
Input Leakage Current		I_{LI}	V_{IN}=0 to $V_{CC(MAX)}$	-	-	±10	uA
Output Leakage Current		I_{LO}	V_{OUT}=0 to $V_{CC(MAX)}$	-	-	±10	uA
Input High Voltage		V_{IH}	-	V_{CC}x0.8	-	V_{CC}+0.3	V
Input Low Voltage		V_{IL}	-	-0.3	-	0.2xV_{CC}	V
Output High Voltage Level		V_{OH}	I_{OH}=-400 uA	2.4	-	-	V
Output Low Voltage Level		V_{OL}	I_{OL}= 2.1 mA	-	-	0.4	V
Output Low Current (R/B#)		I_{OL} (R/B#)	V_{OL}= 0.4V	8	10	-	mA

Table 32 : DC and Operating Characteristics

5.3. AC Test Conditions

Parameter	Value
	2.7V ≤ Vcc ≤ 3.6V
Input Pulse Levels	0 V to V_{CC}
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	V_{CC} / 2
Output Load (2.7V-3.6V)	1 TTL GATE and CL=50_{pF}

Table 33 : AC Test Conditions

Note:
These parameters are verified device characterization and are not 100% tested

5.4. Pin Capacitance (T_A=25℃, F=1.0MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	-	10	pF
$C_{I/O}$	Input/Output Capacitance	V_{IL} = 0V	-	10	pF

Table 34 : Pin Capacitance Parameters

5.5. Program/ Read / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Program Time	t_{PROG}	-	350	600	us
Number of partial Program Cycles in the same page	NOP	-	-	4	cycles
Dummy Busy Time for Multi-Plane setting	t_{DBSY}	-	TBD	1	us
Read	t_R	-	45	400	us
Block Erase Time	t_{BERS}	-	4	10	ms

Table 35 : Program / Erase Characteristics

Notes:
Typical value is measured at Vcc=3.3V, T_A=25℃(3.3V Device). Not 100% tested.

5.6. AC Timing Characteristics

Parameter	Symbol	3.3V		Unit
		Min	Max	
CLE setup time	t_{CLS}	10	-	ns
CLE Hold time	t_{CLH}	5	-	ns
CE# setup time	t_{CS}	15	-	ns
CE# hold time	t_{CH}	5	-	ns
WE# pulse width	t_{WP}	10	-	ns
ALE setup time	t_{ALS}	10	-	ns
ALE hold time	t_{ALH}	5	-	ns
Data setup time	t_{DS}	7	-	ns
Data hold time	t_{DH}	5	-	ns
Write cycle time	t_{WC}	20	-	ns
WE# high hold time	t_{WH}	7	-	ns
Address to data loading time	t_{ADL}	70	-	ns
ALE to RE# delay	t_{AR}	10	-	ns
CLE to RE# delay	t_{CLR}	10	-	ns
Ready to RE# low	t_{RR}	20	-	ns
RE# pulse width	t_{RP}	10	-	ns
WE# high to busy	t_{WB}	-	100	ns
Read cycle time	t_{RC}	20	-	ns
RE# access time	t_{REA}	-	16	ns
RE# high to output high Z	t_{RHZ}	-	100	ns
CE# high to output high Z	t_{CHZ}		30	ns
CE# high to ALE or CLE Don't care	t_{CSD}	10	-	ns
RE# high to output hold	t_{RHOH}	15	-	ns
RE# low to output hold	t_{RLOH}	5	-	ns
RE# or CE# high to output hold	t_{COH}	15	-	ns
RE# high hold time	t_{REH}	7	-	ns
Output Hi-Z to RE# Low	t_{IR}	0	-	ns
RE# high to WE# low	t_{RHW}	100	-	ns
WE# high to RE# low	t_{WHR}	60	-	ns
WE# high to RE# low for Random data out	t_{WHR2}	200	-	ns
CE# low to RE# low	t_{CR}	10	-	ns
Device resetting time (Read/Program/Erase)	t_{RST}	-	5/10/500	us
Write protect time	t_{WW}	100	-	ns

Table 36 : AC Timing Characteristics

Notes:

1. If Reset Command (FFh) is written at Ready state, the device goes into Busy for maximum 5us.

6.1. Revision History

Publication Version:	V1.0 05/12/2021
Note:	First Release