GaN Power Device

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic RDS(on)eff production tested
- Robust design, defined by
  — Wide gate safety margin
  — Transient over-voltage capability
- Very low QRR
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Product Summary		
V_{DSS}	650	V
$R_{DS(on), typ}$	150	mΩ
$Q_{G, typ}$	8	nC
$Q_{RR, typ}$	40	nC

Applications

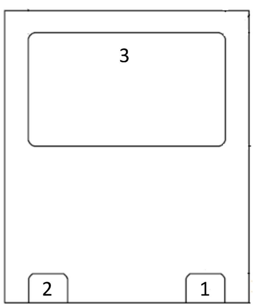
- Consumer
- Power adapters
- Low power SMPS
- Lighting

Main Characteristics

V_{DS}	650 V
$R_{DS(ON)}$	180 mΩ
Current@T_C=25°C $_b$	13 A

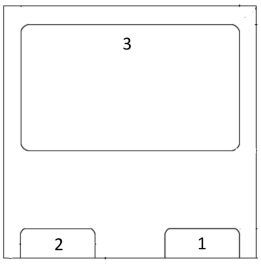
Product Information

(1) DFN 5X6-Dual Punch



Pin No.	Name	Function
1	G	Gate
2	D	Drain
3	S	Source

(2) DFN 8X8



Pin No.	Name	Function
1	G	Gate
2	D	Drain
3	S	Source

Device Information

Part Number	package	packing
GN3065T4ZG	DFN5*6	Tape 4K/reel
GN3065T5ZG	DFN8*8	Tape 3K/reel

Absolute Maximum Ratings (T_c=25°C)

Drain to source voltage (T_J = -55°C to 150°C) -- 650 (V)

Transient drain to source voltage a --800 (V)

Gate to source voltage --- ±20 (V)

Maximum power dissipation @TC=25°C -- 52(W)

Continuous drain current @TC=25°C b --- 13(A)

Continuous drain current @TC=100°C b --- 8.4(A)

Pulsed drain current (pulse width: 10μs) -- 60(A)

Operating temperature Case -- -55 to +150(°C)

Operating temperature Junction -- -55 to +150(°C)

Storage temperature --- -55 to +150(°C)

Reflow soldering temperature c -- 260(°C)

Notes:

a. In off-state, spike duty cycle D<0.01, spike duration <30.00s. Nonrepetitive.
b. For increased stability at high current operation, see Circuit Implementation on page 3
c. Reflow MSL3

Electrical Parameters (T_J = 25°C)

Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
		Forward Device Characteristics				
$V_{DSS(BL)}$	Maximum drain-source voltage	V_{GS}=0V	650	—	—	V
$V_{GS(th)}$	Gate threshold voltage	V_{DS}=V_{GS}, I_D=0.5mA	3.3	4	4.8	V
$\Delta V_{GS(th)}/T_J$	Gate threshold voltage temperature coefficient	V_{DS}=V_{GS}, I_D=0.5mA	—	-5.8	—	mV/°C
$R_{DS(on)eff}$	Drain-source on-resistance [a]	V_{GS}=10V, I_D=8.5A, T_J=25°C	—	150	180	mΩ
		V_{GS}=10V, I_D=8.5A, T_J=150°C	—	307	—	
I_{DSS}	Drain-to-source leakage current	V_{DS}=650V, V_{GS}=0V, T_J=25°C	—	2.5	25	μA
		V_{DS}=650V, V_{GS}=0V, T_J=150°C	—	10	—	
I_{GSS}	Gate-to-source forward leakage current	V_{GS}=20V	—	—	100	nA
	Gate-to-source reverse leakage current	V_{GS}=-20V	—	—	-100	
C_{ISS}	Input capacitance	V_{GS}=0V, V_{DS}=400V, f=1MHz	—	598	—	pF
C_{OSS}	Output capacitance		—	30	—	
C_{RSS}	Reverse transfer capacitance		—	1	—	
$C_{O(er)}$	Output capacitance, energy related [b]	V_{GS}=0V, V_{DS}=0V to 400V	—	43	—	pF
$C_{O(tr)}$	Output capacitance, time related [c]		—	85	—	
Q_G	Total gate charge	V_{DS}=400V, V_{GS}=0V to 10V, I_D=8.5A	—	8	—	nC
Q_{GS}	Gate-source charge		—	3.3	—	
Q_{GD}	Gate-drain charge		—	2	—	
Q_{OSS}	Output charge	V_{GS}=0V, V_{DS}=0V to 400V	—	34	—	nC
$t_{D(on)}$	Turn-on delay	V_{DS}=400V, V_{GS}=0V to 12V, I_D=10A, R_G=70Ω, Z_{FB}=240Ω at 100MHz (See Figure 14)	—	37.8	—	nS
t_R	Rise time		—	5.2	—	
$t_{D(off)}$	Turn-off delay		—	48	—	
t_F	Fall time		—	8	—	

Notes:

a. Dynamic $R_{DS(on)}$ value; see Figures 18 and 19 for conditions
b. Equivalent capacitance to give same stored energy from 0V to 400V
c. Equivalent capacitance to give same charging time from 0V to 400V

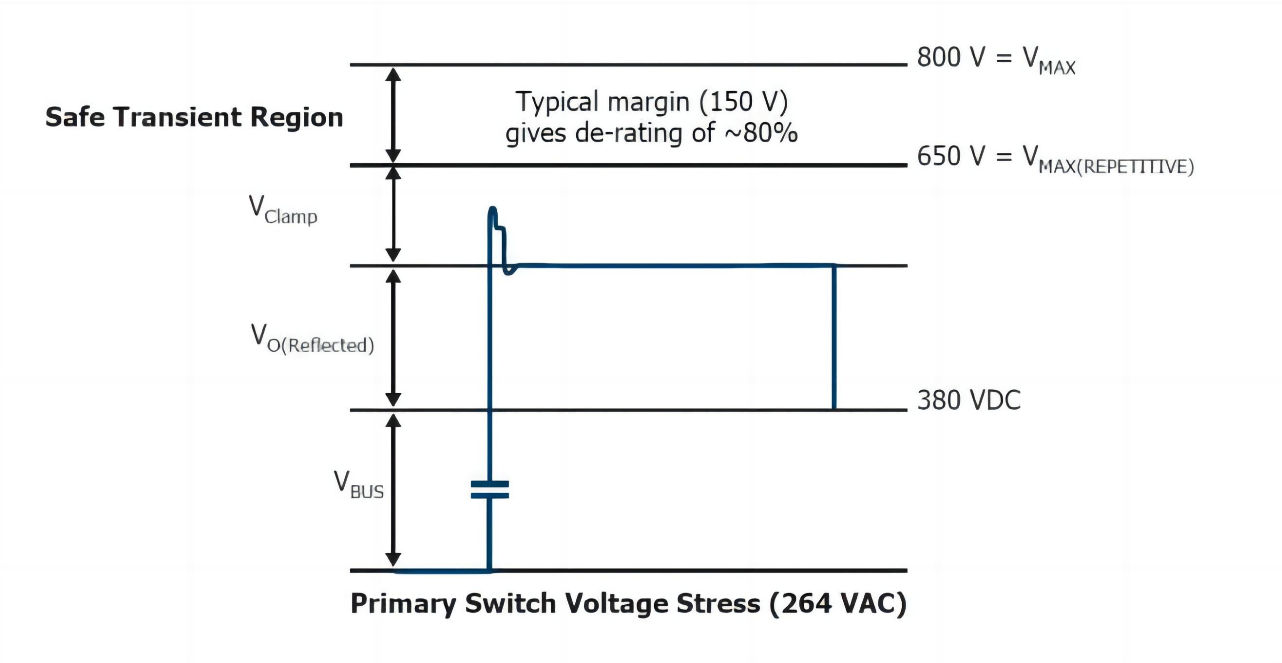
Symbol	Parameter	Test Conditions	Min	Typical	Max	Unit
Reverse Device Characteristics						
IS	Reverse current	VGS=0V, TC=100°C, ≤20% duty cycle	—	—	8.3	A
VSD	Reverse voltage [a]	VGS=0V, IS=10A	—	2.4	—	V
		VGS=0V, IS=5A	—	1.6	—	
tRR	Reverse recovery time	IS=10A, VDD=400V, di/dt=1000A/ms	—	31	—	ns
QRR	Reverse recovery charge		—	40	—	nC

Absolute Maximum Ratings (T_c=25°C unless otherwise stated.)

Symbol	Parameter		Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{DSS\ (TR)}$	Transient drain to source voltage [a]		800	
V_{GSS}	Gate to source voltage		±20	
P_D	Maximum power dissipation @T_C=25°C		52	W
I_D	Continuous drain current @T_C=25°C [b]		13	A
	Continuous drain current @T_C=100°C [b]		8.4	A
I_{DM}	Pulsed drain current (pulse width: 10μs)		60	A
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{SOLD}	Reflow soldering temperature [c]		260	°C

Notes:

a. In off-state, spike duty cycle D<0.01, spike duration <30.00s. Nonrepetitive.
b. For increased stability at high current operation, see Circuit Implementation on page 3
c. Reflow MSL3



Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	2.4	°C/W
$R_{\Theta JA}$	Junction-to-ambient [d]	50	°C/W

Notes:

d. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70μm thickness)

Typical Characteristics

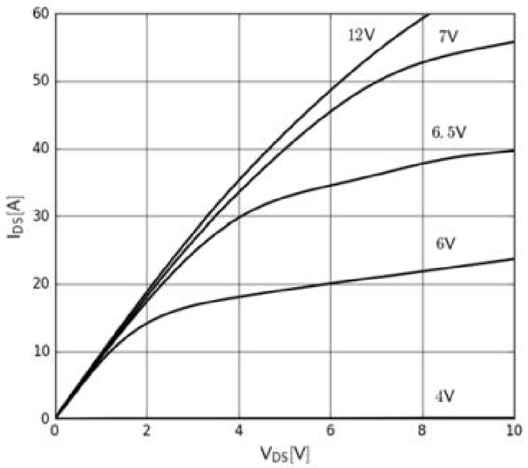


Figure 1. Typical Output Characteristics T_J=25°C
Parameter: V_{GS}

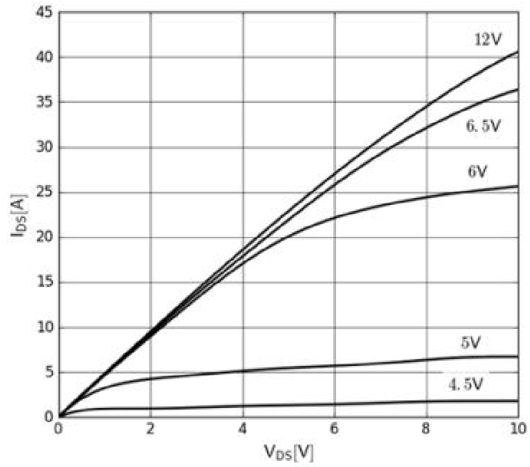


Figure 2. Typical Output Characteristics T_J=150°C
Parameter: V_{GS}

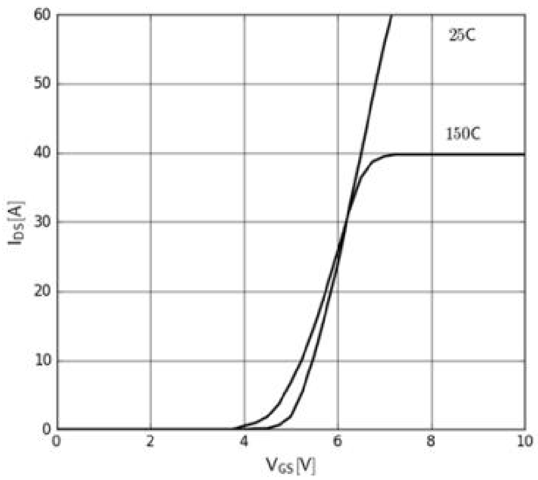


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, parameter: T_J

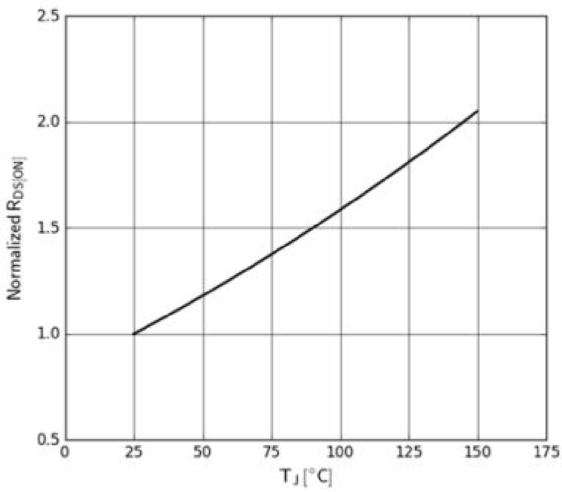


Figure 4. Normalized On-resistance
I_D=16A, V_{GS}=10V

Typical Characteristics

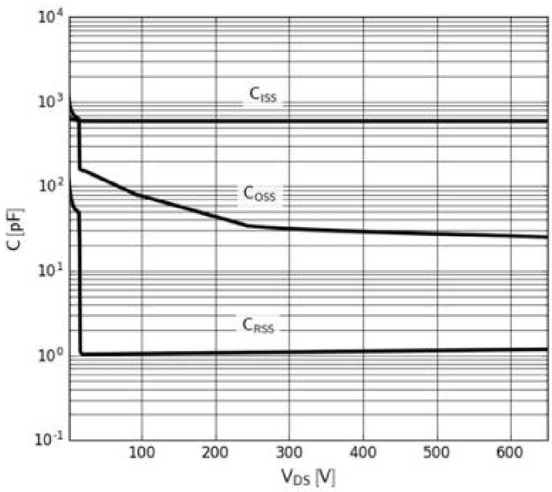


Figure 5. Typical Capacitance

V_{GS}=0V, f=1MHz

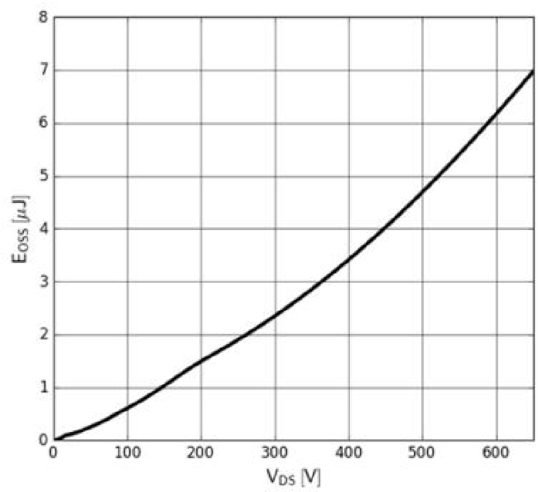


Figure 6. Typical C_{OSS} Stored Energy

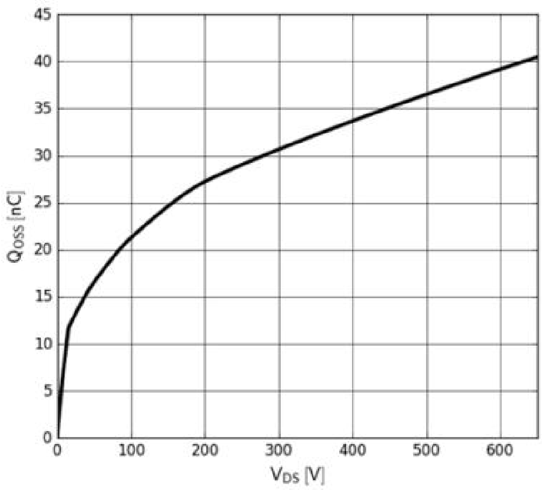


Figure 7. Typical Q_{OSS}

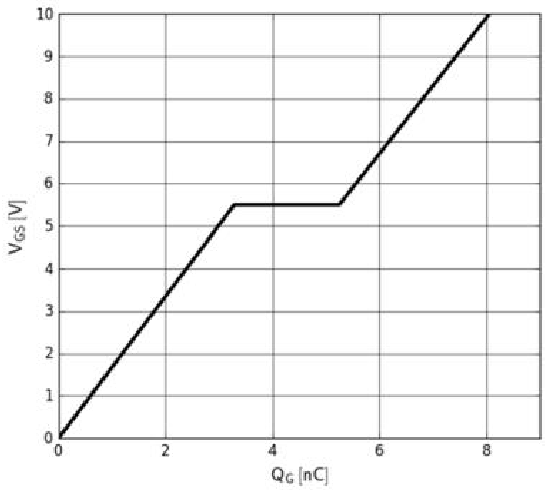


Figure 8. Typical Gate Charge

I_{DS}=10A, V_{DS}=400V

Typical Characteristics

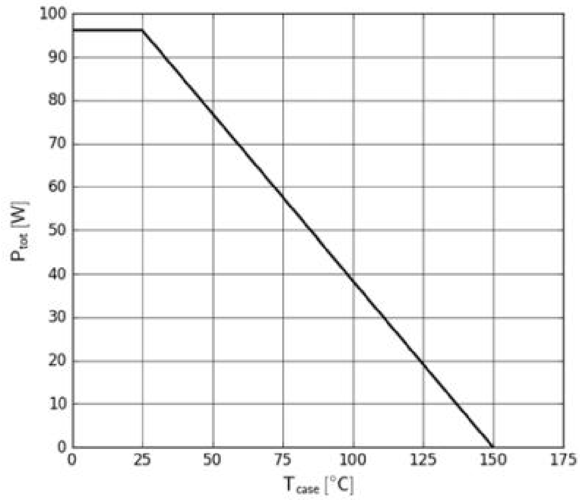


Figure 9. Power Dissipation

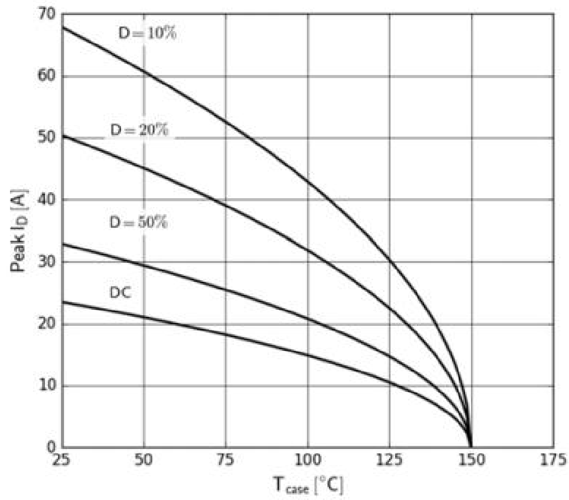


Figure 10. Current Derating

Pulse width ≤ 10μs, V_{GS} ≥ 10V

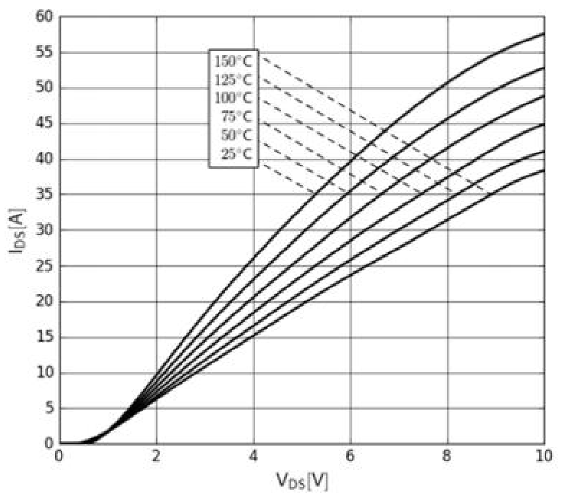


Figure 11. Forward Characteristics of Rev. Diode

I_S=f(V_{SD}), parameter: T_J

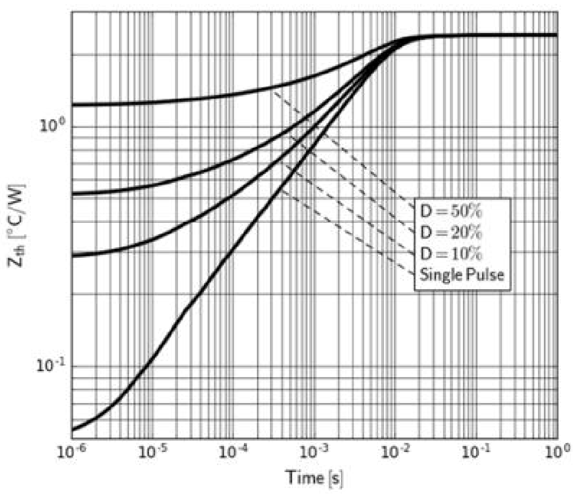


Figure 12. Transient Thermal Resistance

Typical Characteristics

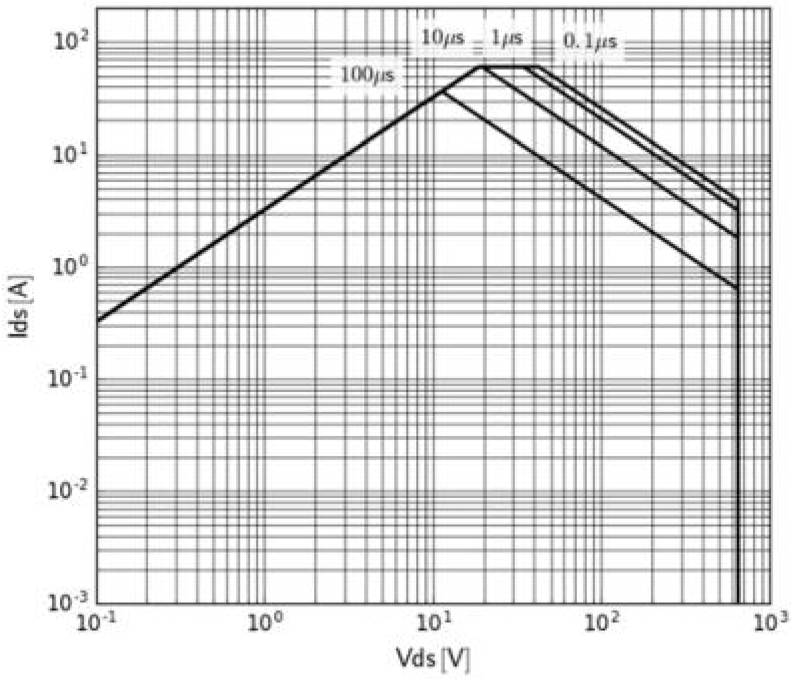


Figure 13. Safe Operating Area T_C=25°C

Test Circuits and Waveforms:

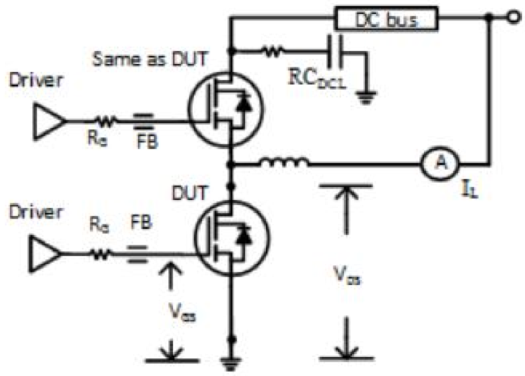


Figure 14. Switching Time Test Circuit
(see circuit implementation on page 3
for methods to ensure clean switching)

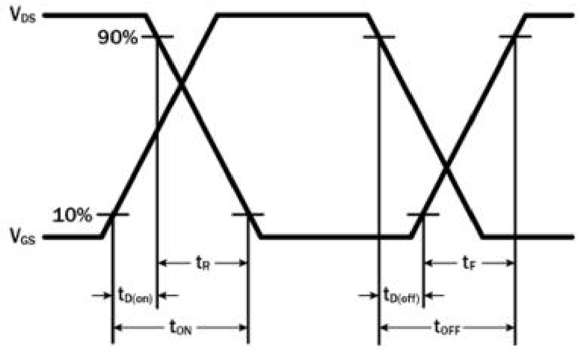


Figure 15. Switching Time Waveform

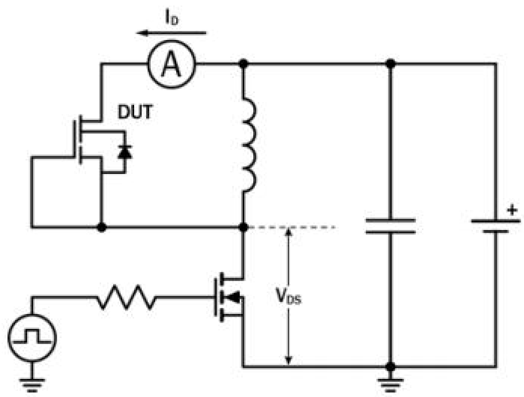


Figure 16. Diode Characteristics Test Circuit

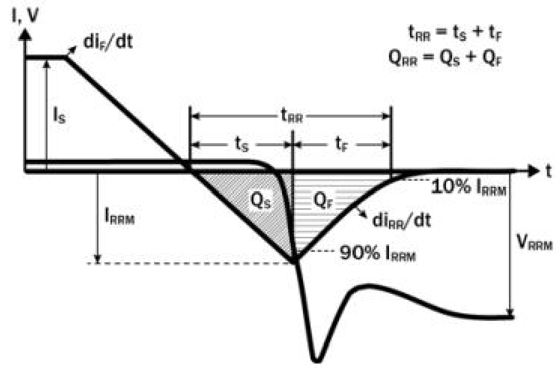


Figure 17. Diode Recovery Waveform

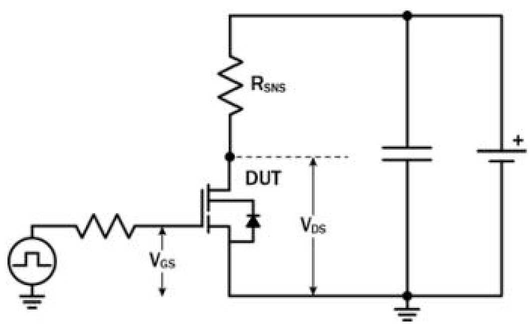


Figure 18. Dynamic RDS(on)eff Test Circuit

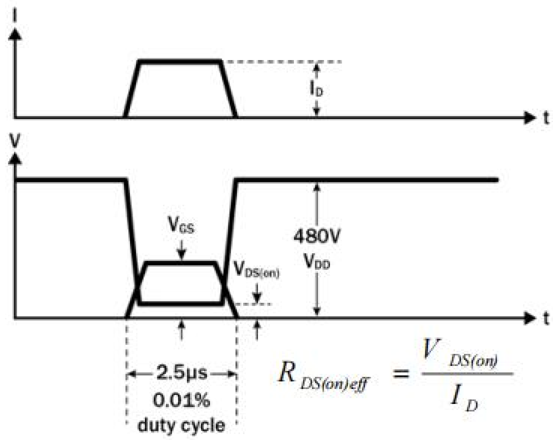
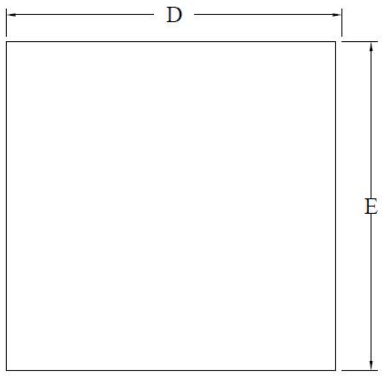


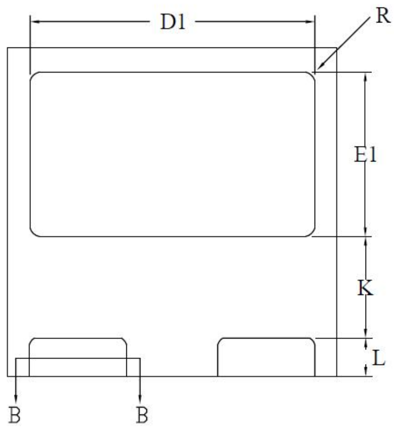
Figure 19. Dynamic RDS(on)eff Waveform

Package Outlines:

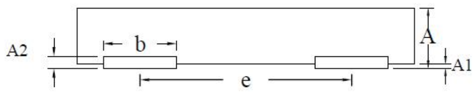
DFN 8X8: (GN3065T)



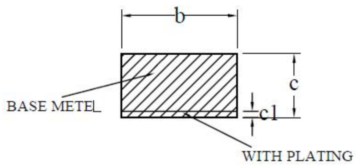
Top View



Bottom View



Side View



SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	1.10	1.15
A1	0.00	——	0.05
A2	——	0.20	0.22
b	2.20	2.25	2.30
c	——	0.20	——
c1	0.01	——	0.02
D	7.90	8.00	8.10
D1	6.85	7.00	7.15
E	7.90	8.00	8.10
E1	4.03	4.18	4.33
e	4.75BSC		
K	2.50	——	——
L	0.70	0.80	0.90
R	——	0.13	——