GaN Power Device

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - Wide gate safety margin
  - Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Product Summary		
V_{DSS}	650	V
$R_{DS(on),typ*}$	480	mΩ
$Q_{G,\ typ}$	9	nC
$Q_{RR,\ typ}$	14	nC

Applications

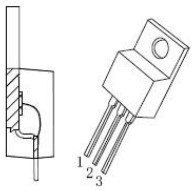
- Consumer
- Power adapters
- Low power SMPS
- Lighting

Main Characteristics

V_{DS}	650 V
$R_{DS(ON)}$	480 mΩ
Current	3.6 A

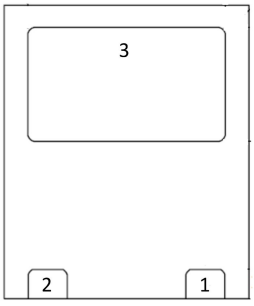
Product Information

(1) TO-220-3L



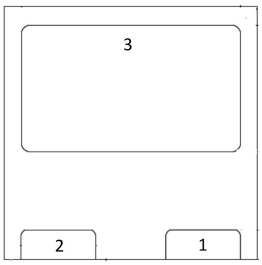
Pin No.	Name	Function
1	G	Gate
2	S	Source
3	D	Drain

(2) DFN 5X6-Dual Punch



Pin No.	Name	Function
1	G	Gate
2	D	Drain
3	S	Source

(3) DFN 8X8



Pin No.	Name	Function
1	G	Gate
2	D	Drain
3	S	Source

Device Information

Part Number	package	packing
GN1065T4ZG	DFN5*6	Tape 4K/reel
GN1065T5ZG	DFN8*8	Tape 3K/reel
GN1065TLG	TO-220	Tape 1K/reel

Absolute Maximum Ratings (T_c = 25°C)

Drain to source voltage (T_J = -55°C to 150°C) ---------- 650 (V)
Transient drain to source voltage [a] ---------- 800(V)
Gate to source voltage ---------- -18~ 18 (V)
Maximum power dissipation @T_C=25°C ---------- -13.2(W)
Continuous drain current @T_C=25°C [b] ---------- 3.6(A)
Continuous drain current @T_C=100°C [b] ---------- 2.3(A)
Pulsed drain current (pulse width: 10μs) ---------- 17(A)
Operating temperature(Case) ---------- -55 to +150(°C)
Operating temperature(Junction) ---------- -55 to +150(°C)
Storage temperature ---------- -55 to +150(°C)
Reflow soldering temperature [c] ---------- 260 (°C)

Electrical Characteristics (T_J = 25°C)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Forward Device Characteristics						
VDSS(BL)	Maximum drain-source voltage	V_{GS}=0V	650	—	—	V
VGS(th)	Gate threshold voltage	V_{DS}=V_{GS}, I_D=0.5mA	1.6	2.2	2.8	V
ΔVGS(th)/TJ	Gate threshold voltage temperature coefficient		—	-5.8	—	mV/°C
RDS(on)eff	Drain-source on-resistance [a]	V_{GS}=8V, I_D=3.4A	—	480	560	mΩ
		V_{GS}=8V, I_D=3.4A, TJ=150°C	—	1000	—	
IDSS	Drain-to-source leakage current	V_{DS}=650V, V_{GS}=0V	—	1	10	μA
		V_{DS}=650V, V_{GS}=0V, TJ=150°C	—	5	—	
IGSS	Gate-to-source forward leakage current	V_{GS}=18V	—	—	100	nA
	Gate-to-source reverse leakage current	V_{GS}=-18V	—	—	-100	
CISS	Input capacitance	V_{GS}=0V, V_{DS}=400V, *f*=1MHz	—	760	—	pF
COSS	Output capacitance		—	9	—	
CRSS	Reverse transfer capacitance		—	1.5	—	
CO(er)	Output capacitance, energy related [b]	V_{GS}=0V, V_{DS}=0V to 400V	—	13	—	pF
CO(tr)	Output capacitance, time related [c]		—	29	—	
QG	Total gate charge	V_{DS}=400V, V_{GS}=0V to 8V, ID=3.4A	—	9	—	nC
QGS	Gate-source charge		—	2.1	—	
QGD	Gate-drain charge		—	2.1	—	
QOSS	Output charge	V_{GS}=0V, V_{DS}=0V to 400V	—	13.5	—	nC
tD(on)	Turn-on delay	V_{DS}=400V, V_{GS}=0V to 8V, I_D=3.4A, RG=30Ω, ZFB=240Ω at 100MHz (See Figure 14)	—	16.6	—	ns
tR	Rise time		—	3.5	—	
tD(off)	Turn-off delay		—	53.2	—	
tF	Fall time		—	7.6	—	

Notes:
a. Dynamic $R_{DS(on)}$ value; see Figures 18 and 19 for conditions
b. Equivalent capacitance to give same stored energy from 0V to 400V
c. Equivalent capacitance to give same charging time from 0V to 400V

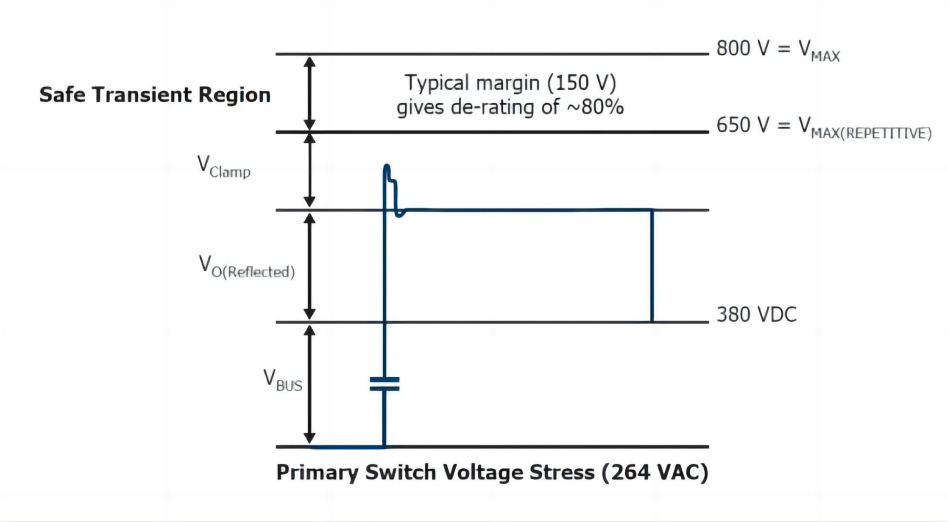
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Reverse Device Characteristics						
IS	Reverse current	V_{GS}=0V, T_C=100°C, ≤25% duty cycle	—	—	2.3	A
VSD	Reverse voltage [a]	V_{GS}=0V, I_S=1.15A	—	1.3	—	V
		V_{GS}=0V, I_S=2.3A	—	1.8	—	
tRR	Reverse recovery time	I_S=3.4A,V_{DD}=400V,	—	14.5	—	ns

Q_{RR}	Reverse recovery charge	di/dt=1000A/us	—	14	—	nC

Maximum ratings, at TC=25 °C, unless otherwise specified

Symbol	Parameter		Limit Value	Unit
VDSS	Drain to source voltage (TJ = -55°C to 150°C)		650	V
VDSS (TR)	Transient drain to source voltage [a]		800	
VGSS	Gate to source voltage		±18	
PD	Maximum power dissipation @TC=25°C		13.2	W
ID	Continuous drain current @TC=25°C [b]		3.6	A
	Continuous drain current @TC=100°C [b]		2.3	A
IDM	Pulsed drain current (pulse width: 10μs)		17	A
TC	Operating temperature	Case	-55 to +150	°C
TJ		Junction	-55 to +150	°C
TS	Storage temperature		-55 to +150	°C
TSOLD	Reflow soldering temperature c		260	°C

Notes:
a. In off-state, spike duty cycle D<0.01, spike duration <30.00s.
b. For increased stability at high current operation, see Circuit Implementation on page 3
c. Reflow MSL3

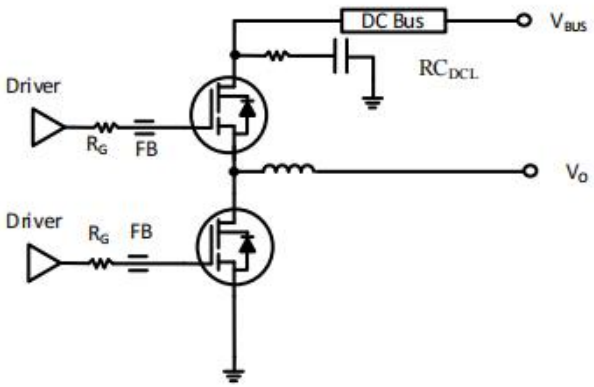


Thermal Resistance

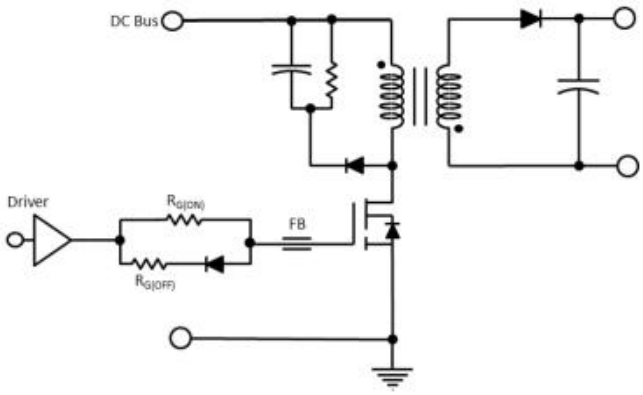
Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	9.5	°C/W
$R_{\Theta JA}$	Junction-to-ambient [d]	50	°C/W

Notes:
d. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm² copper area and 70μm thickness)

Circuit Implementation



Simplified Half-bridge Schematic



Simplified Single Ended Schematic

Recommended gate drive: (0V, 8V) with $R_{G(tot)}$ = 30 Ω[a]

Recommended gate drive: (0V, 12V) with $R_{G(ON)}$ = 100 to 300 Ω
$R_{G(OFF)}$ = 0 to 15 Ω

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber (RC_{DCL})[b]
240Ω @ 100MHz	4.7-10nF + 5Ω

Notes:
a. For bridge topologies only. R_G could be much smaller in single ended topologies.
b. RC_{DCL} should be placed as close as possible to the drain pin.

Typical Characteristics (T_C=25°C unless otherwise stated)

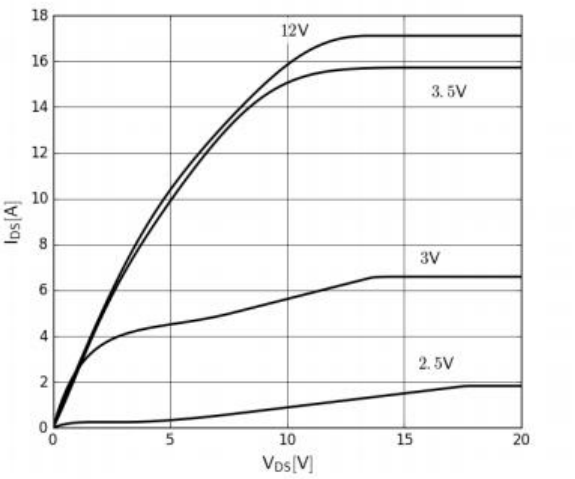


Figure 1. Typical Output Characteristics T_J=25°C
Parameter: V_{GS}

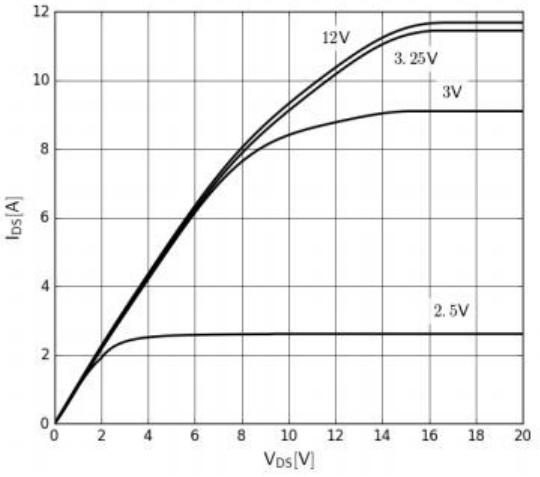


Figure 2. Typical Output Characteristics T_J=150°C
Parameter: V_{GS}

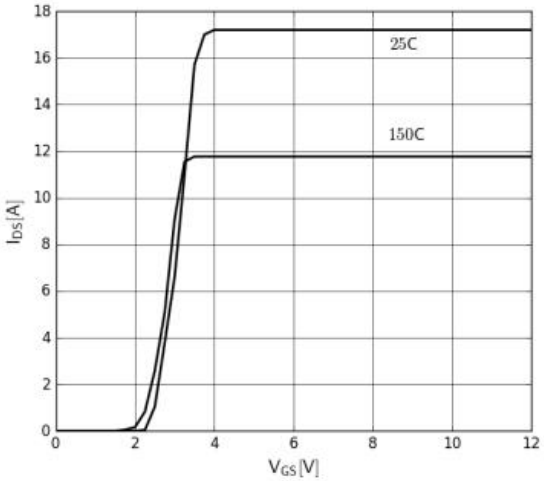


Figure 3. Typical Transfer Characteristics
V_{DS}=20V, parameter: T_J

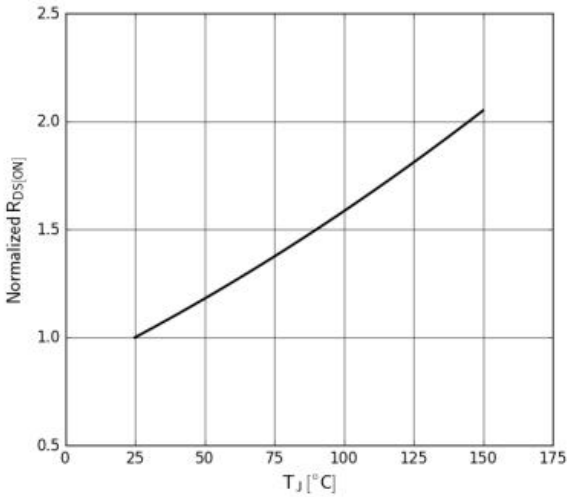


Figure 4. Normalized On-resistance
I_D=16A, V_{GS}=10V

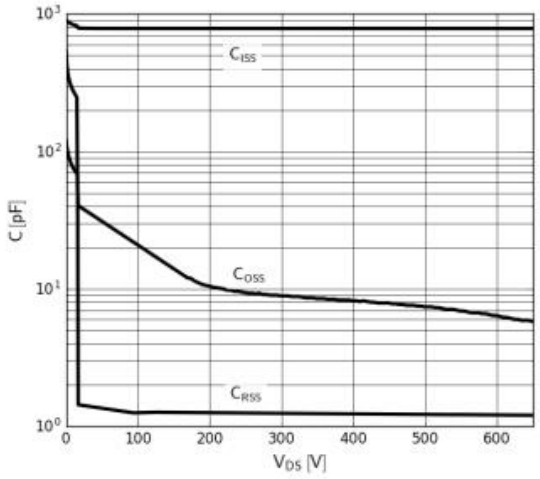


Figure 5. Typical Capacitance
V_{GS}=0V, f=1MHz

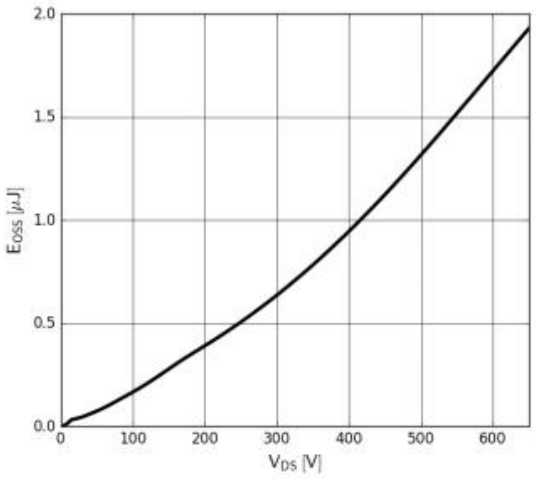


Figure 6. Typical C_{OSS} Stored Energy

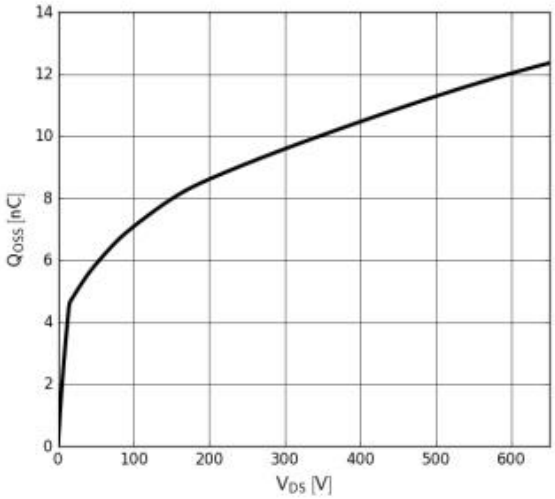


Figure 7. Typical Q_{OSS}

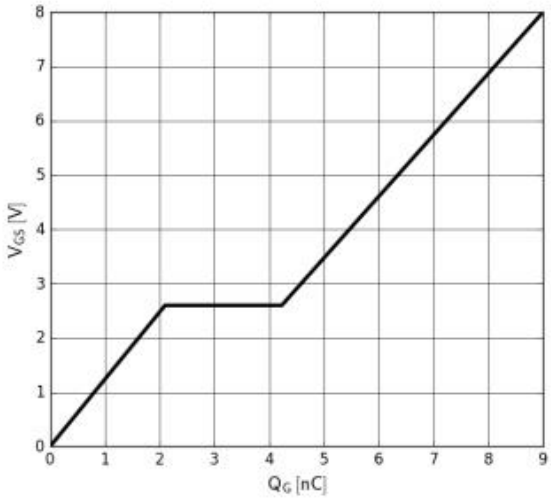


Figure 8. Typical Gate Charge
I_{DS}=3.4A, V_{DS}=400V

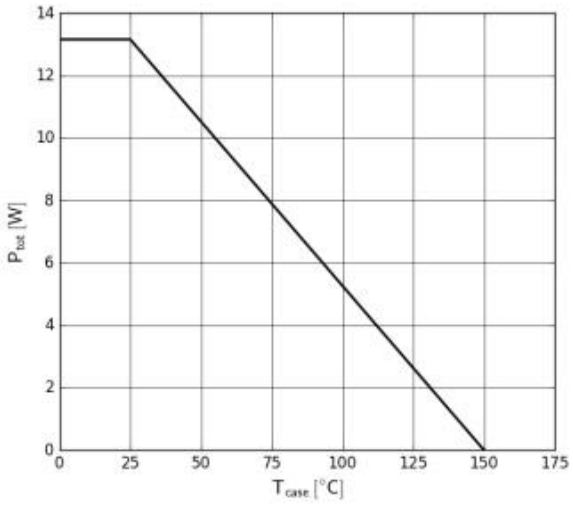


Figure 9. Power Dissipation

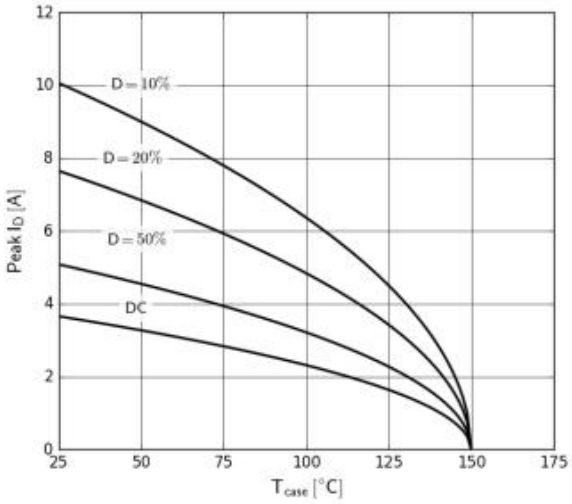


Figure 10. Current Derating
Pulse width ≤ 10µs, V_{GS} ≥ 10V

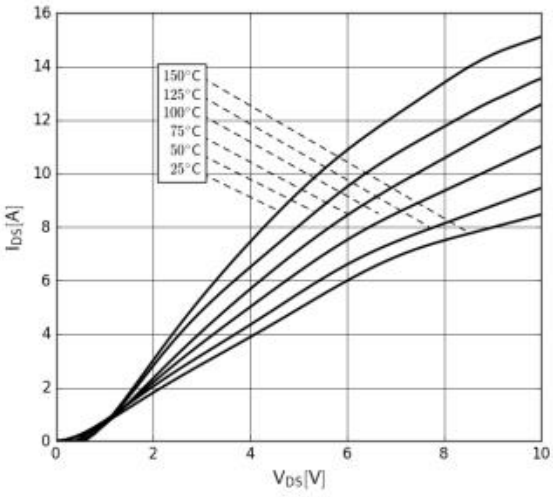


Figure 11. Forward Characteristics of Rev. Diode
I_S=f(V_{SD}), parameter: T_J

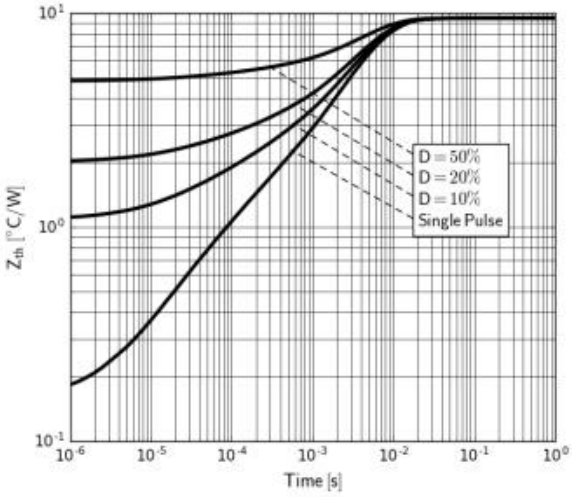


Figure 12. Transient Thermal Resistance

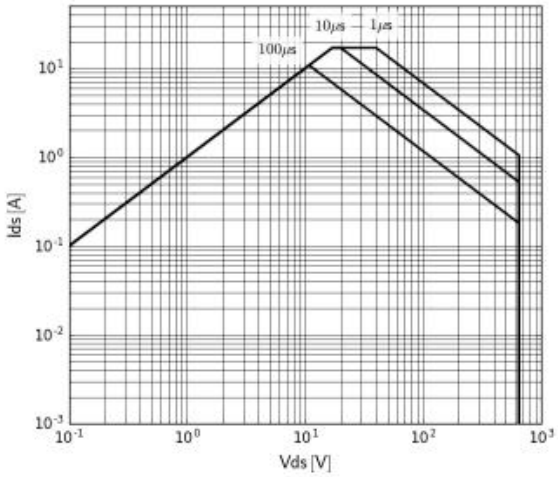


Figure 13. Safe Operating Area T_C=25°C

Test Circuits and Waveforms

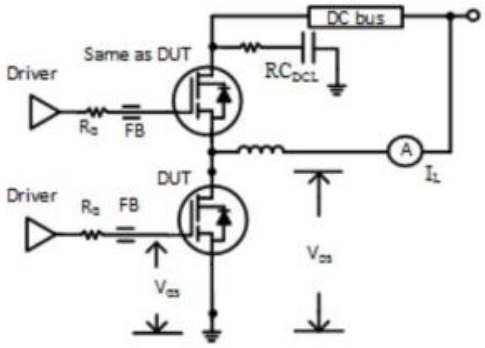


Figure 14. Switching Time Test Circuit
(see circuit implementation on page 3
for methods to ensure clean switching)

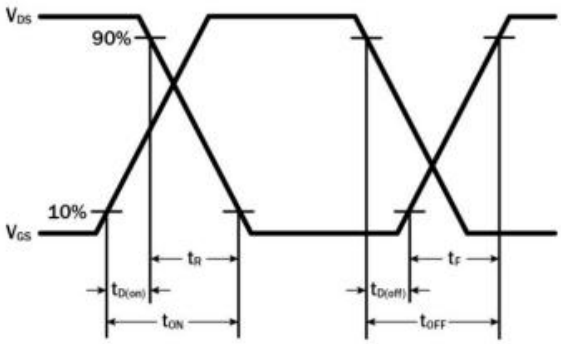


Figure 15. Switching Time Waveform

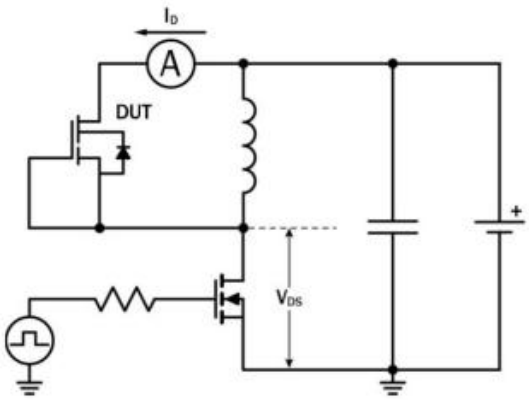


Figure 16. Diode Characteristics Test Circuit

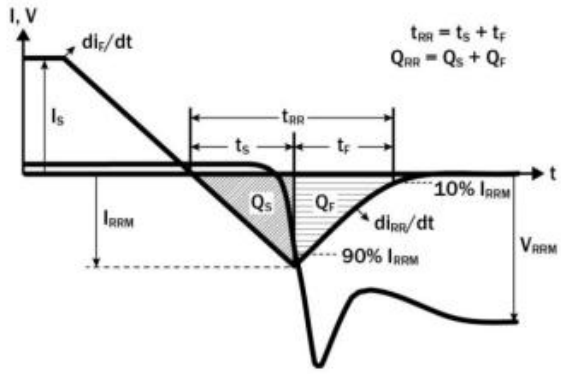


Figure 17. Diode Recovery Waveform

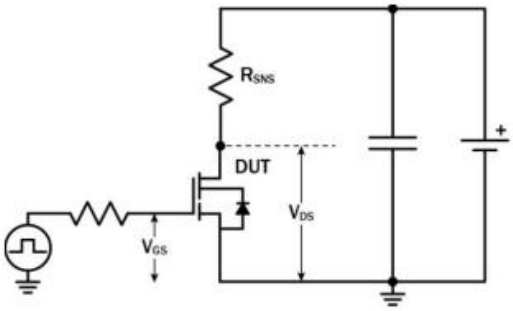


Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit

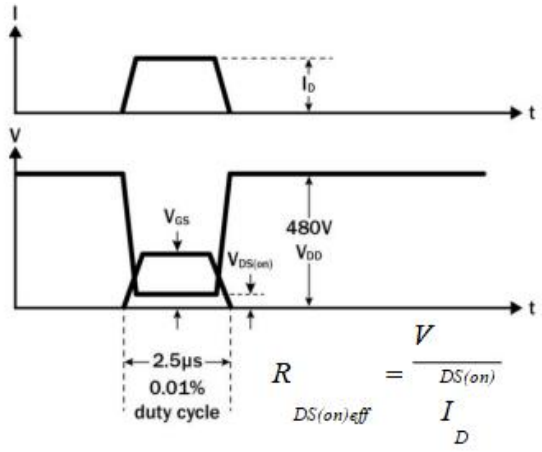
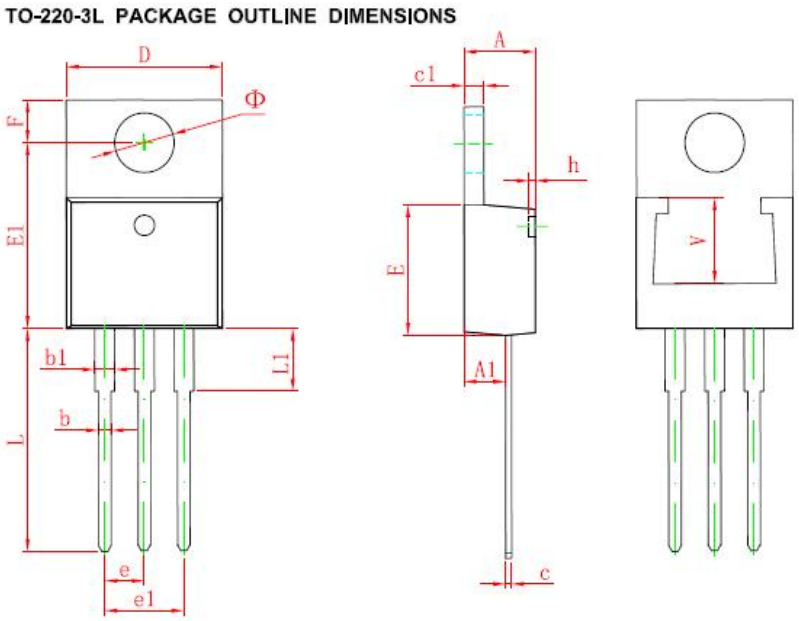


Figure 19. Dynamic $R_{DS(on)eff}$ Waveform

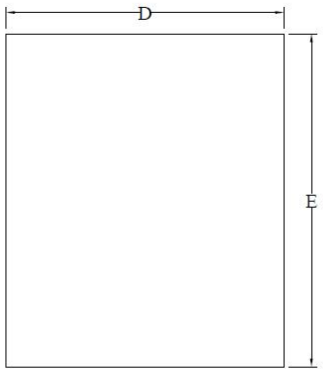
Package Outlines:

(1) TO-220-3L

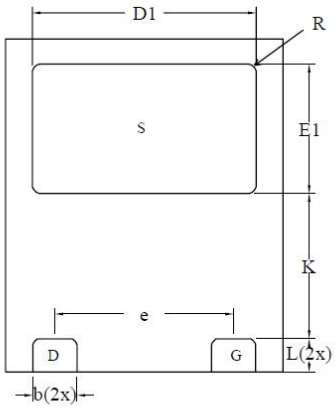


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.470	4.670	0.176	0.184
A1	2.520	2.820	0.099	0.111
b	0.710	0.910	0.028	0.036
b1	1.170	1.370	0.046	0.054
c	0.310	0.530	0.012	0.021
c1	1.170	1.370	0.046	0.054
D	10.010	10.310	0.394	0.406
E	8.500	8.900	0.335	0.350
E1	12.060	12.460	0.475	0.491
e	2.540 TYP.		0.100 TYP.	
e1	4.980	5.180	0.196	0.204
F	2.590	2.890	0.102	0.114
h	0.000	0.300	0.000	0.012
L	13.400	13.800	0.528	0.543
L1	3.560	3.960	0.140	0.156
Φ	3.735	3.935	0.147	0.155
V	5.600 REF.		0.220 REF.	

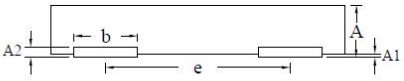
(2) DFN 5X6: (GN1065T)



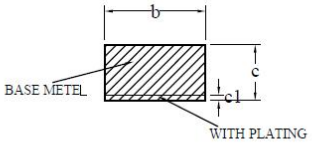
Top View



Bottom View



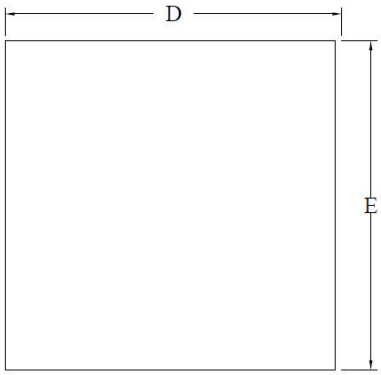
Side View



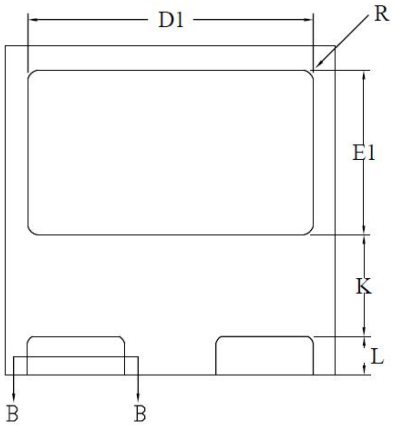
SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	1.10	1.15
A1	0.00	——	0.05
A2	——	0.20	0.22
b	0.82	0.87	0.92
c	——	0.20	——
c1	0.01	——	0.02
D	4.90	5.00	5.10
D1	4.09	4.24	4.39
E	5.90	6.00	6.10
E1	2.15	2.30	2.45
e	3.37BSC		
K	2.50	——	——
L	0.71	0.81	0.91
R	——	0.13	——

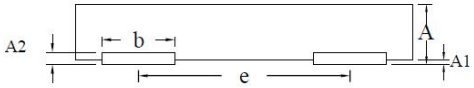
(3) DFN 8X8: (GN1065T)



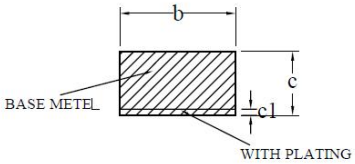
Top View



Bottom View



Side View



SECTION B-B

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	1.10	1.15
A1	0.00	——	0.05
A2	——	0.20	0.22
b	2.20	2.25	2.30
c	——	0.20	——
c1	0.01	——	0.02
D	7.90	8.00	8.10
D1	6.85	7.00	7.15
E	7.90	8.00	8.10
E1	4.03	4.18	4.33
e	4.75BSC		
K	2.50	——	——
L	0.70	0.80	0.90
R	——	0.13	——