HD-LINX™ GS1540
HDTV Serial Digital Non-Equalizing Receiver

DATA SHEET

GS1540

FEATURES

- **SMPTE 292M compliant**
- **1.485 and 1.485/1.001Gb/s operation**
- **integrated adjustment-free reclocker**
- **1:20 serial to parallel conversion**
- **selectable reclocked serial output**
- **reclocker BYPASS capability**
- **LOCK detect**
- **input jitter indicator (IJI)**
- **20 bit output**
- **74.25MHz or 74.25/1.001MHz clock output**
- **Pb-free and Green**
- **single +5.0V power supply**
- **minimal component count for HD SDI receive solutions**

APPLICATIONS

SMPTE 292M Serial Digital Interfaces for Production Switchers, Master Control Switchers, NLE's, and VTR's.

DESCRIPTION

The GS1540 is a high performance integrated Receiver designed for HDTV component signals, conforming to the SMPTE 292M standard. The GS1540 includes adjustment-free clock and data recovery, and 1:20 serial to parallel conversion.

The Clock and Data Recovery stage was designed to automatically recover the embedded clock signal and re-time the data from SMPTE 292M compliant digital video signals. There is also a selectable reclocked serial data buffer output and the ability to bypass the reclocker stage.

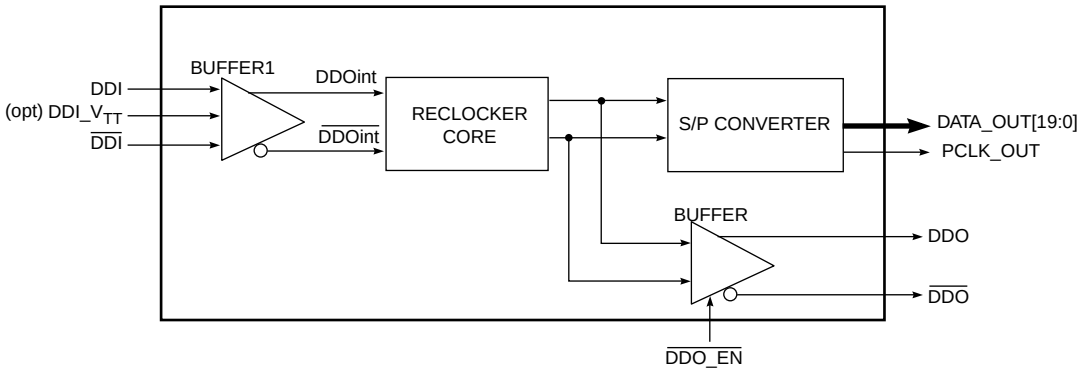
A unique feature, Input Jitter Indicator (IJI), is included for robust system design. This feature is used to indicate excessive input jitter before the chip mutes the outputs.

The Serial to Parallel conversion stage provides 1:20 S/P conversion.

The GS1540 uses the GO1515 external VCO connected to the internal PLL circuitry to achieve ultra low noise PLL performance.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE	Pb-FREE AND GREEN
GS1540-CQR	128 pin MQFP	0°C to 70°C	No
GS1540-CQRE3	128 pin MQFP	0°C to 70°C	Yes



SIMPLIFIED BLOCK DIAGRAM

GENNUM CORPORATION P.O. Box 489, Stn. A, Burlington, Ontario, Canada L7R 3Y3
Tel. +1 (905) 632-2996 Fax. +1 (905) 632-5946 E-mail: info@gennum.com
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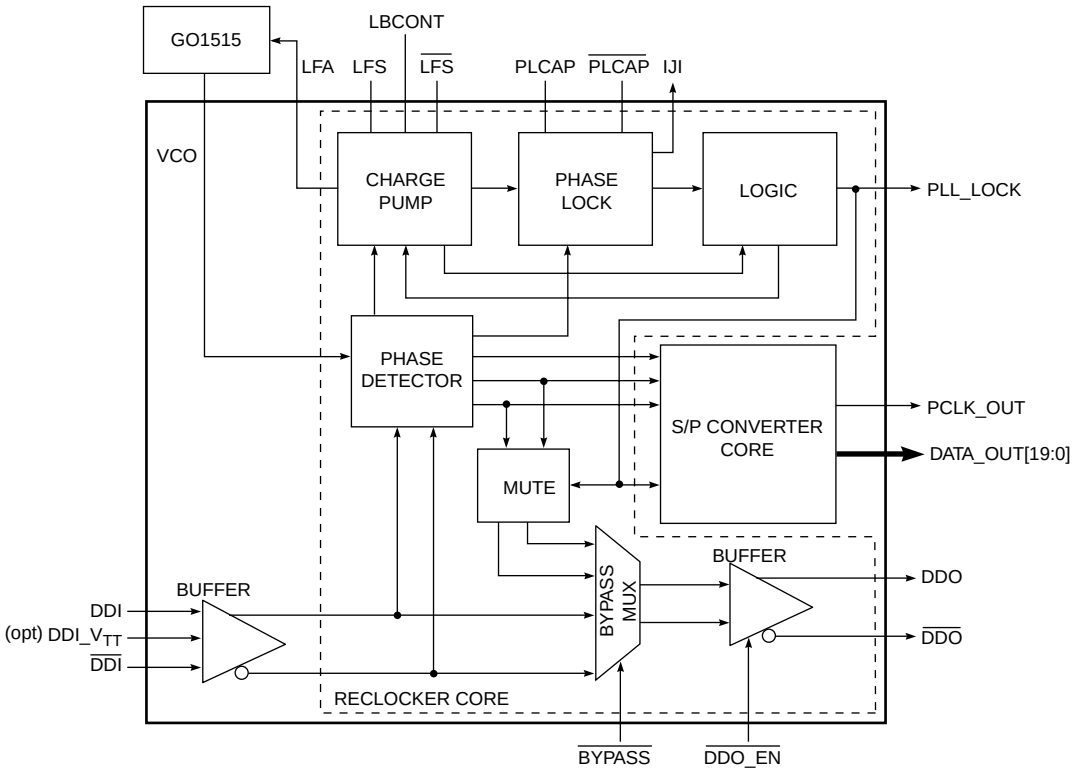


FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise indicated.

PARAMETER	VALUE
Supply Voltage (V_S)	5.5V
Input Voltage Range (any input)	V_{EE} – 0.5 < V_{IN} < V_{CC}+ 0.5
Operating Temperature Range	0°C ≤ T_A ≤ 70°C
Storage Temperature Range	-40°C ≤ T_S ≤ 150°C
Power Dissipation (V_{CC} = 5.25V)	1.85W
Lead Temperature (soldering 10 seconds)	260°C
Input ESD Voltage	1000V
Junction Temperature	125°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V, V_{EE} = 0V, T_A = 0°C to 70°C unless otherwise shown, Data Rate = 1.485Gb/s.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	TEST LEVEL
Positive Supply Voltage	Operating range	V_{CC}	4.75	5.00	5.25	V	3
Power Consumption	V_{CC} = 5; T_A = 25°c	P_D	-	1050	-	mW	5
Supply Current	V_{CC} = 5	I_S	-	180	-	mA	1
Output CM Voltage (DDO, $\overline{DDO}$)		V_{CM}	3.4	3.9	4.30	V	5
Input DC Voltage (DDI, $\overline{DDI}$)	internal bias voltage		3.7	4.0	4.2	V	1
Serial Inputs (DDI, $\overline{DDI}$)	Differential mode T_A = 25°C	V_{SID}	100	-	800	mV	3
	Common mode T_A = 25°C	V_{CM}	2.5+$V_{SID/2}$	-	V_{CC}-$V_{SID/2}$	V	3
High Level Input Voltage ($\overline{BYPASS}$)	V_{CC} = 5, T_A = 25°C	V_{IH}	2.0	-	-	V	3
Low Level Input Voltage ($\overline{BYPASS}$)	V_{CC} = 5, T_A = 25°C	V_{IL}	-	-	0.8	V	3
High Level Output Voltage (D[19:0], PCLK)	V_{CC} = 5, I_{SOURCE} =1.0mA	V_{OH}	2.4	-	3.0	V	1
Low Level Output Voltage (D[19:0], PCLK)	V_{CC} = 5, I_{SINK} = 1.0mA	V_{OL}	-	-	0.4	V	1
High Level Output Voltage (PLL_LOCK)	V_{CC} = 5, I_{SOURCE} = 200µA	V_{OH}	2.4	3.0	-	V	1
Low Level Output Voltage (PLL_LOCK)	V_{CC} = 5, I_{SINK} = 500µA	V_{OL}	-	-	0.4	V	1

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

AC ELECTRICAL CHARACTERISTICS - RECLOCKER STAGE

V_{CC} = 5V, T_A = 25°C

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	TEST LEVEL
Serial Input – Data Rate	SMPTE 292M	BR_{SDI}	1.485/1.001	1.485	-	Gb/s	3
Serial Input – Jitter Tolerance	Sinewave Modulation (p – p)	J_{TOL}	-	0.6	-	UI	9
Phase Lock Time - Asynchronous	Loop bandwidth approximately 1.4MHz @ 0.2 UI input jitter modulation (LBCONT floating).	T_{ALOCK}	-	120	145	ms	7
Phase Lock Time - Synchronous	Loop bandwidth approximately 1.4MHz @ 0.2 UI input jitter modulation (LBCONT floating).	T_{SLOCK}	-	2	3.2	µs	7
Carrier Detect Time	Loop bandwidth approximately 1.4MHz @ 0.2 UI input jitter modulation (LBCONT floating).		-	12	14	ms	7
Phase Lock/Unlock Time (1nF PLCAP)	Loop bandwidth approximately 1.4MHz @ 0.2 UI input jitter modulation (LBCONT floating).		80	-	-	µs	7
Digital Data Output (DDO) – Signal Swing		V_{DDO}	355	400	480	mV	1
Digital Data Output (DDO) - Rise and Fall Time		$t_{R\text{-}DDO}$, $t_{F\text{-}DDO}$	-	160	-	ps	7
Digital Data Output (DDO) – Rise and Fall Time Mismatch			-	30	-	ps	7
Digital Data Output (DDO) – Intrinsic Jitter	(RMS Jitter for clean PRN 2^{23} – 1 input on DDI/$\overline{DDI}$ inputs)	t_{IJ}	-	10	-	ps	9
Loop bandwidth	@ 0.2UI jitter modulation LBCONT floating	1.2	1.4	1.5	-	MHz	7
Jitter peaking			-	-	0.1	dB	7

AC ELECTRICAL CHARACTERISTICS - SERIAL TO PARALLEL STAGE

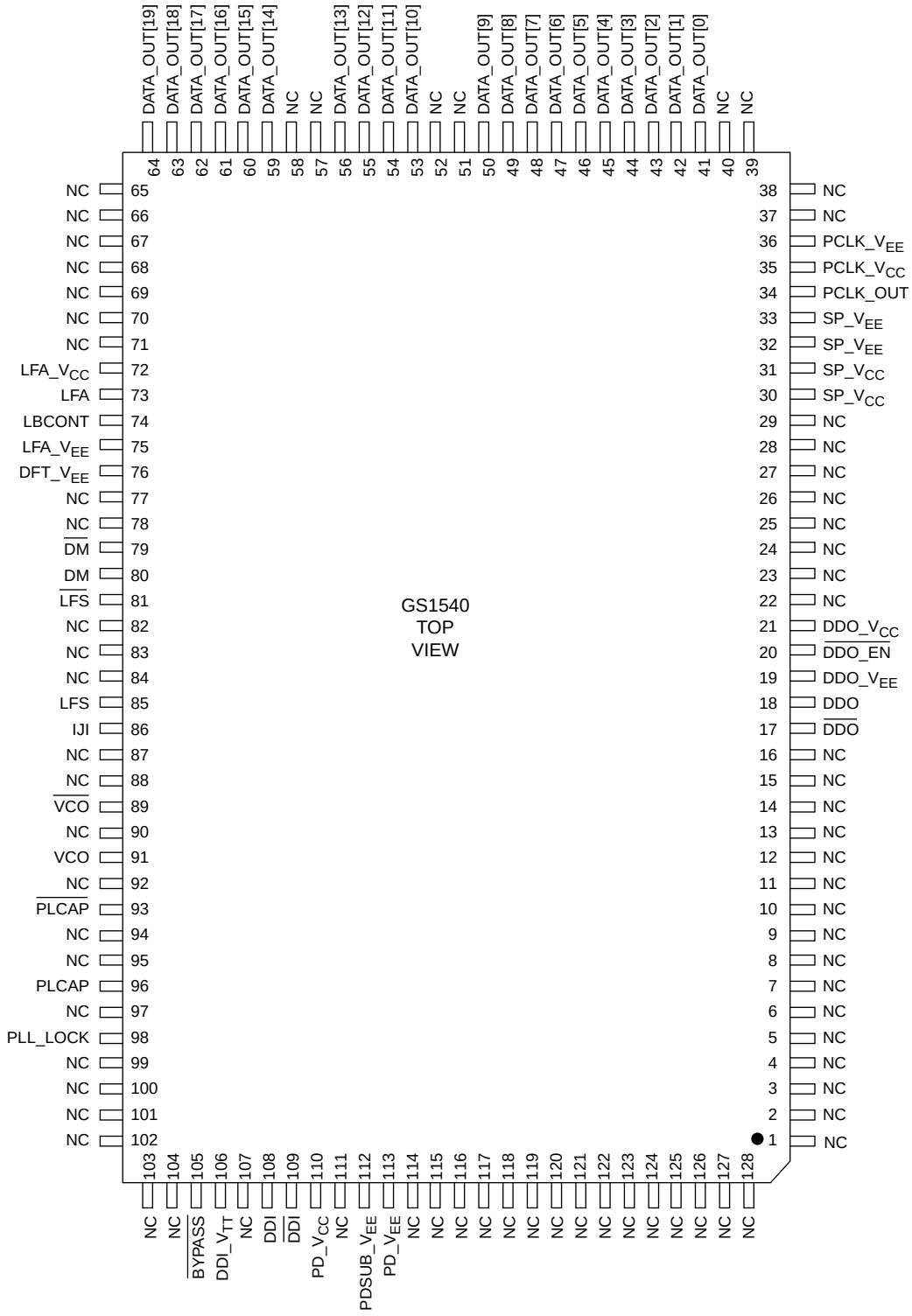
V_{CC} = 5V, T_A = 25°C

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	TEST LEVEL
Parallel Output Clock Frequency	SMPTE 292M	P_{CLK_OUT}	74.25/1.001	74.25	-	MHz	3
Clock Pulse Width Low	15pF load	t_{PWL}	7	-	6.1	ns	7
Clock Pulse Width High	15pF load	t_{PWH}	6	-	6.4	ns	7
Output signal Rise/Fall time	15pF load	t_r, t_f	-	2.70	3.60	ns	7
Output Signal Rise/Fall Time Matching	15pF load	t_{rfm}	-	1.00	1.60	ns	7
Output Setup Time	15pF load	t_{OD}	5	5.5	-	ns	7
Output Hold Time	15pF load	t_{OH}	6.2	7.1	-	ns	7

TEST LEVELS

1. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges.
2. Production test at room temperature and nominal supply voltage with guardbands for supply and temperature ranges using correlated test.
3. Production test at room temperature and nominal supply voltage.
4. QA sample test.
5. Calculated result based on Level 1,2, or 3.
6. Not tested. Guaranteed by design simulations.
7. Not tested. Based on characterization of nominal parts.
8. Not tested. Based on existing design/characterization data of similar product.
9. Indirect test.

PIN CONNECTIONS



PIN DESCRIPTIONS

NUMBER	SYMBOL	LEVEL	TYPE	DESCRIPTION
1, 2, 3, 4, 6, 5, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 22, 23, 24, 25, 26, 27, 28, 29, 37, 38, 39, 40, 51, 52, 57, 58, 65, 66, 67, 68, 69, 70, 71, 77, 78, 82, 83, 84, 87, 88, 90, 92, 94, 95, 97, 99, 100, 101, 102, 103, 104, 107, 111, 114, 115, 116, 117, 118, 119, 120, 121, 122, 123, 124, 125, 126, 127, 128	NC			No Connect. Leave these pins floating.
17, 18	DDO, $\overline{\text{DDO}}$	ECL/PECL compatible	Output	Digital Data Output. Differential serial outputs. 50Ω pull up resistors are included on chip. Note that these outputs are not cable drivers. Ensure that the trace length between the GS1540 and the GS1508 Cable driver is kept to a minimum and that a PCB trace characteristic impedance of 50Ω is maintained between the GS1508 and the GS1540. 50Ω end termination is recommended.
19	DDO_V_{EE}	Power	Input	Negative Supply. Most negative power supply connection for serial data output stage.
20	$\overline{\text{DDO\_EN}}$	Power	Input	Control Signal Input. Used to enable or disable the serial output stage. If a loop through function is not required, then this pin should be tied to the most positive power supply voltage. When $\overline{\text{DDO\_EN}}$ is tied to the most negative power supply voltage, the DDO, $\overline{\text{DDO}}$ outputs are enabled. When $\overline{\text{DDO\_EN}}$ is tied to the most positive power supply voltage, the DDO, $\overline{\text{DDO}}$ outputs are disabled.
21	DDO_V_{CC}	Power	Input	Positive Supply. Most positive power supply connection for serial data output stage.
30, 31	SP_V_{CC}	Power	Input	Positive Supply. Most positive power supply connection for serial to parallel converter stage.
32, 33	SP_V_{EE}	Power	Input	Negative Supply. Most negative power supply connection for the parallel output stage.
34	PCLK_OUT	TTL	Output	Output Clock. The device uses PCLK_OUT for clocking the output data stream from DATA_OUT[19:0]. This clock is also used to clock the data into the GS1500 HDTV Deformatter, or GS1510 HDTV Deformatter.
35	PCLK_V_{CC}	Power	Input	Positive Supply. Most positive supply connection for parallel clock output stage.
36	PCLK_V_{EE}	Power	Input	Negative Supply. Most negative power supply connection for parallel clock output stage.
41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 53, 54, 55, 56, 59, 60, 61, 62, 63, 64	DATA_OUT[19:0]	TTL	Output	Parallel Data Output Bus. The device outputs a 20 bit parallel data stream running at 74.25 or 74.25/1.001MHz on DATA_OUT[19:0]. DATA_OUT[19] is the MSB and DATA_OUT[0] is the LSB.

PIN DESCRIPTIONS (Continued)

NUMBER	SYMBOL	LEVEL	TYPE	DESCRIPTION
72	LFA_V_{CC}	Power	Input	**Positive Supply**. Loop filter most positive power supply connection.
73	LFA	Analog	Output	**Control Signal Output.** Control voltage for GO1515 VCO.
74	LBCONT	Analog	Input	**Control Signal Input**. Used to provide electronic control of Loop Bandwidth.
75	LFA_V_{EE}	Power	Input	**Negative Supply**. Loop filter most negative power supply connection.
76	DFT_V_{EE}	Power	Input	Most negative power supply connection - enables the jitter demodulator functionality. This pin should be connected to ground. If left floating, the DM function is disabled resulting in a current saving of 340µA.
79, 80	DM, $\overline{DM}$	Analog	Output	**Test Signal**. Used for manufacturing test only. These pins must be floating for normal operation.
81, 85	LFS, $\overline{LFS}$	Analog	Input	**Loop Filter Connections**.
86	IJI	Analog	Output	**Status Signal Output**. Approximates the amount of excessive jitter on the incoming DDI and $\overline{DDI}$ input.
89	$\overline{VCO}$	Analog	Input	**Control Signal Input**. Input pin is AC coupled to ground using a 50Ω transmission line.
91	VCO	Analog	Input	**Control Signal Input.** Voltage controlled oscillator input. This pin is connected to the output pin of the GO1515 VCO. This pin must be connected to the GO1515 VCO output pin via a 50Ω transmission line.
93, 96	PLCAP, $\overline{PLCAP}$	Analog	Input	**Control Signal Input**. Phase lock detect time constant capacitor.
98	PLL_LOCK	TTL	Output	**Status Indicator Signal**. This signal is a combination (logical AND) of the carrier detect and phase lock signals. When input is present and PLL is locked, the PLL_LOCK goes high and the outputs are valid. When the PLL_LOCK output is low the data output is muted (latched at the last state). PLL_LOCK is independent of the $\overline{BYPASS}$ signal.
105	$\overline{BYPASS}$	TTL	Input	**Control Signal Input**. Selectable input that controls whether the input signal is reclocked or passed through the chip. When $\overline{BYPASS}$ is high; the input signal is reclocked. When $\overline{BYPASS}$ is low; the input signal is passed through the chip and not reclocked. Muting does not effect bypassed signal.
106	DDI_V_{TT}	Analog	Input	**Bias Input.** Selectable input for interfacing standard ECL outputs requiring 50Ω pull down to V_{TT} power supply for a seamless interface. *See Typical Application Circuit for recommended circuit application.*
108, 109	DDI, $\overline{DDI}$	Differential ECL/PECL	Input	**Digital Data Input Signals.** Digital input signals from a GS1504 Equalizer or HD crosspoint switch. Because of on chip 50Ω termination resistors, a PCB trace characteristic impedance of 50Ω is recommended.
110	PD_V_{CC}	Power		**Positive Supply**. Phase detector most positive power supply connection.
112	PDSUB_V_{EE}	Power	Input	**Substrate Connection**. Connect to phase detector's most negative power supply.
113	PD_V_{EE}	Power	Input	**Negative Supply.** Phase detector most negative power supply connection.

INPUT/OUTPUT CIRCUITS

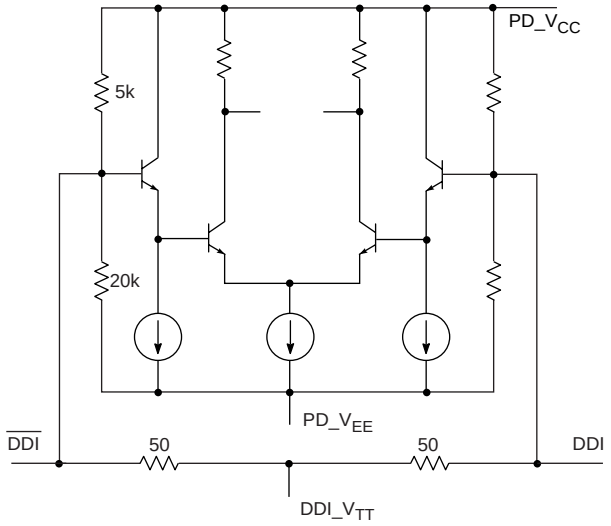


Fig. 1 DDI/$\overline{\text{DDI}}$ Input Circuit

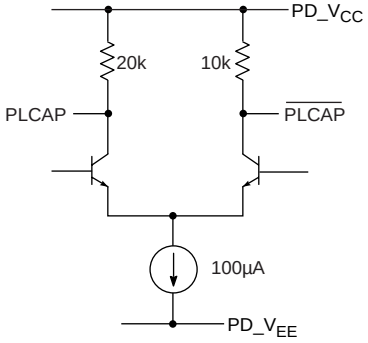


Fig. 4 PLCAP/$\overline{\text{PLCAP}}$ Output Circuit

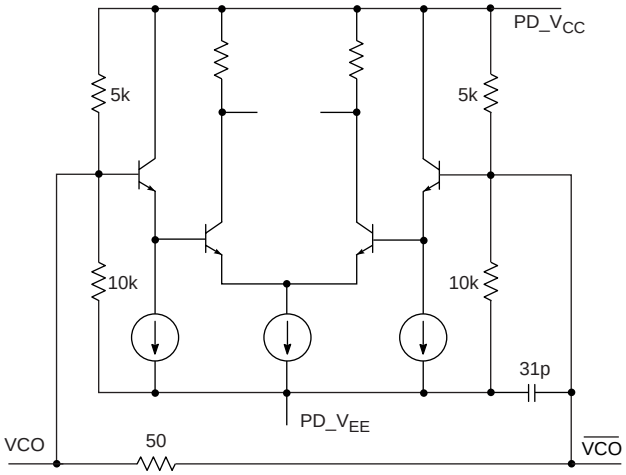


Fig. 2 VCO/$\overline{\text{VCO}}$ Input Circuit

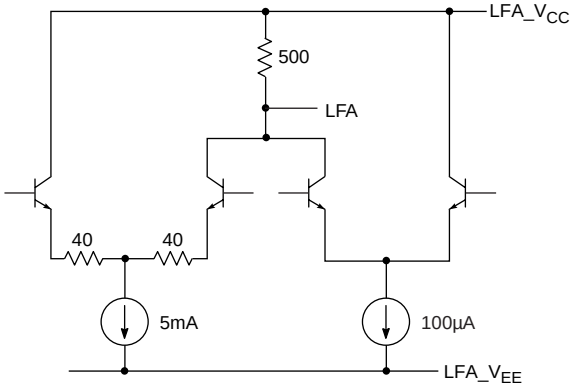


Fig. 5 LFA Circuit

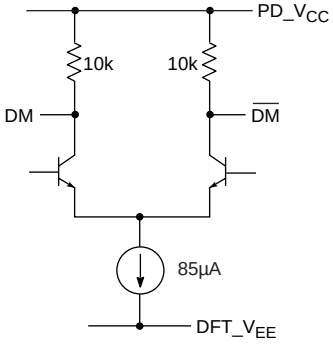


Fig. 3 DM/$\overline{\text{DM}}$ Output Circuit

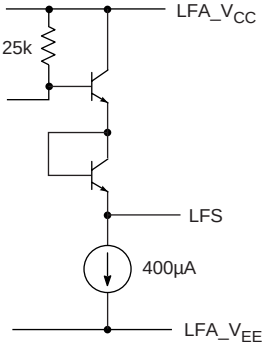


Fig. 6 LFS Output Circuit

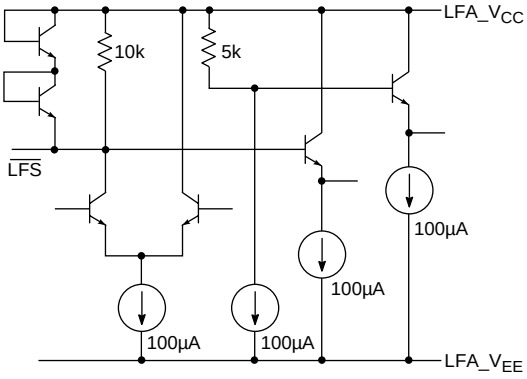


Fig. 7 $\overline{\text{LFS}}$ Input Circuit

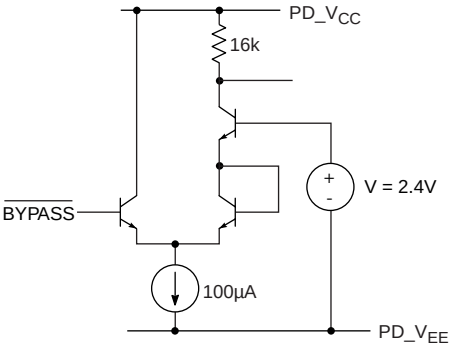


Fig. 10 $\overline{\text{BYPASS}}$ Circuit

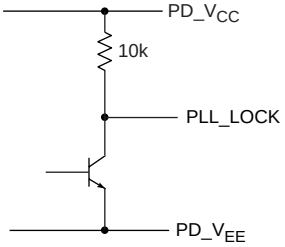


Fig. 8 PLL_LOCK Output Circuit

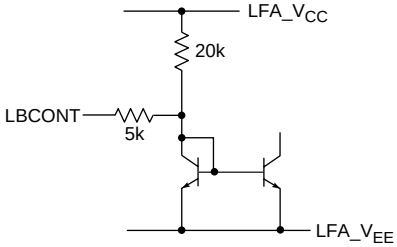


Fig. 11 LBCONT Circuit

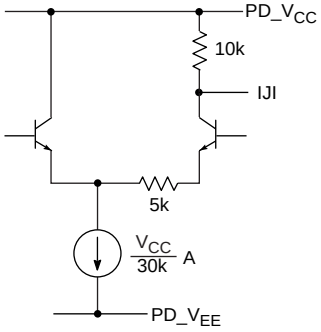


Fig. 9 IJI Output Circuit

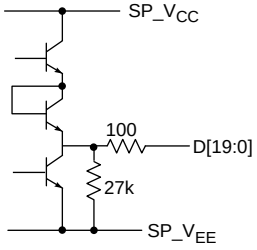


Fig. 12 D[19:0] Output Circuit

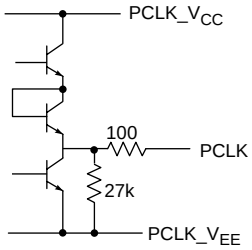


Fig. 13 PCLK Output Circuit

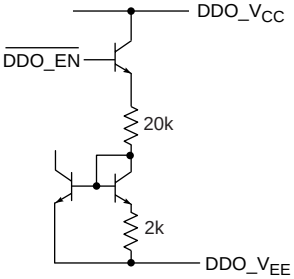


Fig. 14 $\overline{\text{DDO\_EN}}$ Circuit

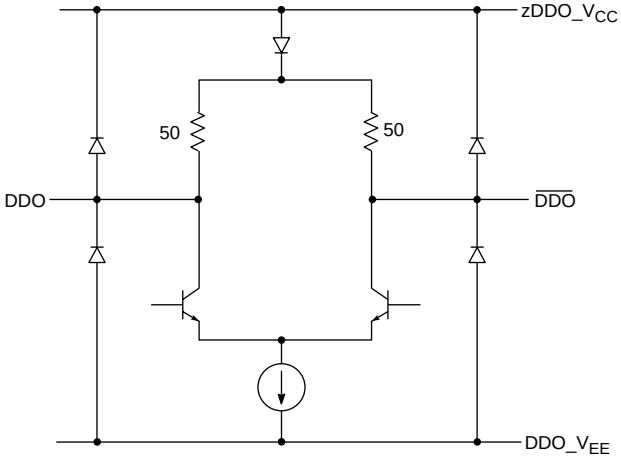


Fig. 15 Serial (DDO) Output Stage Circuit

DETAILED DESCRIPTION

The GS1540 is a single standard receiver for serial digital HDTV signals at 1.485Gb/s and 1.485/1.001Gb/s.

UNIQUE SLEW PHASE LOCK LOOP (S-PLL):

A unique feature of the GS1540 is the innovative slew phase lock loop (S-PLL). When a step phase change is applied to the PLL, the output phase gains constant rate of change with respect to time. This behaviour is termed slew. Figure 16 shows an example of input and output phase variation over time for slew and linear (conventional) PLLs. Since the slewing is a nonlinear behavior, the small signal analysis cannot be done in the same way as the standard PLL. However, it is still possible to plot input jitter transfer characteristics at a constant input jitter modulation.

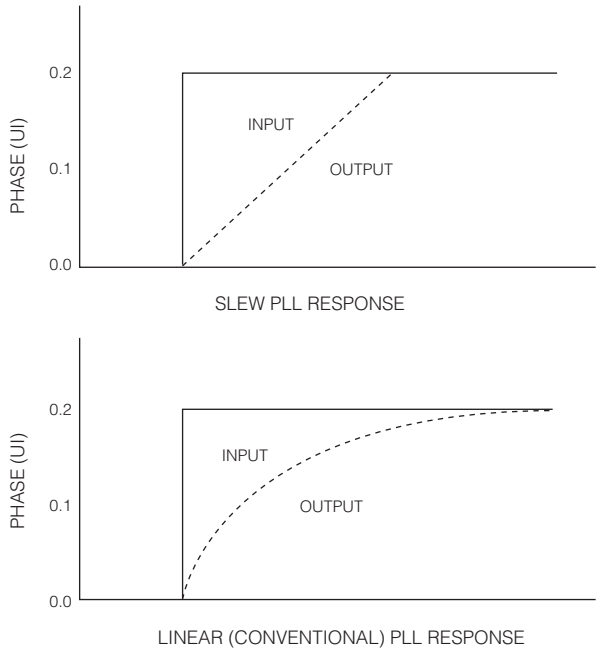


Fig. 16 PLL Characteristics

Slew PLLs offer several advantages such as excellent noise immunity. Because of the infinite bandwidth for an infinitely small input jitter modulation (or jitter introduced by VCO), the loop corrects for that immediately thus the small signal noise of the VCO is cancelled. The GS1540 uses a very clean, external VCO called the GO1515 (*refer to the GO1515 Data Sheet for details*). In addition, the bi-level digital phase detector provides constant loop bandwidth that is predominantly independent of the data transition density. The loop bandwidth of a conventional tri-stable charge pump drops with reducing data transitions. During pathological signals, the data transition density reduces from 0.5 to 0.05, but the slew PLL's performance essentially remains unchanged.

Because most of the PLL circuitry is digital, it is more like other digital systems which are generally more robust than their analog counterparts. Additionally, signals like DM/$\overline{DM}$ which represent the internal functionality can be generated without adding additional artifacts. Thus, system debugging is also possible with these features. The complete slew PLL is made up of several blocks including the phase detector, the charge pump and an external Voltage Controlled Oscillator (VCO).

DIGITAL INPUT BUFFER

The input buffer is a self-biased circuit. On-chip 50Ω termination resistors provide a seamless interface for other HD-LINX™ products such as the GS1504 Adaptive Cable Equalizer.

PHASE DETECTOR

The phase detector portion of the slew PLL used in the GS1540 is a bi-level digital phase detector. It indicates whether the data transition occurred before or after with respect to the falling edge of the internal clock. When the phase detector is locked, the data transition edges are aligned to the falling edge of the clock. The input data is then sampled by the rising edge of the clock, as shown in Figure 17. In this manner, the allowed input jitter is 1UI p-p in an ideal situation. However, due to setup and hold time, the GS1540 typically achieves 0.5UI p-p input jitter tolerance without causing any errors in this block. When the signal is locked to the internal clock, the control output from the phase detector is refreshed at the transition of each rising edge of the data input. During this time, the phase of the clock drifts in one direction.

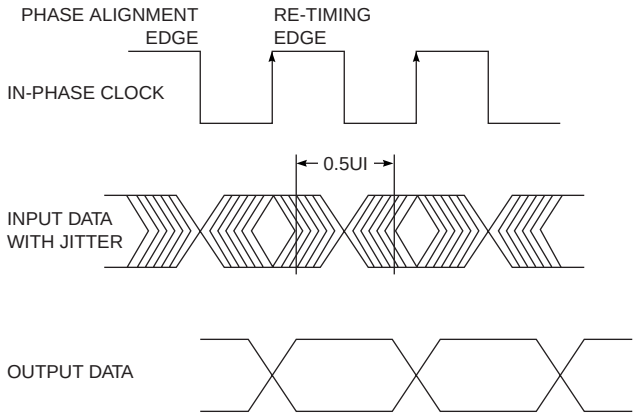


Fig. 17 Phase Detector Characteristics

During pathological signals, the amount of jitter that the phase detector will add can be calculated. By choosing the proper loop bandwidth, the amount of phase detector induced jitter can also be limited. Typically, for a 1.41MHz loop bandwidth at 0.2UI input jitter modulation, the phase detector induced jitter is about 0.015UIp-p. This is not very significant, even for the pathological signals.

CHARGE PUMP

The charge pump in a slew PLL is different from the charge pump in a linear PLL. There are two main functions of the charge pump. One function is to hold the frequency information of the input data. This information is held by C_{CP1}, which is connected between LFS and $\overline{LFS}$. The other capacitor, C_{CP2} between $\overline{LFS}$ and LFA_GND is used to remove common mode noise. Both C_{CP1} and C_{CP2} should be the same value. The second function of the charge pump is to provide a binary control voltage to the VCO depending upon the phase detector output. The output pin, LFA controls the VCO. Internally there is a 500Ω pull-up resistor, which is driven with a 100µA current called I_P. Another analog current I_F, with 5mA maximum drive proportional to the voltage across the $C_{CP1,}$ is applied at the same node. The voltage at the LFA node is V_{LFA_VCC} - 500(I_P+I_F) at any time.

Because of the integrator, I_F changes very slowly whereas I_P could change at the positive edge of the data transition as often as a clock period. In the locked position, the average voltage at the LFA (V_{LFA_VCC} – 500(I_P/2+I_F) is such that VCO generates frequency f, equal to the data rate clock frequency. Since I_P is changing all the time between 0A and 100µA, there will be two levels generated at the LFA output.

VCO

The GO1515 is an external hybrid VCO, which has a centre frequency of 1.485GHz and is also guaranteed to provide 1.485/1.001GHz within the control voltage (3.1V – 4.65V) of the GS1540 over process, power supply and temperature. The GO1515 is a very clean frequency source and, because of the internal high Q resonator, it is an order of magnitude more immune to external noise as compared to on-chip VCOs.

The VCO gain, Kf, is nominally 16MHz/V. The control voltage around the average LFA voltage will be 500 x I_P/2. This will produce two frequencies off from the centre by f=Kf x 500 x I_P/2.

LBCONT

The LBCONT pin is used to adjust the loop bandwidth by externally changing the internal charge pump current. For maximum loop bandwidth, connect LBCONT to the most positive power supply. For medium loop bandwidth, connect LBCONT through a pull-up resistor ($R_{PULL-UP}$). For low loop bandwidth, leave LBCONT floating. The formula below shows the loop bandwidth for various configurations.

$$LBW = LBW_{NOMINAL} \times \frac{(25k\Omega + R_{PULL-UP})}{(5k\Omega + R_{PULL-UP})}$$

where LBW nominal is the loop bandwidth when LBCONT is left floating.

LOOP BANDWIDTH OPTIMIZATION

Since the feed back loop has only digital circuits, the small signal analysis does not apply to the system. The effective loop bandwidth scales with the amount of input jitter modulation index.

PHASE LOCK

The phase lock circuit is used to determine the phase locked condition. It is done by generating a quadrature clock by delaying the in-phase clock (the clock whose falling edge is aligned to the data transition) by 166ps (0.25UI at 1.5GHz) with the tolerance of 0.05UI. When the PLL is locked, the falling edge of the in-phase clock is aligned with the data edges as shown in Figure 18. The quadrature clock is in a logic high state in the vicinity of input data transitions. The quadrature clock is sampled and latched by positive edges of the data transitions. The generated signal is low pass filtered with an RC network. The R is an on-chip 20kΩ resistor and C_{PL} is an external capacitor (recommended value 10nF). The time constant is about 67µs, or more than a video line.

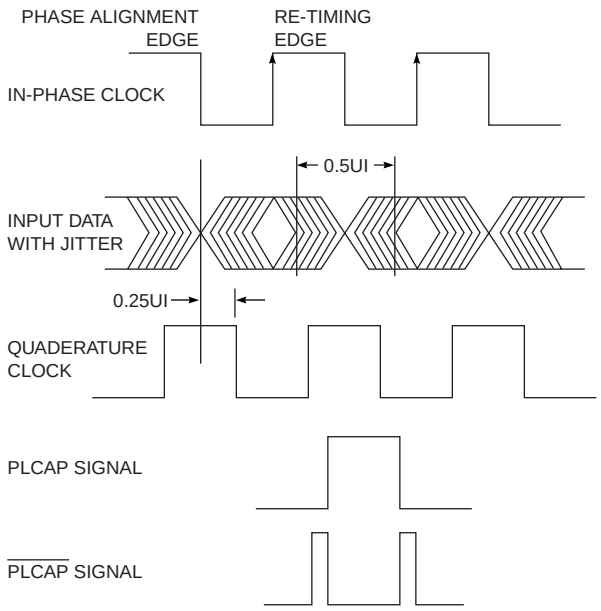


Fig. 18 PLL Circuit Principles

If the signal is not locked, the data transition phase could be anywhere with respect to the internal clock or the quadrature clock. In this case, the normalized filtered sample of the quadrature clock will be 0.5. When VCO is locked to the incoming data, data will only sample the quadrature clock when it is logic high. The normalized filtered sample quadrature clock will be 1.0. We chose a threshold of 0.66 to generate the phase lock signal. Because the threshold is lower than 1, it allows jitter to be greater than 0.5UI before the phase lock circuit reads it as "not phase locked".

INPUT JITTER INDICATOR (IJI)

This signal indicates the amount of excessive jitter (beyond the quadrature clock window 0.5UI), which occurs beyond the quadrature clock window *(see Figure 18)*. All the input data transitions occurring outside the quadrature clock window, will be captured and filtered by the low pass filter as mentioned in the Phase Lock section. The running time average of the ratio of the transitions inside the quadrature clock and outside the quadrature is available at the PLCAP/$\overline{\text{PLCAP}}$ pins. A signal, IJI, which is the buffered signal available at the PLCAP is provided so that loading does not effect the filter circuit. The signal at IJI is referenced with the power supply such that the factor V_{IJI}/V_{CC} is a constant over process and power supply for a given input jitter modulation. The IJI signal has 10kΩ output impedance. Figure 19 shows the relationship of the IJI signal with respect to the sine wave modulated input jitter.

P-P SINE WAVE JITTER IN UI	IJI VOLTAGE
0.00	4.75
0.15	4.75
0.30	4.75
0.39	4.70
0.45	4.60
0.48	4.50
0.52	4.40
0.55	4.30
0.58	4.20
0.60	4.10
0.63	3.95

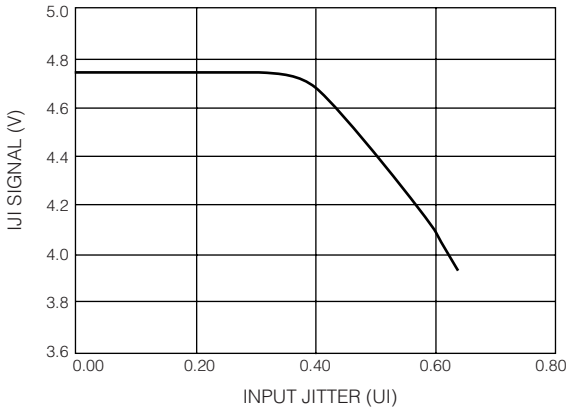


Fig. 19 Input Jitter Indicator (Typical at T_A = 25°C)

JITTER DEMODULATION (DM)

The differential jitter demodulation (DM) signal is available at the DM and $\overline{DM}$ pins. This signal is the phase correction signal of the PLL loop, which is amplified and buffered. If the input jitter is modulated, the PLL tracks the jitter if it is within loop bandwidth. To track the input jitter, the VCO has to be adjusted by the phase detector via the charge pump. Thus, the signal which controls the VCO contains the information of the input jitter modulation. The jitter demodulation signal is only valid if the input jitter is less than 0.5UIp-p. The DM/$\overline{DM}$ signals have 10kΩ output impedance, which could be low pass filtered with appropriate capacitors to eliminate high frequency noise. DFT_V_{EE} should be connected to GND to activate DM/$\overline{DM}$ signals.

The DM signals can be used as diagnostic tools. Assume there is an HDTV SDI source, which contains excessive noise during the horizontal blanking because of the transient current flowing in the power supply. In order to discover the source of the noise, one could probe around the source board with a low frequency oscilloscope (Bandwidth < 20MHz) that is triggered with an appropriately filtered DM/$\overline{DM}$ signal. The true cause of the modulation will be synchronous and will appear as a stationary signal with respect to the DM/$\overline{DM}$ signal.

Figure 20 shows an example of such a situation. An HDTV SDI signal is modulated with a modulation signal causing about 0.2UI jitter in Figure 20 (Channel 1). The GS1540 receives this signal and locks to it. Figure 20 (Channel 2) shows the DM signal. Notice the wave shape of the DM signal, which is synchronous to the modulating signal. The DM/$\overline{DM}$ signal could also be used to compare the output jitter of the HDTV signal source.

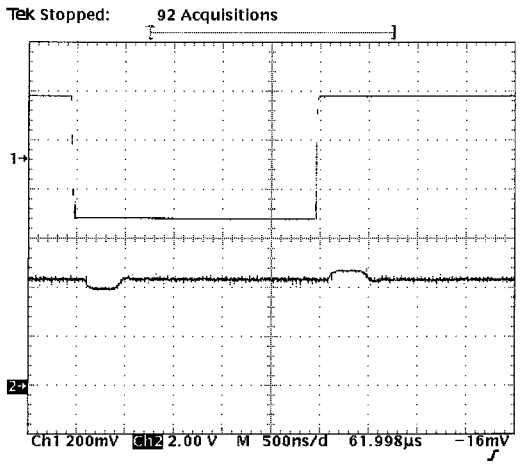


Fig. 20 Jitter Demodulation Signal

LOCK LOGIC

Logic is used to produce the PLL_LOCK signal which is based on the LFS signal and phase lock signal. When there is not any data input, the integrator will charge and eventually saturate at either end. By sensing the saturation of the integrator, it is determined that no data is present. If either data is not present or phase lock is low, the lock signal is made low. Logic signals are used to acquire the frequency by sweeping the integrator. Injecting a current into the summing node of the integrator achieves the sweep. The sweep is disabled once phase lock is asserted. The direction of the sweep is also changed once LFS saturates at either end.

$\overline{BYPASS}$

The $\overline{BYPASS}$ block bypasses the reclocked/mute path of the data whenever a logic low input is applied to the $\overline{BYPASS}$ input. In the bypass mode, the mute does not have any effect on the outputs. Also, the internal PLL still locks to a valid HDTV signal and shows PLL_LOCK.

SERIAL OUTPUT STAGE

The serial output (DDO, $\overline{DDO}$) signals have a nominal voltage of 400mVpp differential, or 200mVpp single ended when terminated with 50Ω.

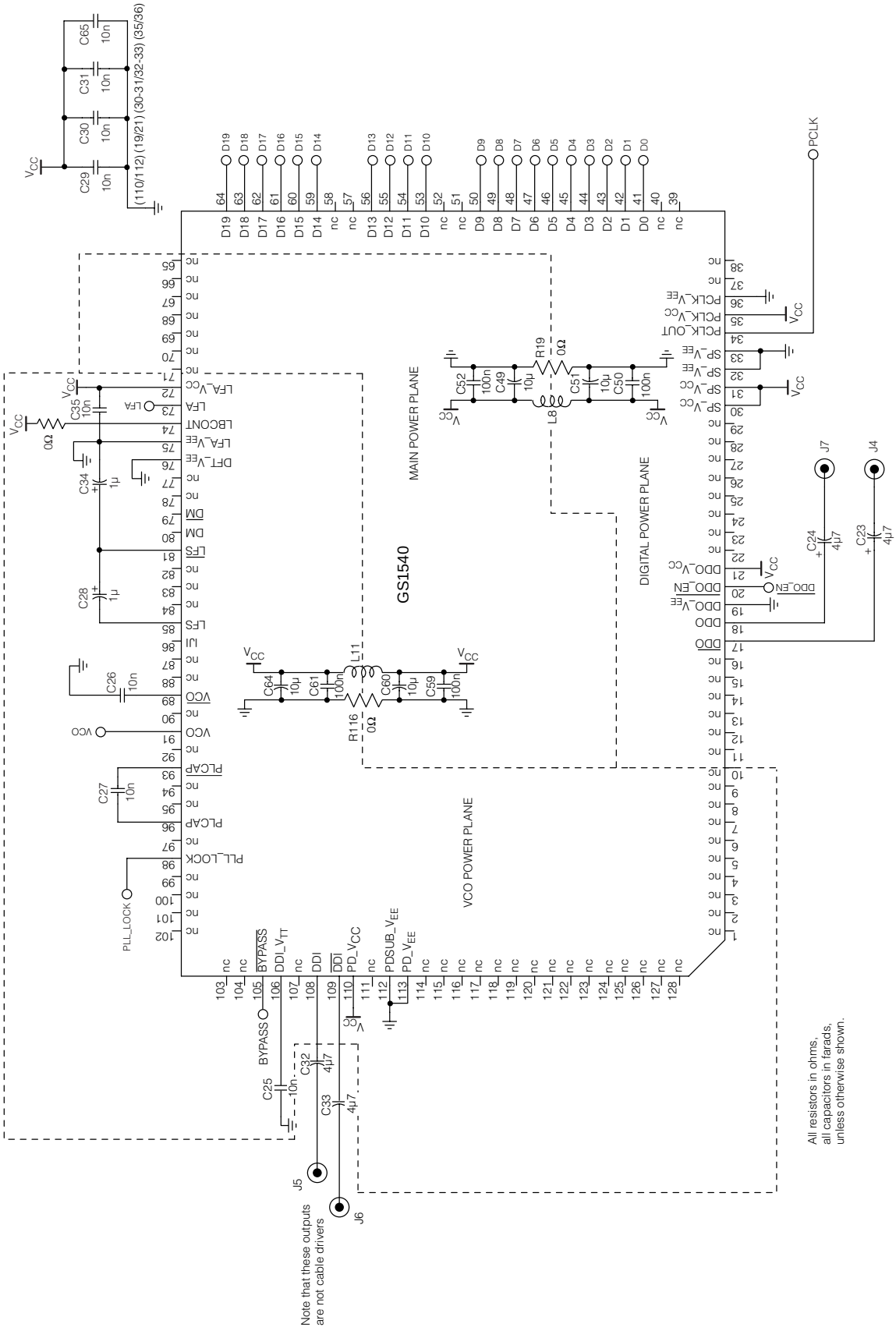
$\overline{DDO\_EN}$

The $\overline{DDO\_EN}$ enables or disables the serial output driver. To disable the driver, tie $\overline{DDO\_EN}$ to V_{CC}. To enable the driver, tie $\overline{DDO\_EN}$ to V_{EE}. When disabled, the supply current is reduced by approximately 10mA.

SERIAL TO PARALLEL CONVERTER

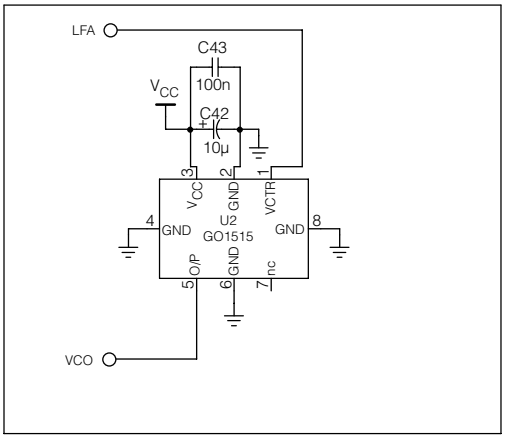
The high-speed serial to parallel converter accepts differential clock and data signals from the reclocker core. The S/P core converts this serial output into a 20-bit wide data stream (D[19:0]). Note that this data stream is not word aligned or descrambled. It also provides a parallel clock, which is 1/20th the serial clock rate (PCLK_OUT). The outputs of the S/P block are TTL compatible. When the PLL loses lock, the parallel clock continues to freewheel. The parallel clock and data outputs were designed for seamless interfaces to the GS1500 and GS1510 deformatters.

TYPICAL APPLICATION CIRCUIT

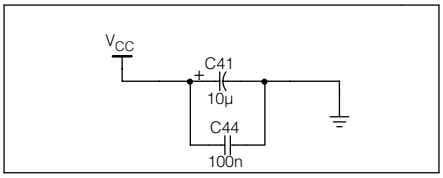


TYPICAL APPLICATION CIRCUIT (continued)

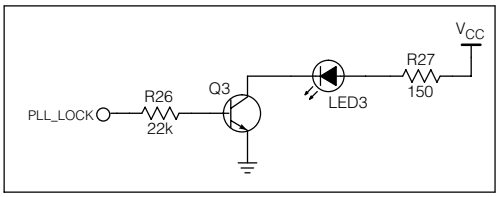
GO1515 VCO



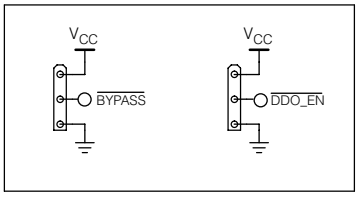
POWER CONNECT



GS1540 LOCK DETECT



GS1540 CONFIGURATION JUMPERS

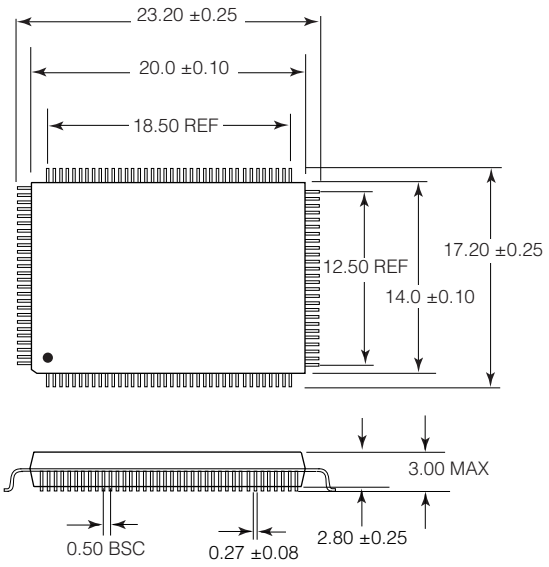


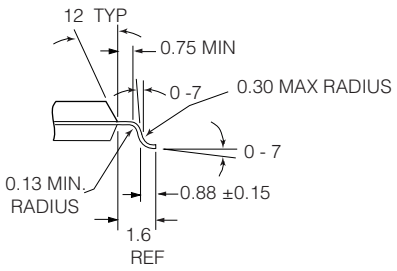
All resistors in ohms,
all capacitors in farads,
unless otherwise shown.

APPLICATION INFORMATION

Please refer to the EBHDRX evaluation board documentation for more detailed application and circuit information on using the GS1540 with the GS1500 and GS1510 Deformatters.

PACKAGE DIMENSIONS





128 pin MQFP
All dimensions are in millimetres.

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES

DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION

DOCUMENT IDENTIFICATION
PRELIMINARY DATA SHEET
The product is in a preproduction phase and specifications are subject to change without notice.

REVISION NOTES:
Added lead-free and green information.
For latest product information, visit www.gennum.com

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