

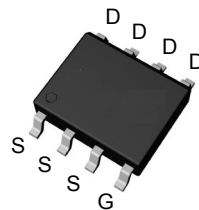
Features

- -40V/-11A,
 $R_{DS(ON)} = 12m\Omega$ (max.) @ $V_{GS} = -10V$
 $R_{DS(ON)} = 16m\Omega$ (max.) @ $V_{GS} = -4.5V$
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

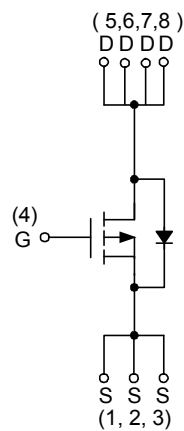
Applications

- Power Management in LCD TV Inverter.

Pin Description



Top View of SOP-8



P-Channel MOSFET

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DSS}	Drain-Source Voltage	-40	V
V_{GSS}	Gate-Source Voltage	± 20	
I_D^a	Continuous Drain Current ($V_{GS} = -10V$)	$T_A = 25^\circ C$	-11
		$T_A = 70^\circ C$	-9
I_{DM}^a	300 μs Pulsed Drain Current ($V_{GS} = -10V$)	-44	A
I_S^a	Diode Continuous Forward Current	-3	
I_{AS}^b	Avalanche Current, Single pulse ($L = 0.1mH$)	-33	
E_{AS}^b	Avalanche Energy, Single pulse ($L = 0.1mH$)	54	
T_J	Maximum Junction Temperature	150	$^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150	
P_D^a	Maximum Power Dissipation	$T_A = 25^\circ C$	3.1
		$T_A = 70^\circ C$	2.0
$R_{\theta JA}^a$	Thermal Resistance-Junction to Ambient	$t \leq 10s$	40
		Steady State	75
$R_{\theta JL}^c$	Thermal Resistance-Junction to Lead	Steady State	24

Note a: Surface Mounted on 1in² pad area, $t \leq 10sec$.

Note b: UIS tested and pulse width limited by maximum junction temperature 150 $^\circ C$ (initial temperature $T_J = 25^\circ C$).

Note c: The power dissipation P_D is based on $T_{J(MAX)} = 150^\circ C$, and it is useful for reducing junction-to-case thermal resistance ($R_{\theta JC}$) when additional heat sink is used.

Electrical Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_{DS} = -250\mu A$	-40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -32V, V_{GS} = 0V$	-	-	-1	μA
		$T_J = 85^\circ C$	-	-	-30	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{DS} = -250\mu A$	-1.4	-1.9	-2.4	V
I_{GSS}	Gate Leakage Current	$V_{GS} = \pm 25V, V_{DS} = 0V$	-	-	± 100	nA
$R_{DS(ON)}^a$	Drain-Source On-state Resistance	$V_{GS} = -10V, I_{DS} = -11A$	-	12	16	m Ω
		$V_{GS} = -4.5V, I_{DS} = -7A$	-	16	22	

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

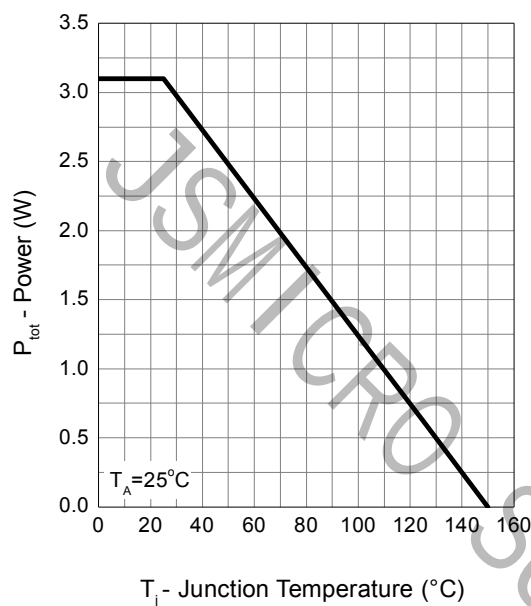
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Diode Characteristics						
V_{SD}^a	Diode Forward Voltage	$I_{SD}=-1A, V_{GS}=0V$	-	-0.75	-1	V
t_{rr}	Reverse Recovery Time	$I_{SD}=-11A, di_{SD}/dt=100A/\mu s$	-	24	-	ns
Q_{rr}	Reverse Recovery Charge		-	18	-	nC
Dynamic Characteristics ^b						
R_G	Gate Resistance	$V_{GS}=0V, V_{DS}=0V, F=1MHz$	-	2.3	-	Ω
C_{iss}	Input Capacitance	$V_{GS}=0V, V_{DS}=-20V, Frequency=1.0MHz$	-	1500	-	pF
C_{oss}	Output Capacitance		-	235	-	
C_{rss}	Reverse Transfer Capacitance		-	180	-	
$t_{d(ON)}$	Turn-on Delay Time	$V_{DD}=-20V, R_L=20\Omega, I_{DS}=-1A, V_{GEN}=-10V, R_G=6\Omega$	-	14	-	ns
t_r	Turn-on Rise Time		-	12	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	41	-	
t_f	Turn-off Fall Time		-	22	-	
Gate Charge Characteristics ^b						
Q_g	Total Gate Charge	$V_{DS}=-20V, V_{GS}=-10V, I_{DS}=-11A$	-	32	-	nC
Q_{gs}	Gate-Source Charge		-	5.2	-	
Q_{gd}	Gate-Drain Charge		-	8	-	

Note a: Pulse test; pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

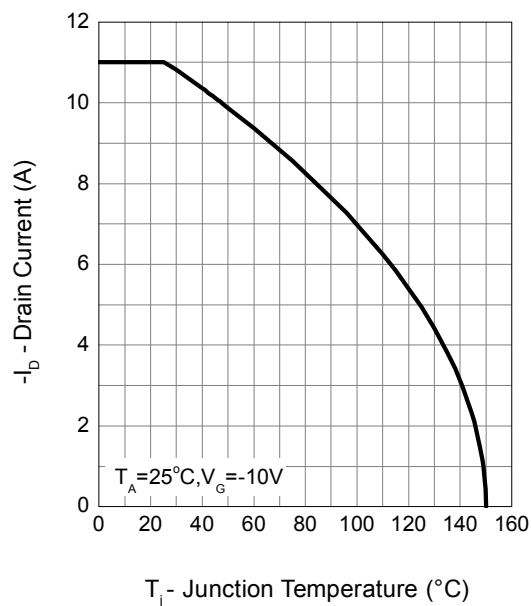
Note b: Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

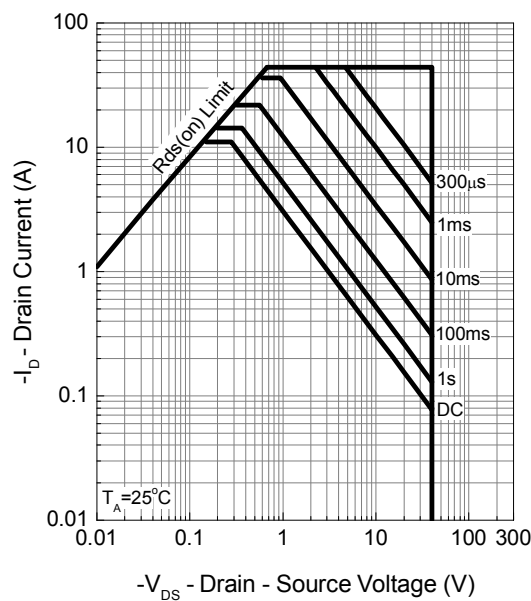
Power Dissipation



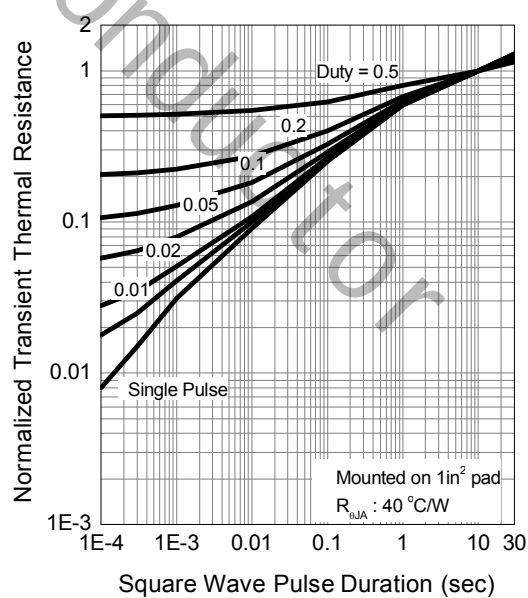
Drain Current



Safe Operation Area

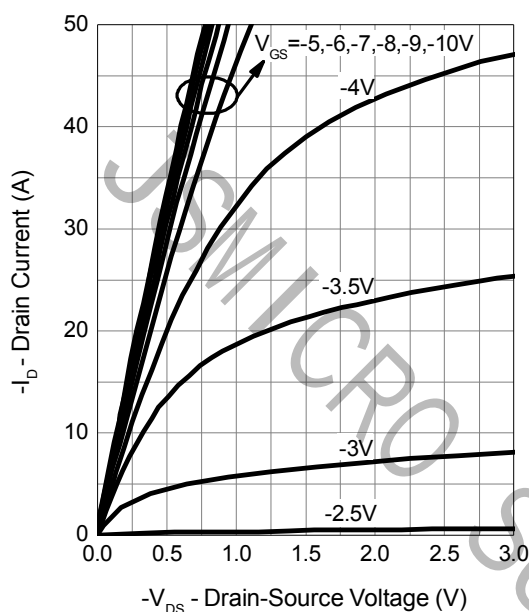


Thermal Transient Impedance

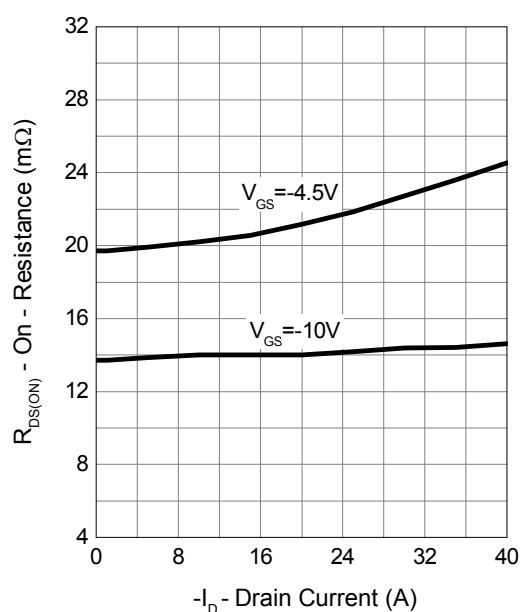


Typical Operating Characteristics (Cont.)

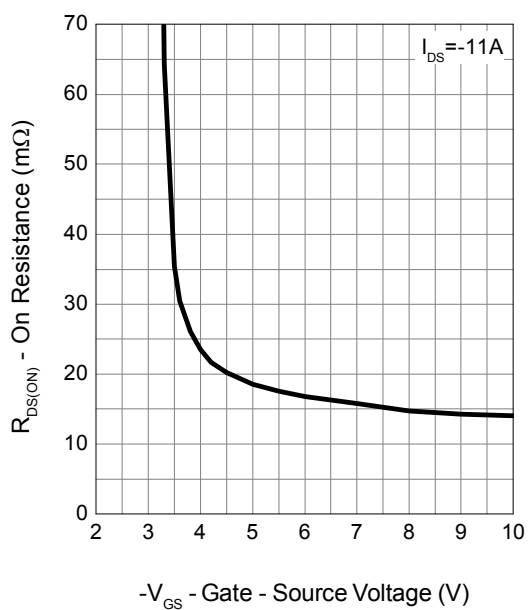
Output Characteristics



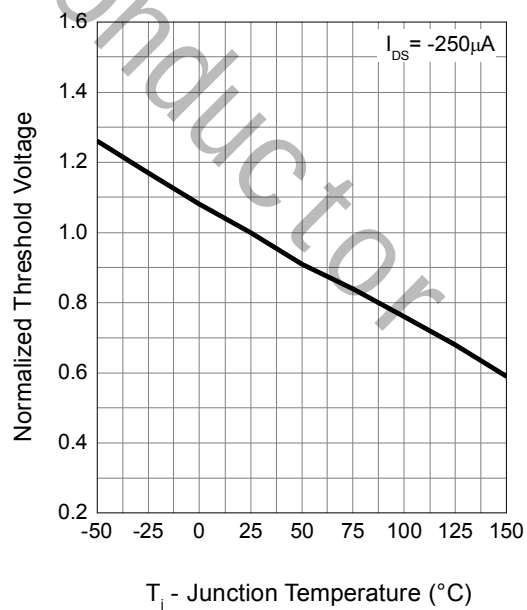
Drain-Source On Resistance



Gate-Source On Resistance

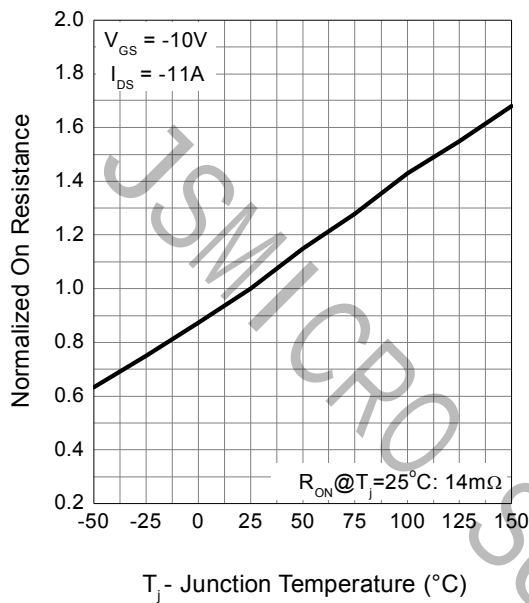


Gate Threshold Voltage

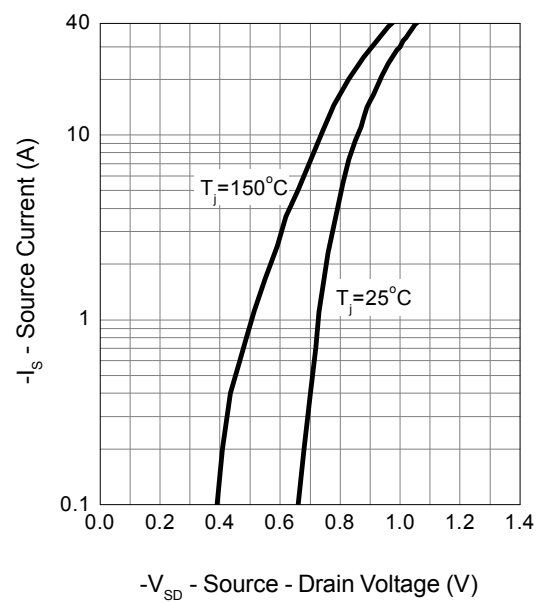


Typical Operating Characteristics (Cont.)

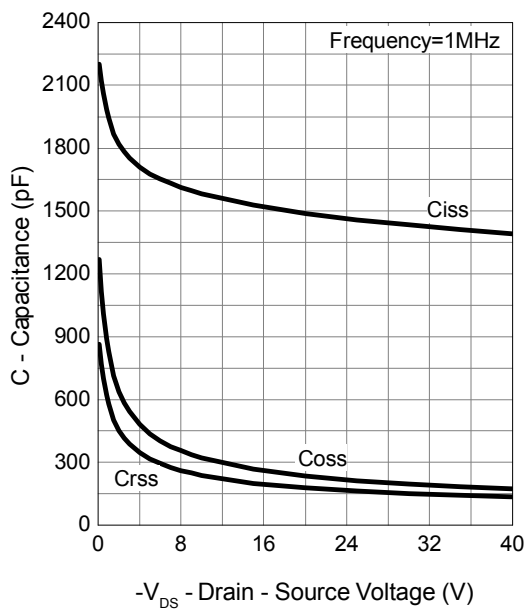
Drain-Source On Resistance



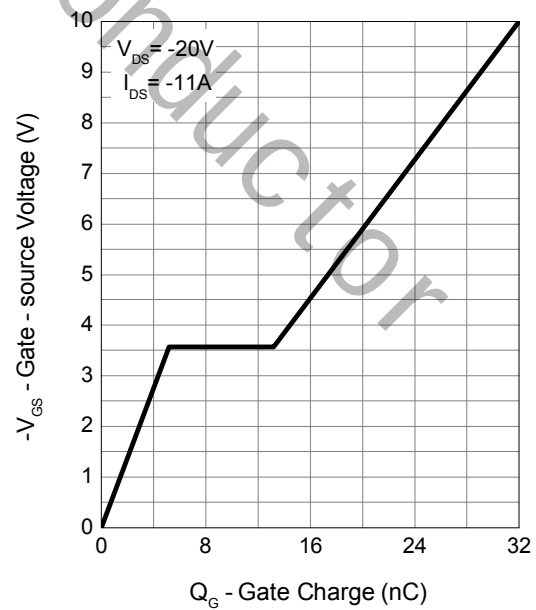
Source-Drain Diode Forward



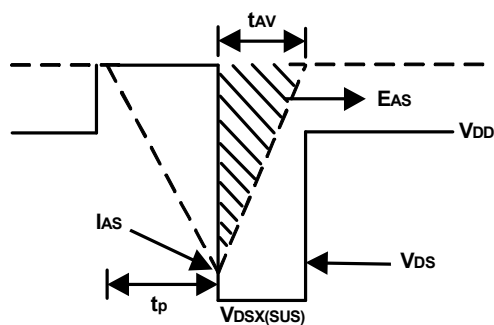
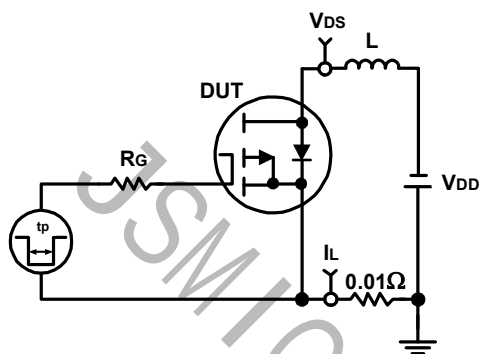
Capacitance



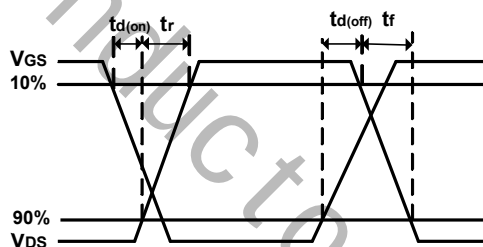
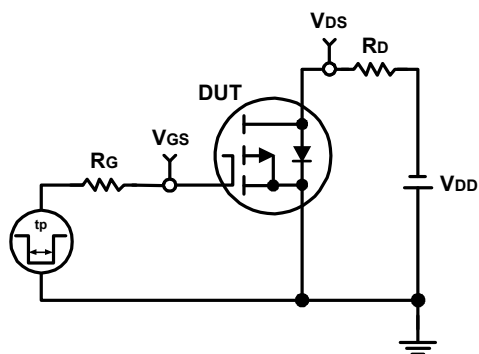
Gate Charge



Avalanche Test Circuit and Waveforms

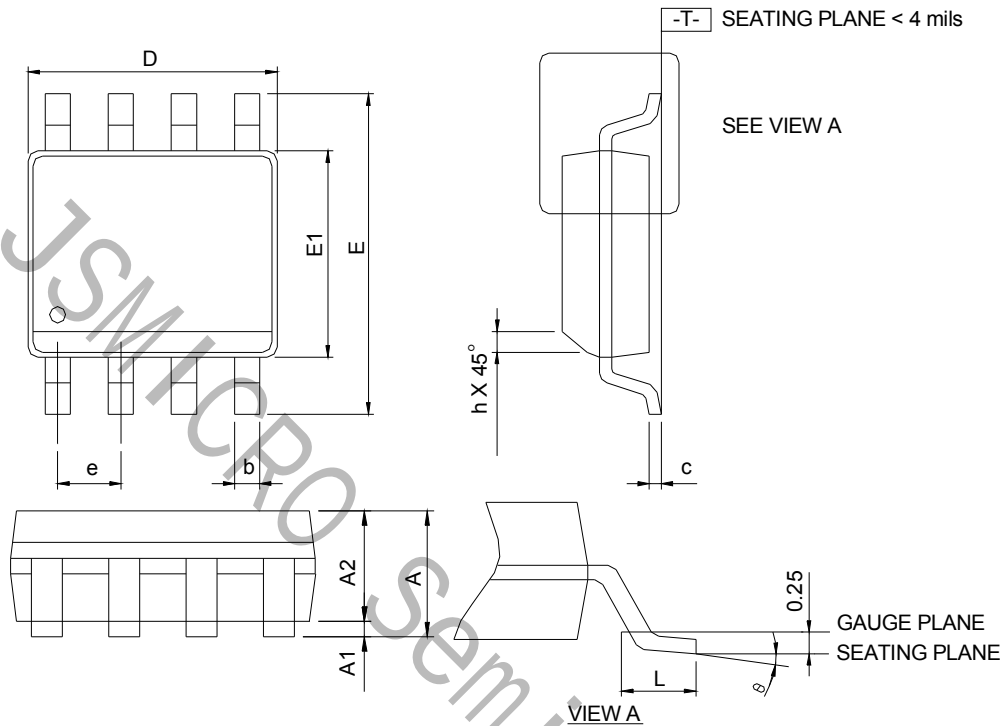


Switching Time Test Circuit and Waveforms



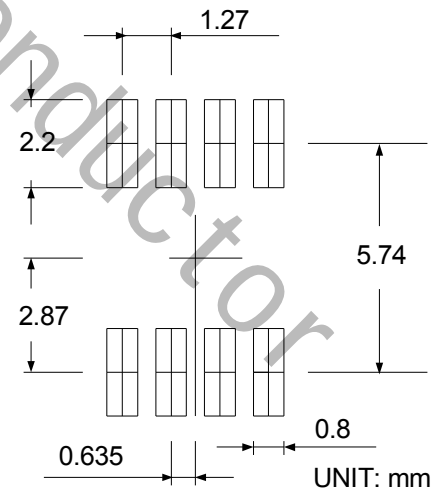
Package Information

SOP-8



	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



- Note: 1. Follow JEDEC MS-012 AA.
2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.