30V N-Channel MOSFET

PRODUCT SUMMARY

V_{DS}	30V
I_D (at V_{GS}=10V)	40A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 4.5mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	< 5.3mΩ

100% UIS Tested
100% R_g Tested

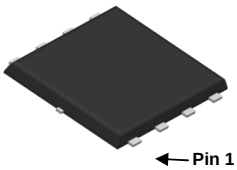
- Trench Power αMOS Technology
- Low $R_{DS(ON)}$
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

Applications

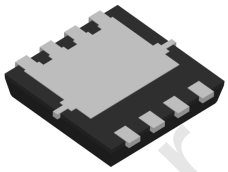
- DC/DC Converters in Computing
- Isolated DC/DC Converters in Telecom and Industrial

DFN 3x3_EP

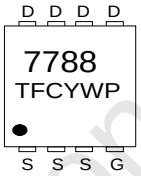
Top View



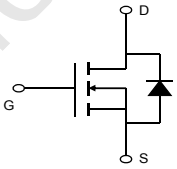
Bottom View



Top View



Equivalent Circuit



Y :year code W :week code

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
7788	7788	PDFN3x3-8	Ø330mm	12mm	4000 units

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current [G]	T_C=25°C	I_D	40	A
Pulsed Drain Current [C]		I_{DM}	150	
Continuous Drain Current	T_A=25°C	I_{DSM}	20	A
	T_A=70°C		16	
Avalanche Current [C]		I_{AS}, I_{AR}	35	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	61	mJ
Power Dissipation [B]	T_C=25°C	P_D	36	W
Power Dissipation [A]	T_A=25°C	P_{DSM}	3.1	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	30	40	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		60	75	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	2.8	3.4	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=10mA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			0.5	uA
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±12V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1.2	1.6	2	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	150			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		4.5	5.5	mΩ
		V_{GS}=4.5V, I_D=20A		6.5	7.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		115		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.4	0.7	V
I_S	Maximum Body-Diode Continuous Current [G]				40	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz	2730	3415	4100	pF
C_{oss}	Output Capacitance		240	340	440	pF
C_{rss}	Reverse Transfer Capacitance		140	232	325	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.6	1.2	1.8	Ω
SWITCHING PARAMETERS						
Q_g(4.5V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, ID=20A	19	24	29	nC
Q_{gs}	Gate Source Charge			6.6		nC
Q_{gd}	Gate Drain Charge			10		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		9		ns
t_r	Turn-On Rise Time			4.5		ns
$t_{D(off)}$	Turn-Off DelayTime			47		ns
t_f	Turn-Off Fall Time			5.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/μs	8	10	12	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/μs	12	15	18	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ t ≤ 10s value and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

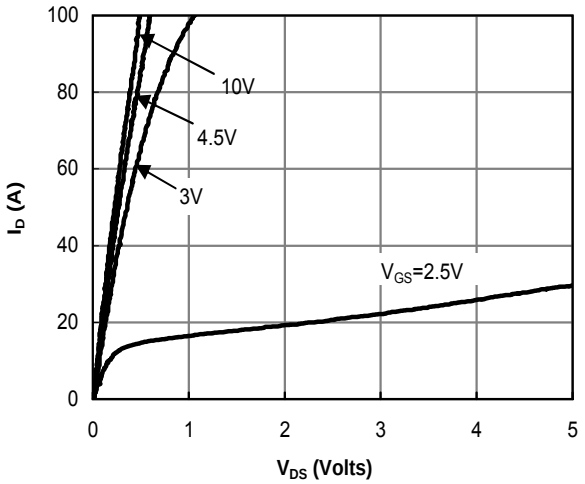

Fig 1: On-Region Characteristics (Note E)

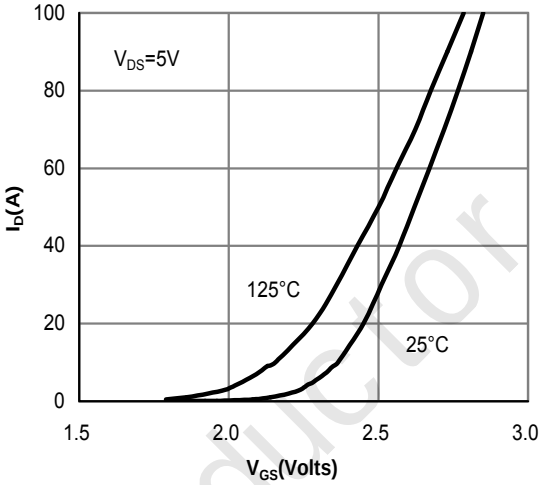

Figure 2: Transfer Characteristics (Note E)

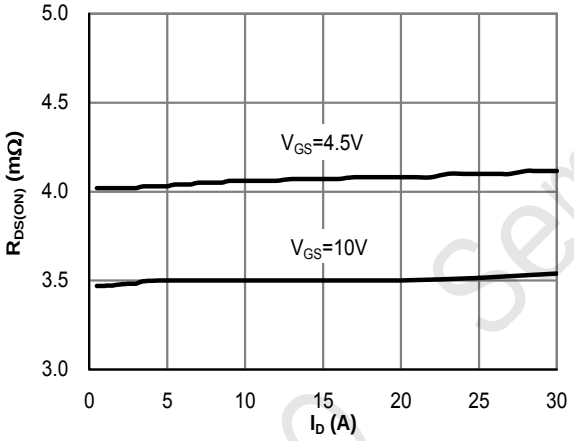

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

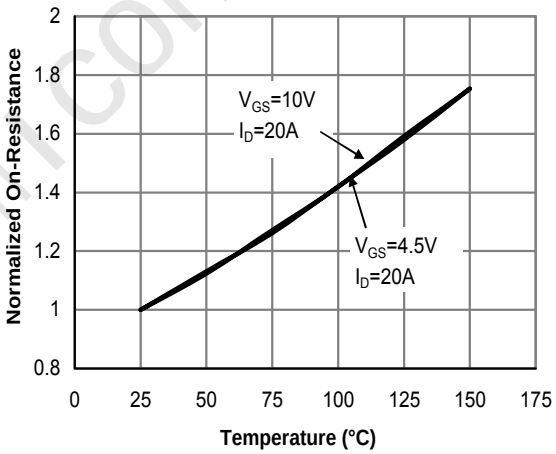

Figure 4: On-Resistance vs. Junction Temperature (Note E)

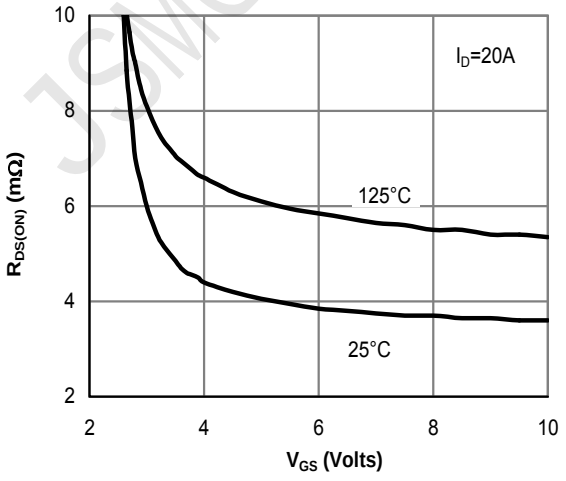

Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

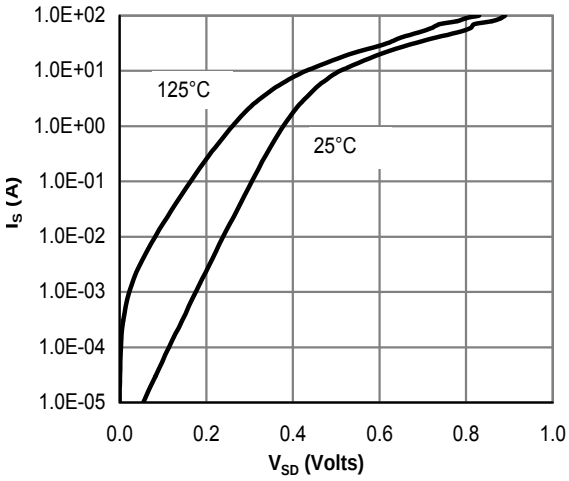

Figure 6: Body-Diode Characteristics (Note E)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

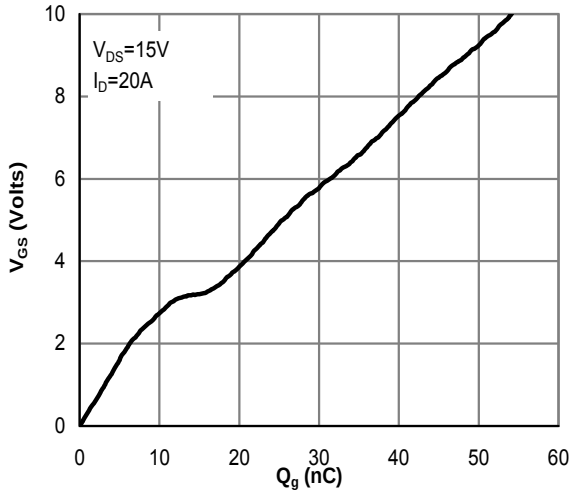

Figure 7: Gate-Charge Characteristics

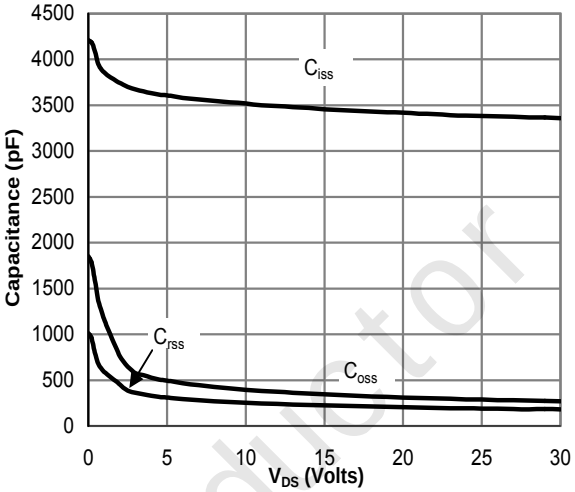

Figure 8: Capacitance Characteristics

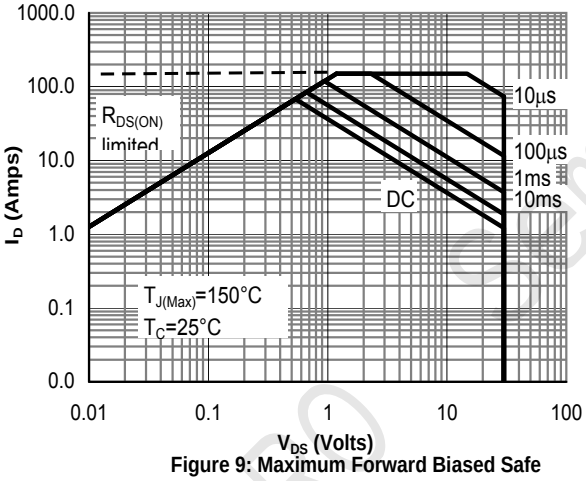

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

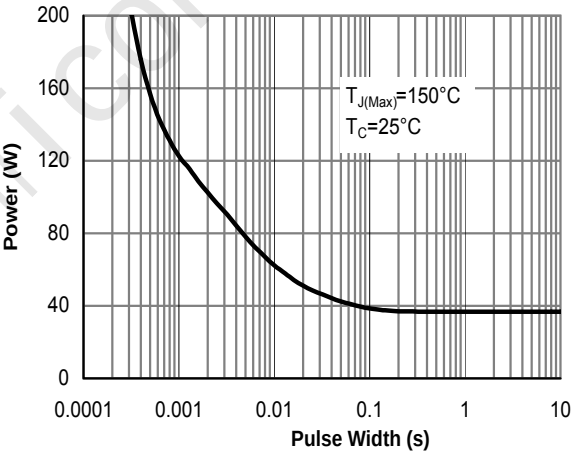

Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

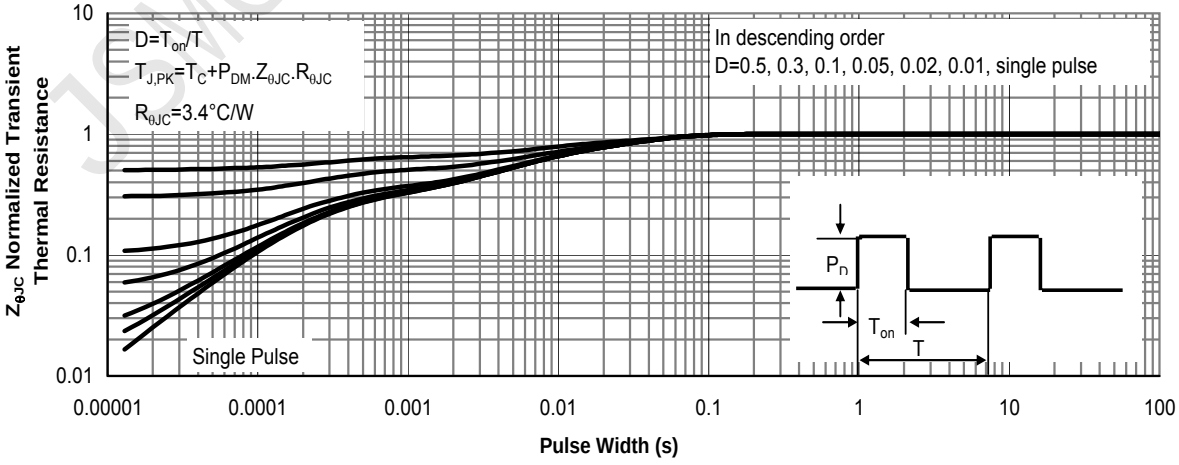

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

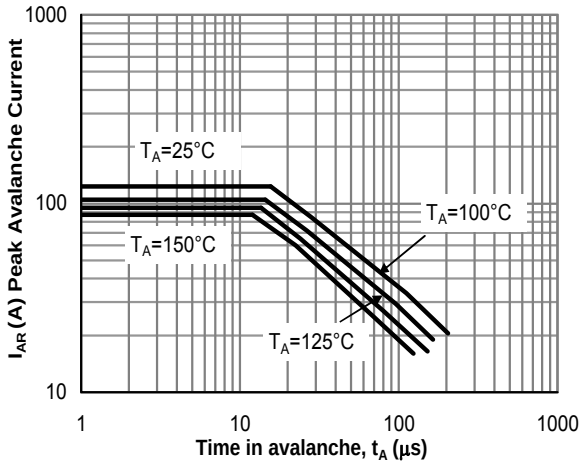

Figure 12: Single Pulse Avalanche capability (Note C)

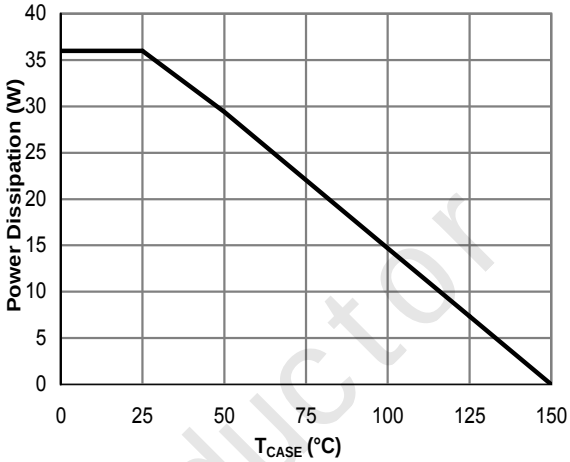

Figure 13: Power De-rating (Note F)

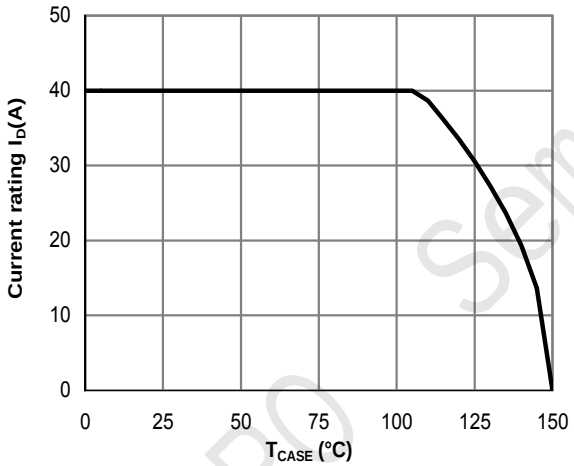

Figure 14: Current De-rating (Note F)

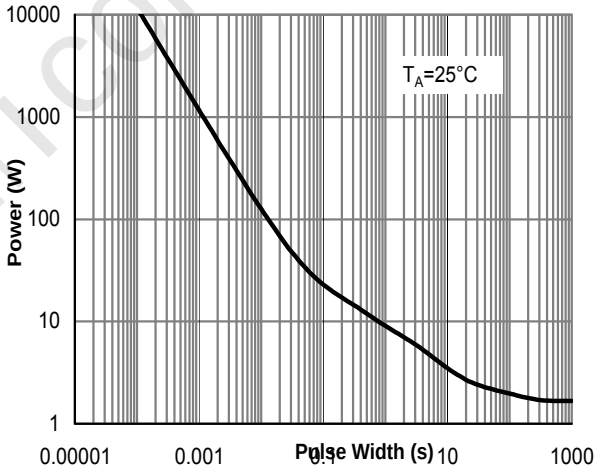

Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

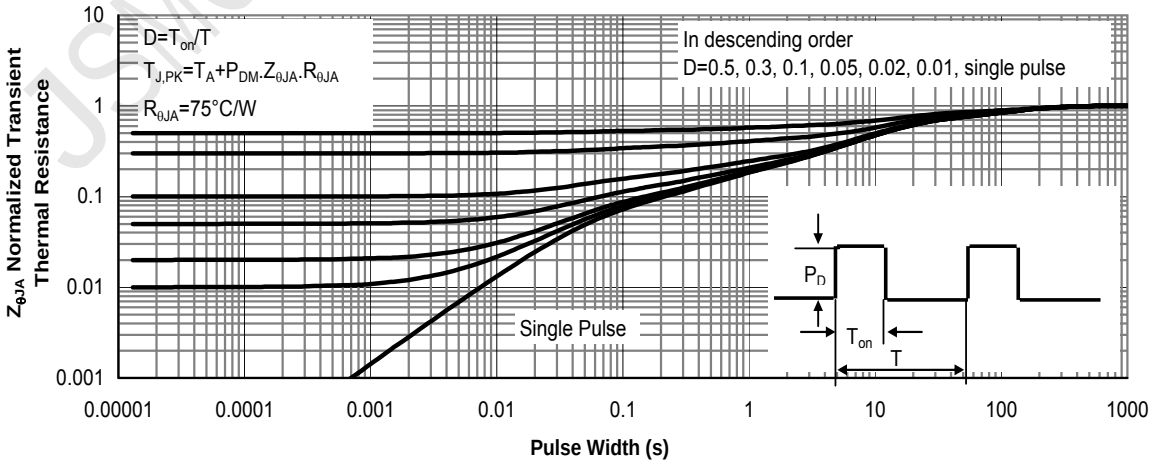

Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

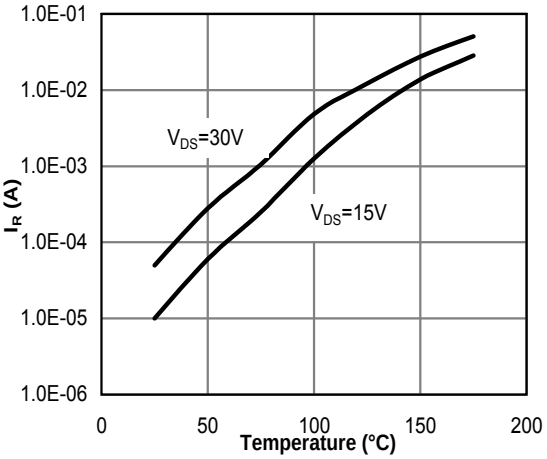

Figure 17: Diode Reverse Leakage Current vs. Junction Temperature

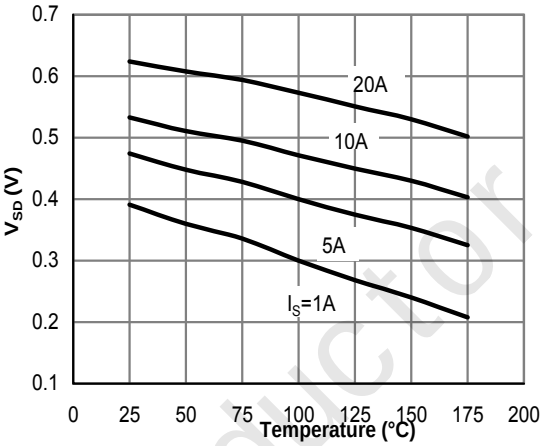

Figure 18: Diode Forward voltage vs. Junction Temperature

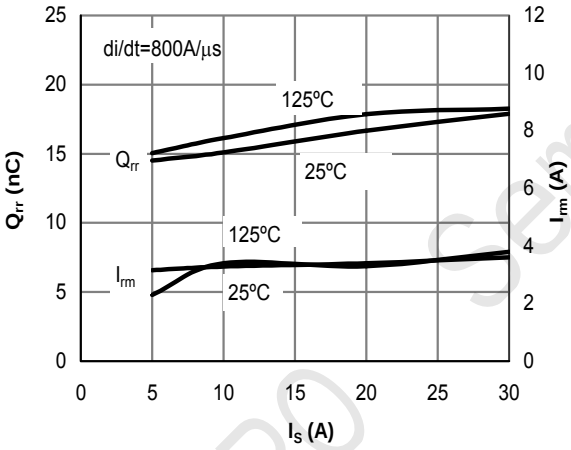

Figure 19: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

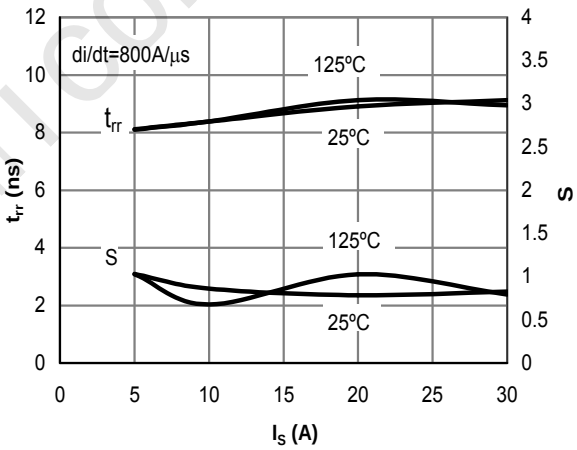

Figure 20: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

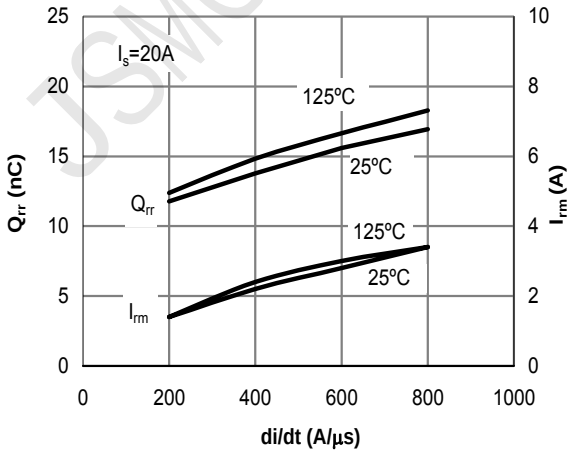

Figure 21: Diode Reverse Recovery Charge and Peak Current vs. di/dt

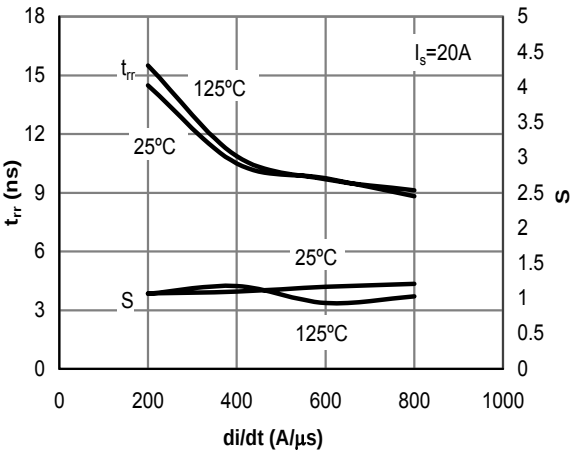

Figure 22: Diode Reverse Recovery Time and Softness Factor vs. di/dt

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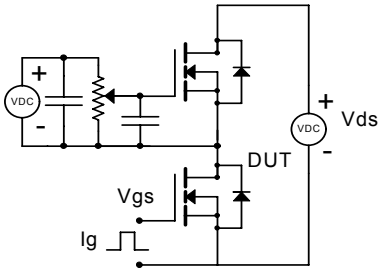
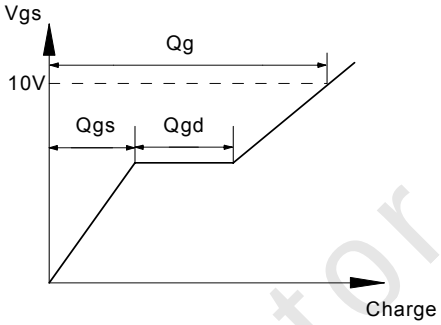
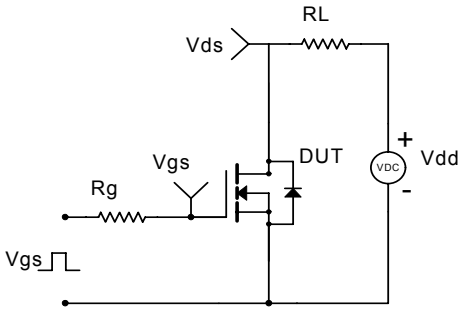
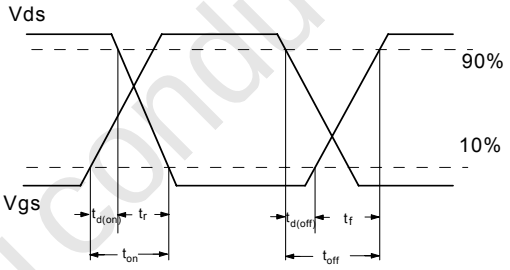
Gate Charge Test Circuit & Waveform



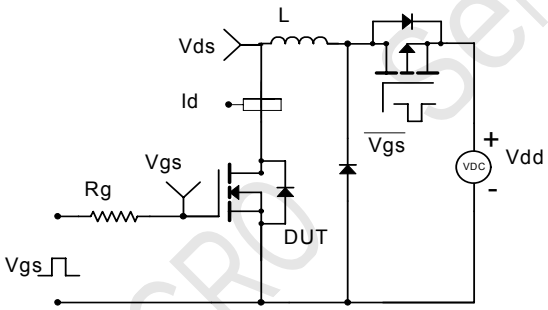


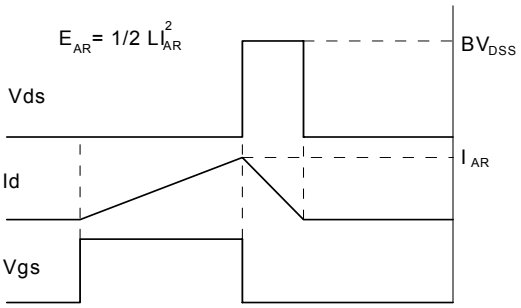
Resistive Switching Test Circuit & Waveforms



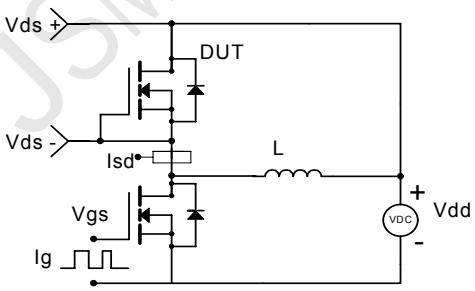


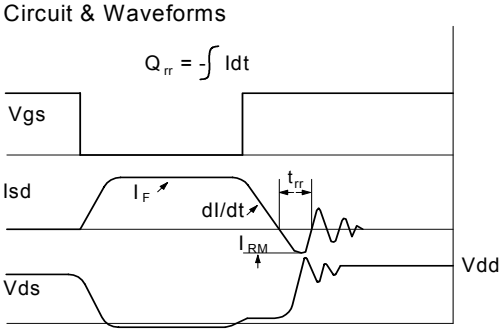
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms





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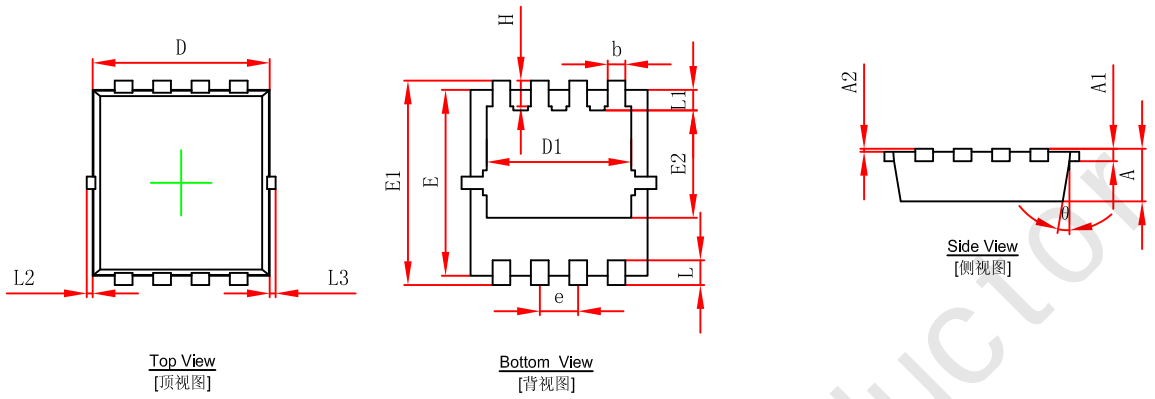
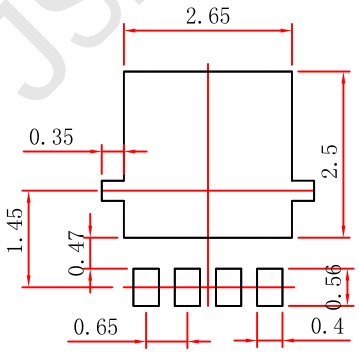
PDFN 3x3-8L Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.650	0.850	0.026	0.033
A1	0.152 REF.		0.006 REF.	
A2	0~0.05		0~0.002	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.102
E	2.900	3.100	0.114	0.122
E1	3.150	3.450	0.124	0.136
E2	1.535	1.935	0.060	0.076
b	0.200	0.400	0.008	0.016
e	0.550	0.750	0.022	0.030
L	0.300	0.500	0.012	0.020
L1	0.180	0.480	0.007	0.019
L2	0~0.100		0~0.004	
L3	0~0.100		0~0.004	
H	0.315	0.515	0.012	0.020
θ	9°	13°	9°	13°

PDFNWB3.3x3.3-8L Suggested Pad Layout



Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.05mm.
3.The pad layout is for reference purposes only.

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