

PRODUCT SUMMARY				
	V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
N-Channel	20	0.040 at $V_{GS} = 4.5$ V	4.2	3.7 nC
		0.065 at $V_{GS} = 2.5$ V	3.3	
P-Channel	- 20	0.090 at $V_{GS} = - 4.5$ V	- 2.9	5.3 nC
		0.137 at $V_{GS} = - 2.5$ V	- 2.3	

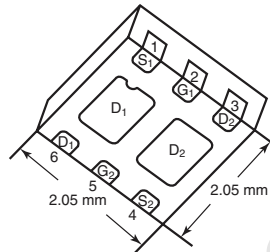
FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Power MOSFETs
- New Thermally Enhanced PowerPAK® SC-70 Package
 - Small Footprint Area
 - Low On-Resistance
- Compliant to RoHS Directive 2002/95/EC

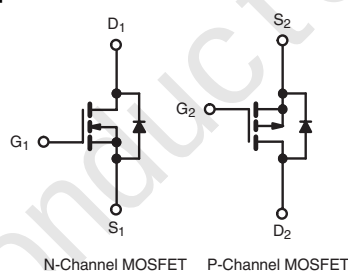
APPLICATIONS

- Load Switch for Portable Devices

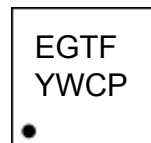
DFN2X2-6L



Equivalent Circuit



MARKING



Y :year code W :week code

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V _{DS}	20	- 20	V
Gate-Source Voltage		V _{GS}	± 12		
Continuous Drain Current (T _J = 150 °C)	T _C = 25 °C	I _D	4.2	- 2.9	A
Pulsed Drain Current		I _{DM}	15	- 15	
Source Drain Current Diode Current	T _C = 25 °C	I _S	4.5	- 4.5	
Maximum Power Dissipation	T _C = 25 °C	P _D	7.8	7.8	W
	T _A = 25 °C		1.9	1.9	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature) ^{d, e}			260		

THERMAL RESISTANCE RATINGS							
Parameter		Symbol	N-Channel		P-Channel		Unit
			Typ.	Max.	Typ.	Max.	
Maximum Junction-to-Ambient ^{b, f}	$t \leq 5$ s	R_{thJA}	52	65	52	65	$^\circ\text{C/W}$
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	12.5	16	12.5	16	

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)								
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit	
Static								
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	N-Ch	20			V	
		V _{GS} = 0 V, I _D = - 250 μA	P-Ch	- 20				
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA	N-Ch		23		mV/°C	
		I _D = - 250 μA	P-Ch		- 11			
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	N-Ch		- 3.3			
		I _D = - 250 μA	P-Ch		2.6			
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.6		1.4	V	
		V _{DS} = V _{GS} , I _D = - 250 μA	P-Ch	- 0.5		- 1.3		
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 12 V	N-Ch			± 0.1	μA	
			P-Ch			± 0.1		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V	N-Ch			0.1		
		V _{DS} = - 20 V, V _{GS} = 0 V	P-Ch			- 0.1		
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 4.5 V	N-Ch	10			A	
		V _{DS} ≤ - 5 V, V _{GS} = - 4.5 V	P-Ch	- 10				
Drain-Source On-State Resistance ^b	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.2 A	N-Ch		0.032	0.040	Ω	
		V _{GS} = - 4.5 V, I _D = - 2.9 A	P-Ch		0.074	0.090		
		V _{GS} = 2.5 V, I _D = 3.3 A	N-Ch		0.053	0.065		
		V _{GS} = - 2.5 V, I _D = - 2.3 A	P-Ch		0.113	0.137		
Forward Transconductance ^b	g _{fs}	V _{DS} = 10 V, I _D = 4.2 A	N-Ch		12		S	
		V _{DS} = - 10 V, I _D = - 2.9 A	P-Ch		7			
Dynamic ^a								
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		350		pF	
Output Capacitance	C _{oss}		P-Ch		340			
Reverse Transfer Capacitance	C _{rss}	P-Channel V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch		82			
			P-Ch		105			
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 10 V, I _D = 5.5 A	N-Ch		7.7	12	nC	
		V _{DS} = - 10 V, V _{GS} = - 10 V, I _D = - 3.7 A	P-Ch		10.5	16		
		N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 5.5 A	N-Ch		3.7	6		
			P-Ch		5.3	8		
Gate-Source Charge	Q _{gs}	P-Channel V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 3.7 A	N-Ch		0.85			
Gate-Drain Charge	Q _{gd}		P-Ch		0.75			
			N-Ch		0.95			
			P-Ch		2			
Gate Resistance	R _g	f = 1 MHz	N-Ch	0.7	3.5	7	Ω	
			P-Ch	0.2	10	20		

Notes:

a. Guaranteed by design, not subject to production testing.

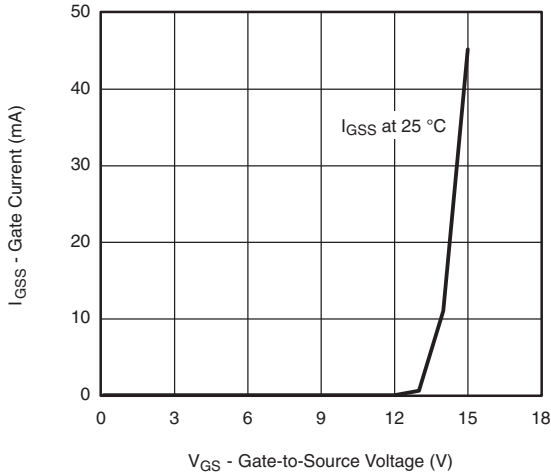
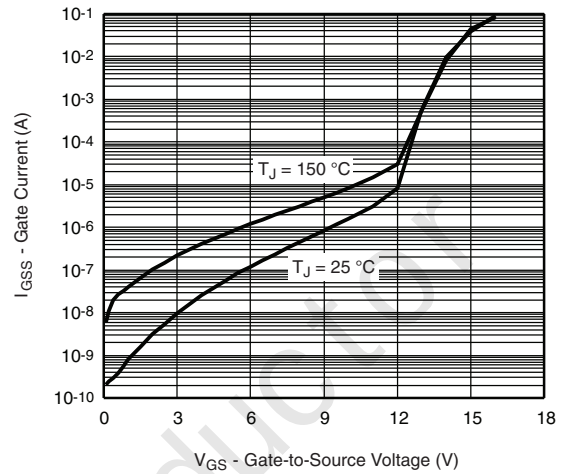
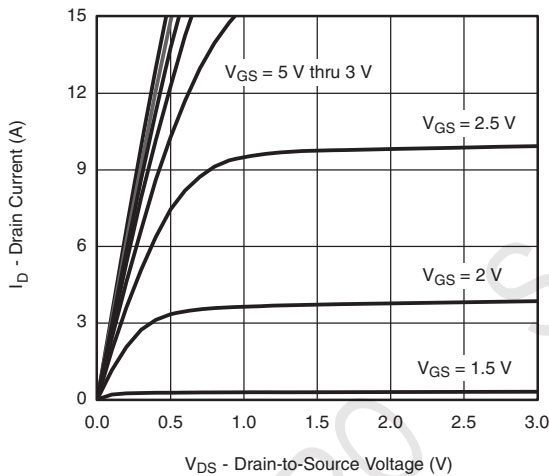
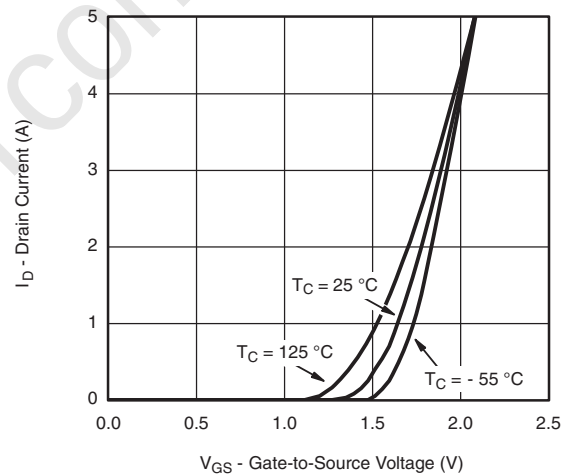
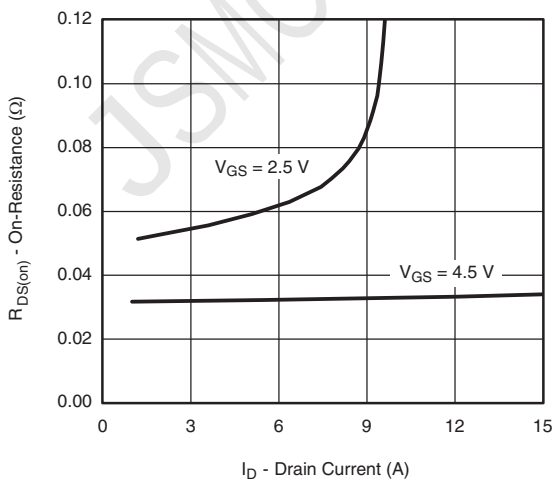
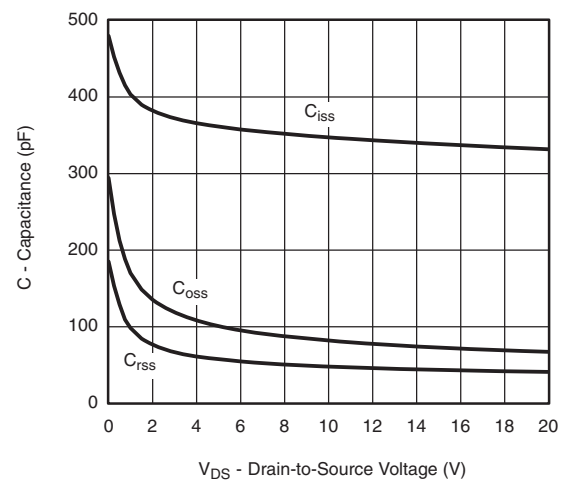
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

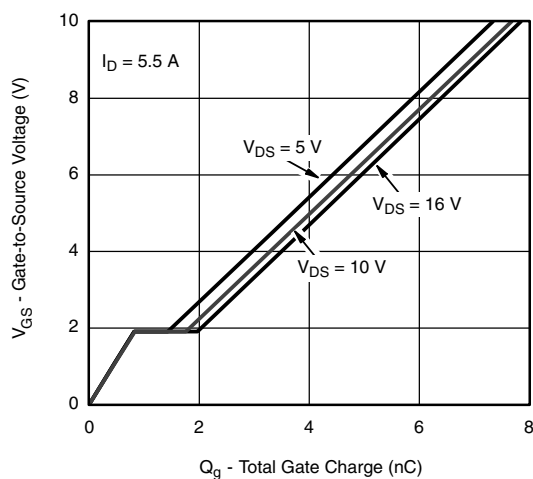
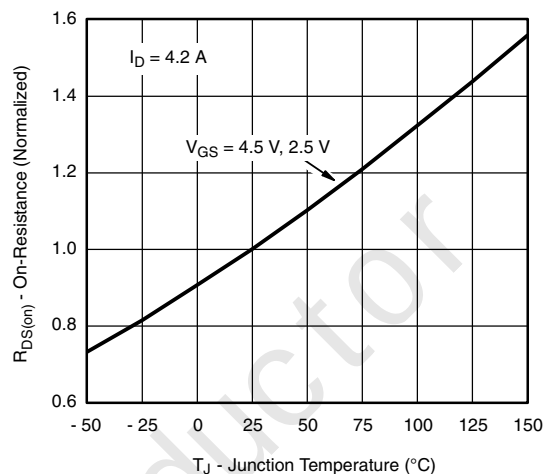
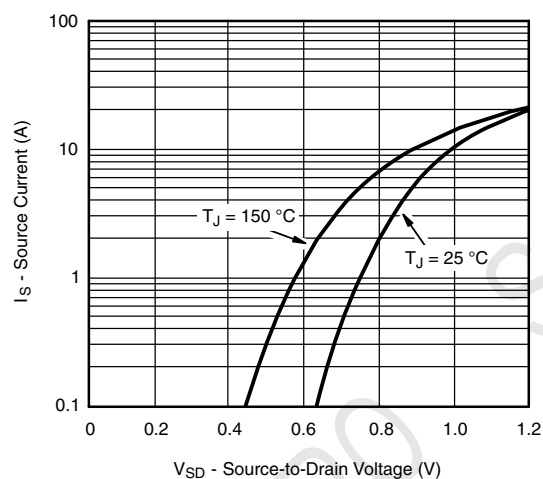
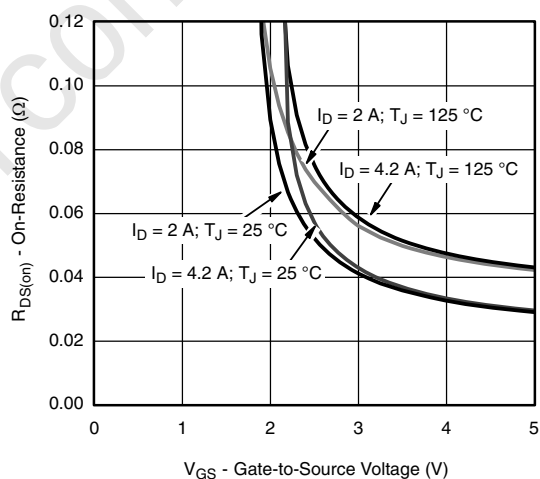
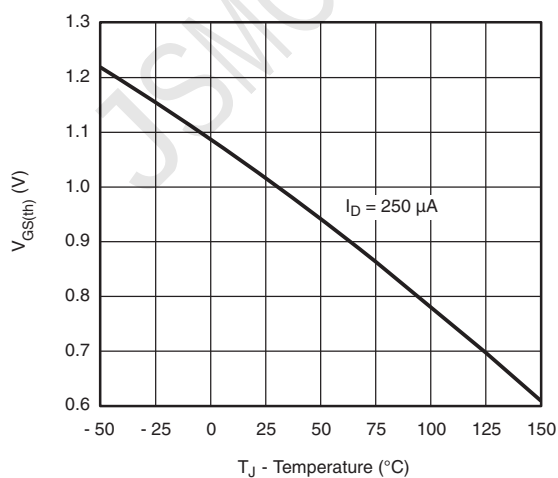
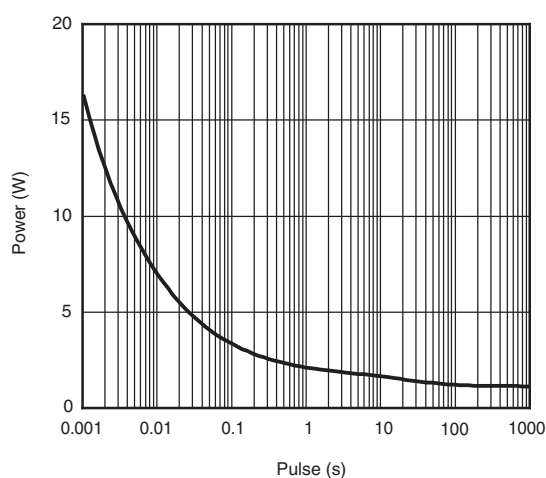
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Dynamic ^a							
Turn-On Delay Time	t _{d(on)}	N-Channel V _{DD} = 10 V, R _L = 2.3 Ω I _D ≅ 4.4 A, V _{GEN} = 4.5 V, R _g = 1 Ω	N-Ch		10	15	ns
Rise Time	t _r		P-Ch		20	30	
			N-Ch		12	20	
Turn-Off Delay Time	t _{d(off)}		P-Ch		20	30	
		N-Ch		21	35		
Fall Time	t _f	P-Ch		25	40		
		N-Ch		16	25		
Turn-On Delay Time	t _{d(on)}	P-Ch		10	15		
		N-Ch		5	10		
Rise Time	t _r	P-Ch		5	10		
		N-Ch		10	15		
Turn-Off Delay Time	t _{d(off)}	P-Ch		10	15		
		N-Ch		15	25		
Fall Time	t _f	P-Ch		20	30		
		N-Ch		10	15		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	N-Ch			4.5	A
			P-Ch			- 4.5	
Pulse Diode Forward Current ^a	I _{SM}		N-Ch			15	A
			P-Ch			- 15	
Body Diode Voltage	V _{SD}	I _S = 4.4 A, V _{GS} = 0 V	N-Ch		0.8	1.2	V
		I _S = - 3 A, V _{GS} = 0 V	P-Ch		- 0.8	- 1.2	
Body Diode Reverse Recovery Time	t _{rr}	N-Channel I _F = 4.4 A, di/dt = 100 A/μs, T _J = 25 °C	N-Ch		15	30	ns
			P-Ch		26	50	
Body Diode Reverse Recovery Charge	Q _{rr}		N-Ch		8	20	nC
			P-Ch		13	25	
Reverse Recovery Fall Time	t _a	P-Channel I _F = - 3 A, di/dt = - 100 A/μs, T _J = 25 °C	N-Ch		8		ns
			P-Ch		14		
Reverse Recovery Rise Time	t _b		N-Ch		7		ns
			P-Ch		12		

Notes:

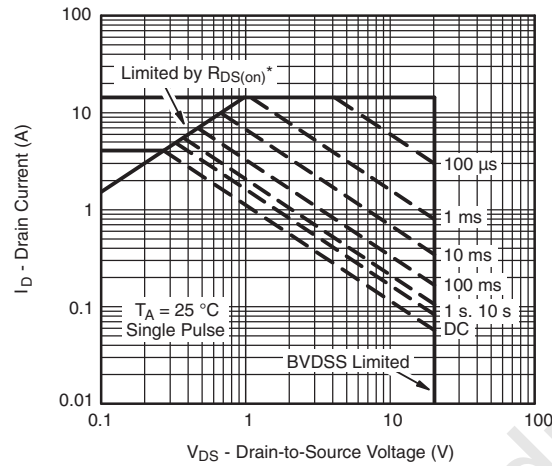
a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Current vs. Gate-Source Voltage

Gate Current vs. Gate-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

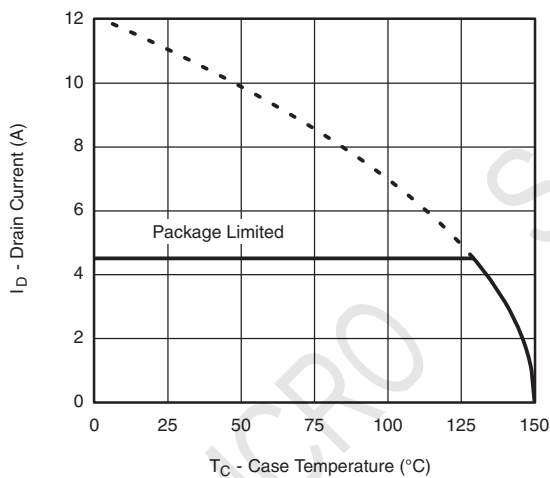
N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Charge

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power (Junction-to-Ambient)

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

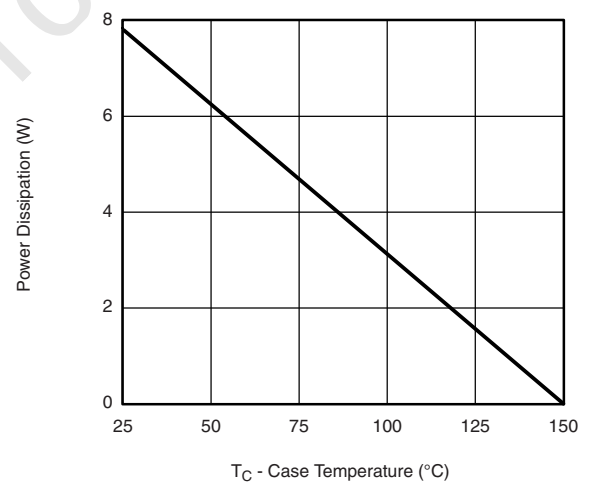


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

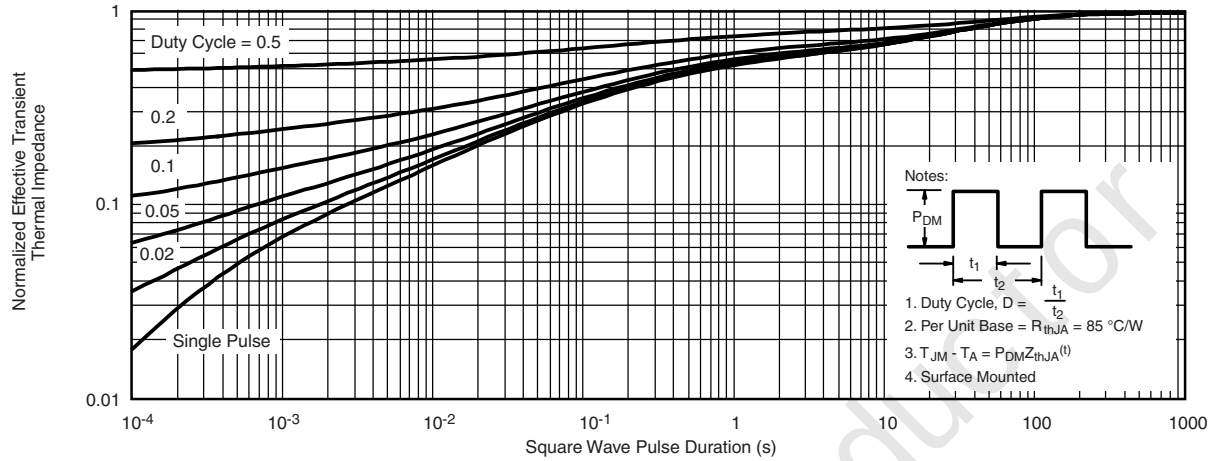
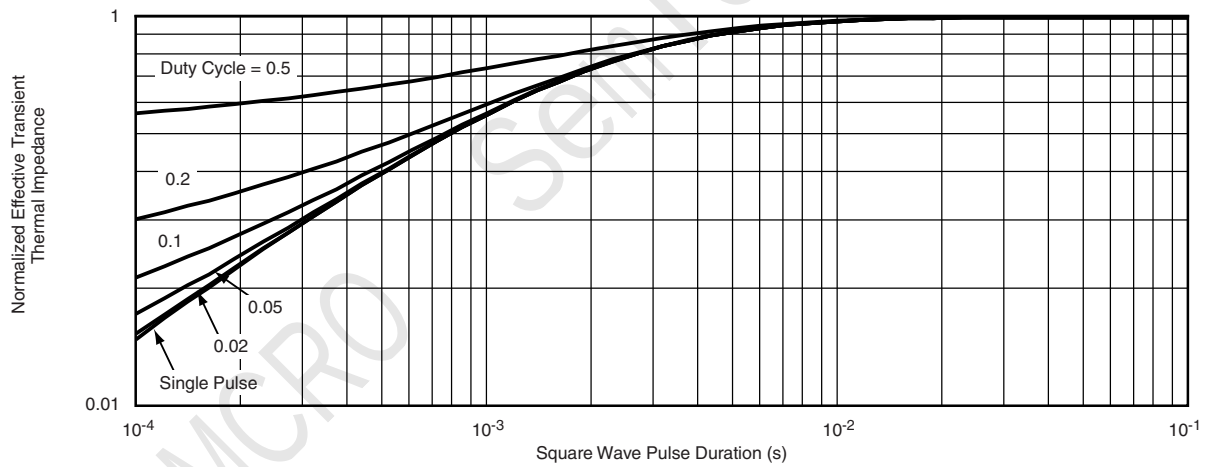


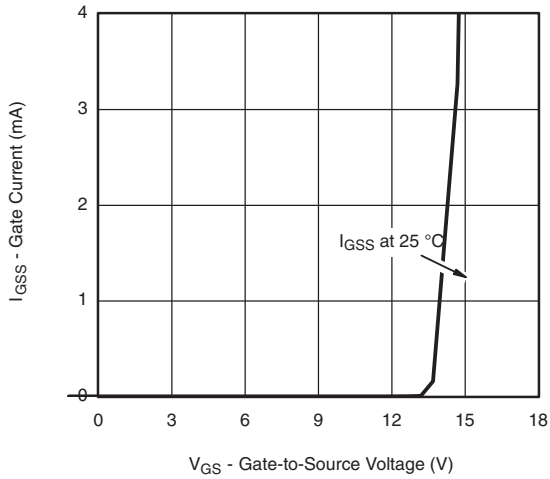
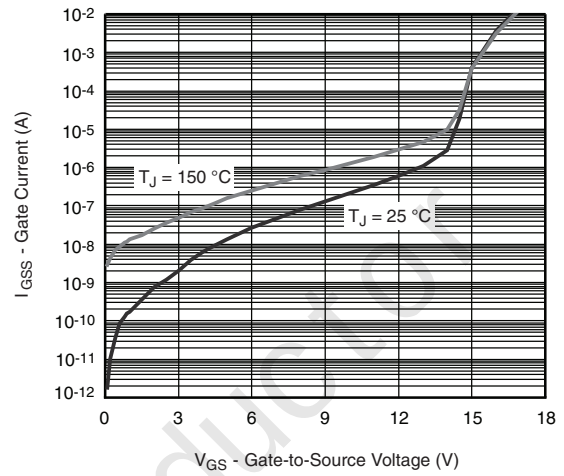
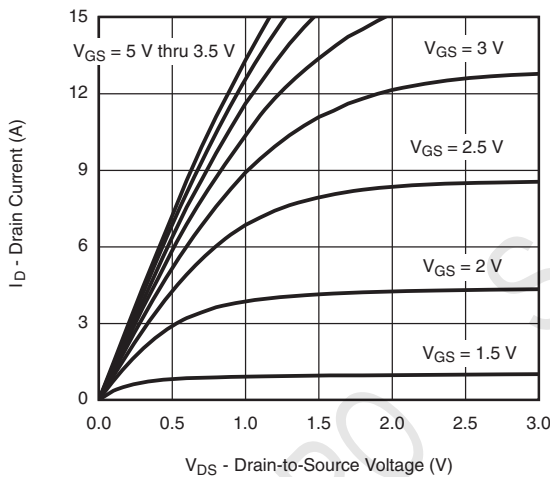
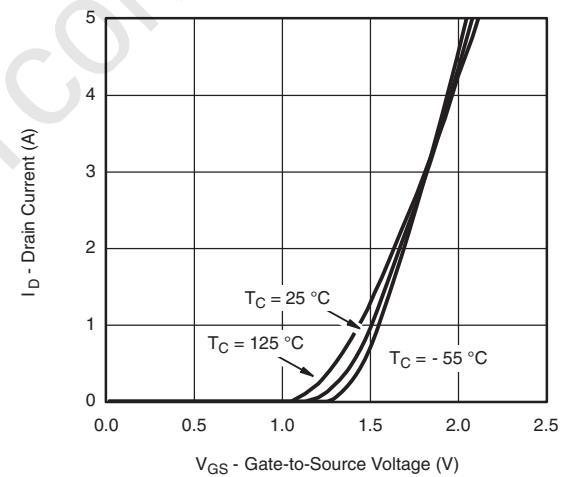
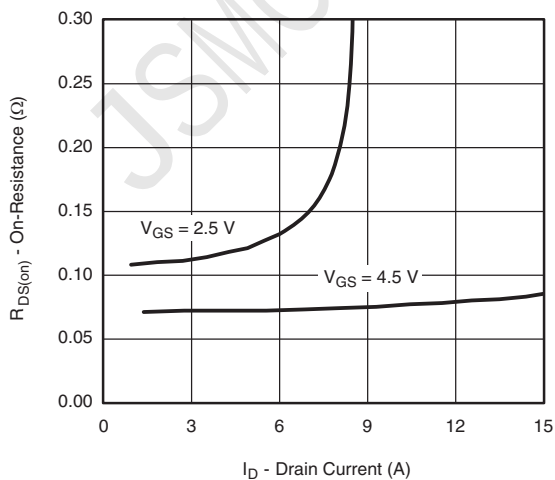
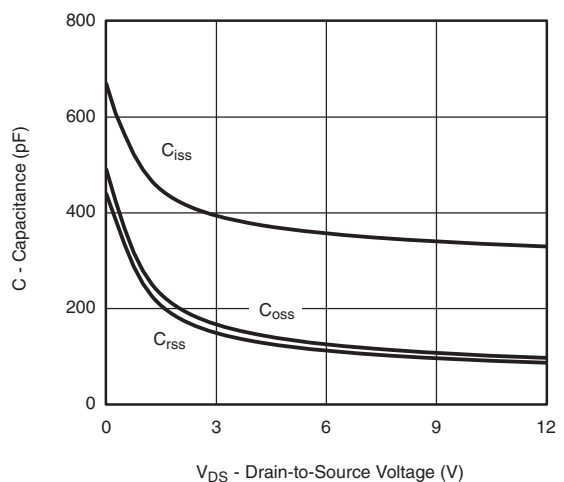
Current Derating*

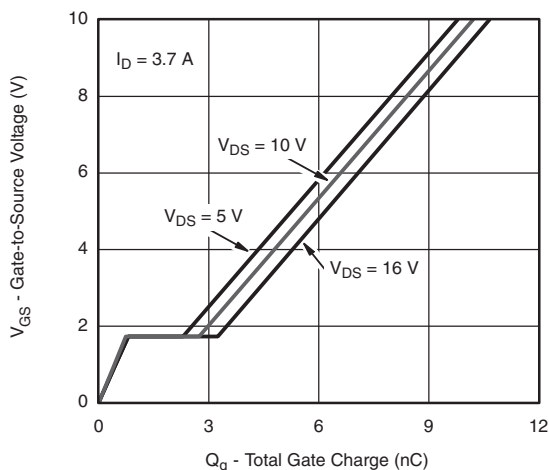
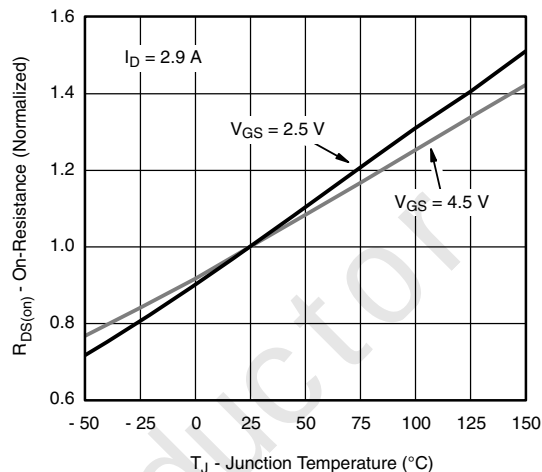
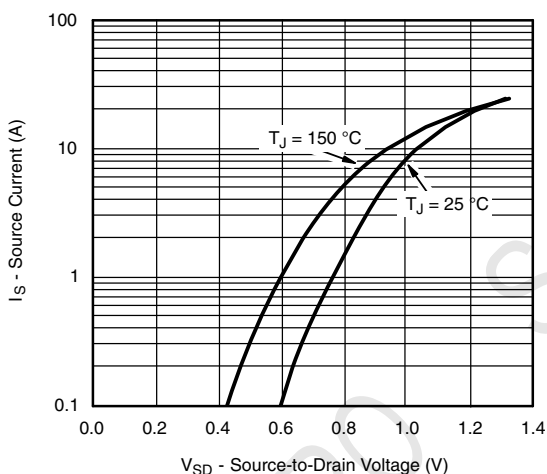
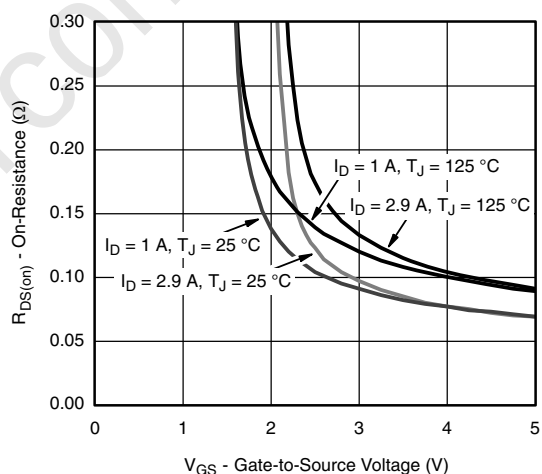
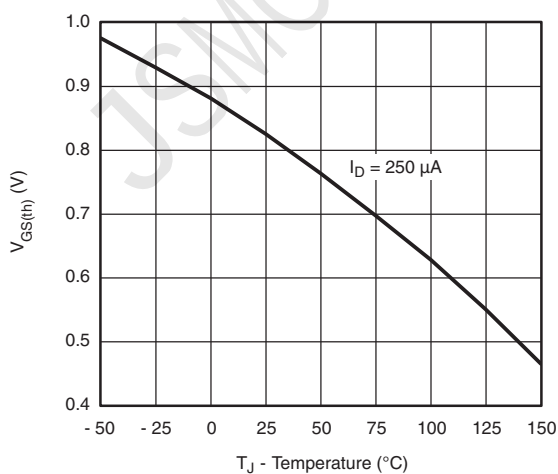
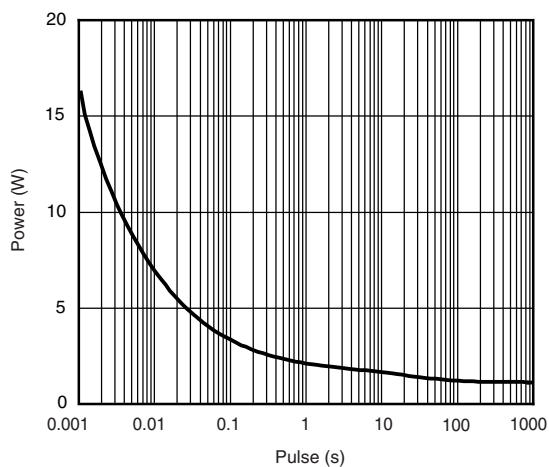


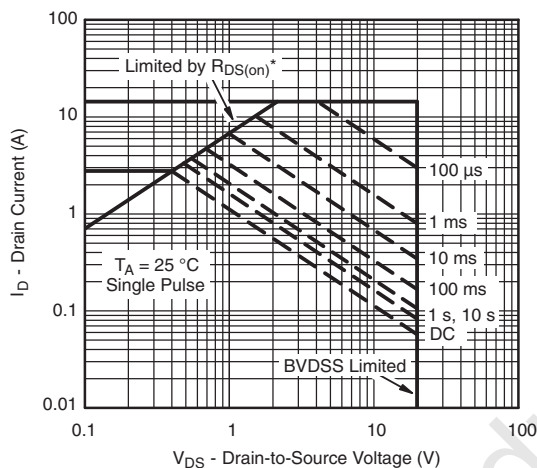
Power Derating

* The power dissipation P_D is based on $T_{J(max.)} = 150\text{ }^{\circ}\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

N-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case

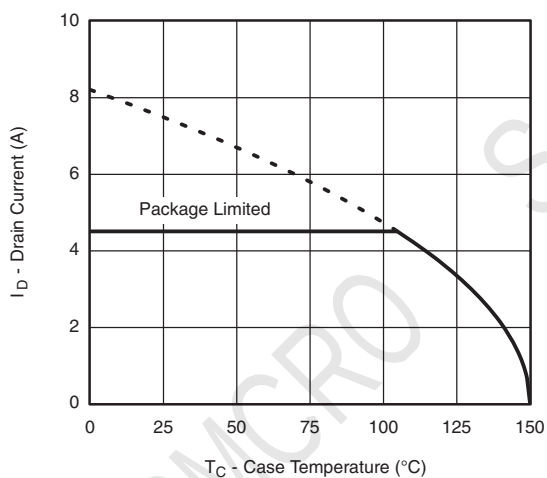
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Current vs. Gate-Source Voltage

Gate Current vs. Gate-Source Voltage

Output Characteristics

Transfer Characteristics

On-Resistance vs. Drain Current and Gate Voltage

Capacitance

P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Gate Charge

On-Resistance vs. Junction Temperature

Source-Drain Diode Forward Voltage

On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

Single Pulse Power (Junction-to-Ambient)

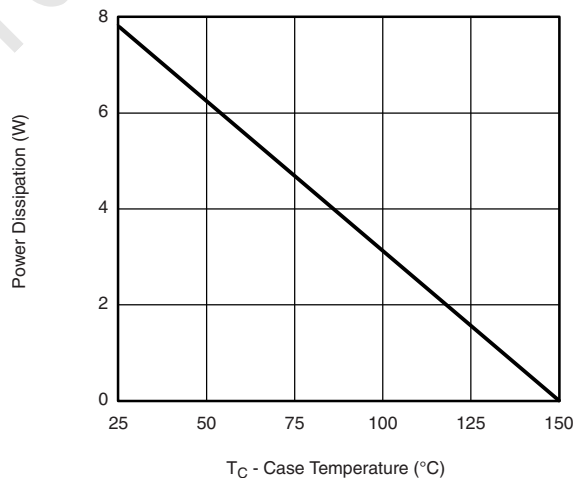
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area, Junction-to-Ambient

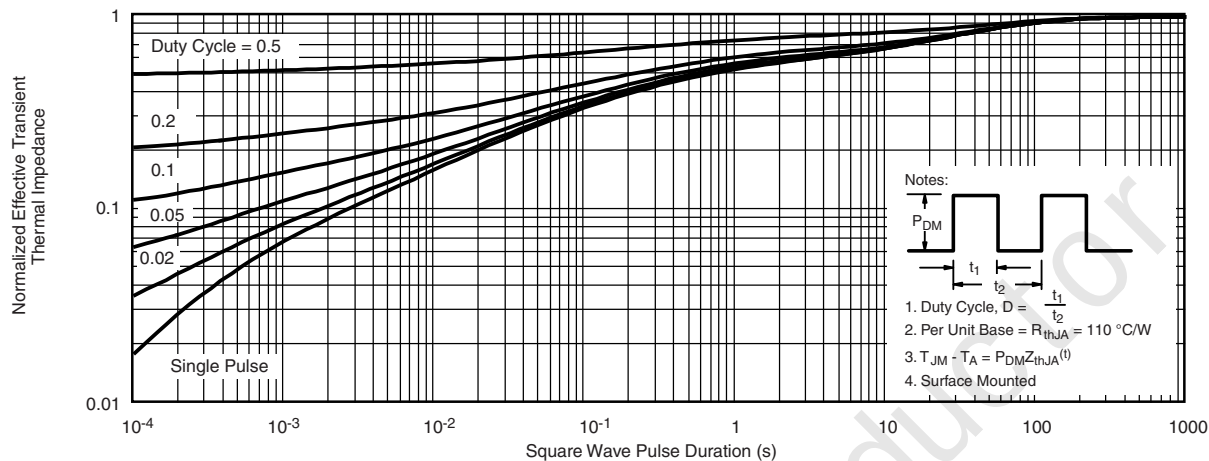
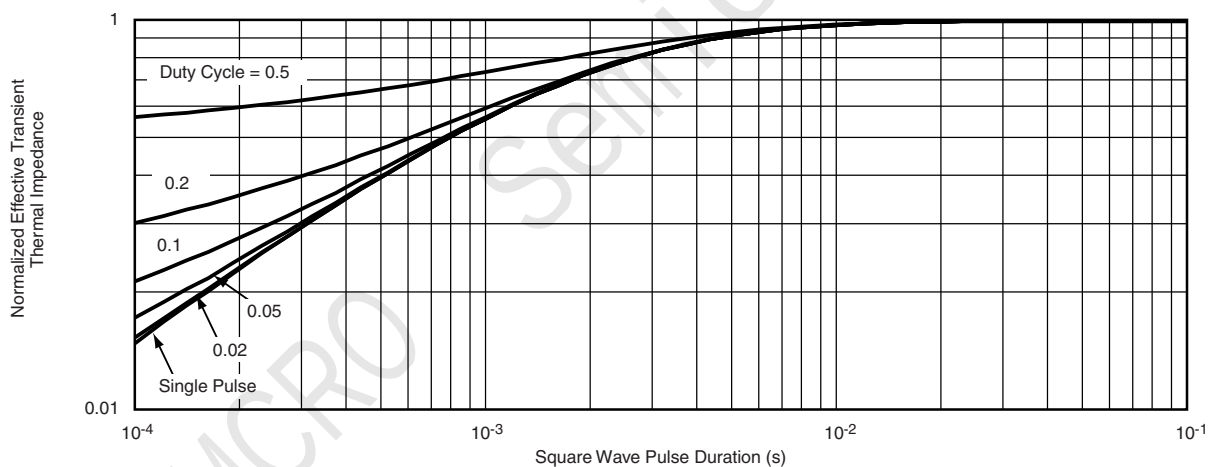


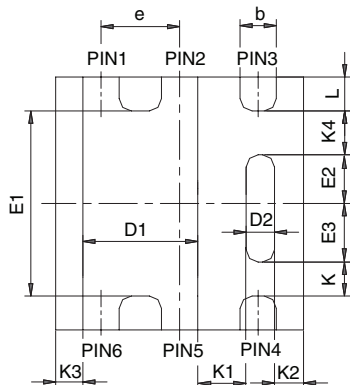
Current Derating*



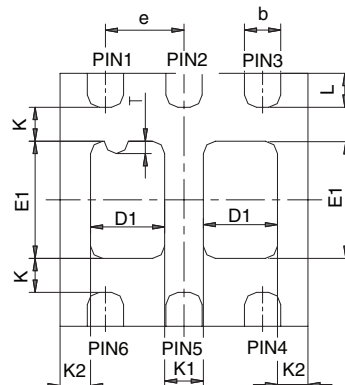
Power Derating

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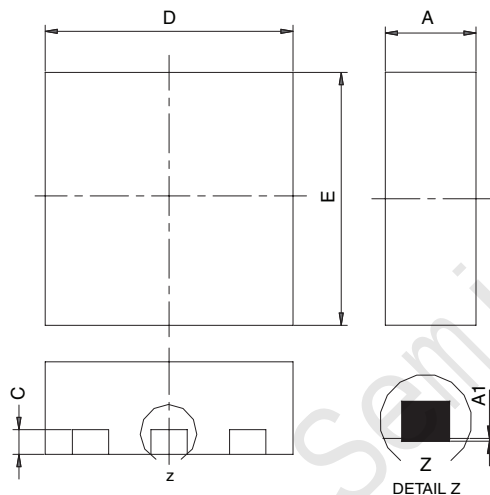
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Normalized Thermal Transient Impedance, Junction-to-Ambient

Normalized Thermal Transient Impedance, Junction-to-Case



BACKSIDE VIEW OF SINGLE



BACKSIDE VIEW OF DUAL



Notes:

1. All dimensions are in millimeters
2. Package outline exclusive of mold flash and metal burr
3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C-07431 – Rev. C, 06-Aug-07												
DWG: 5934												