

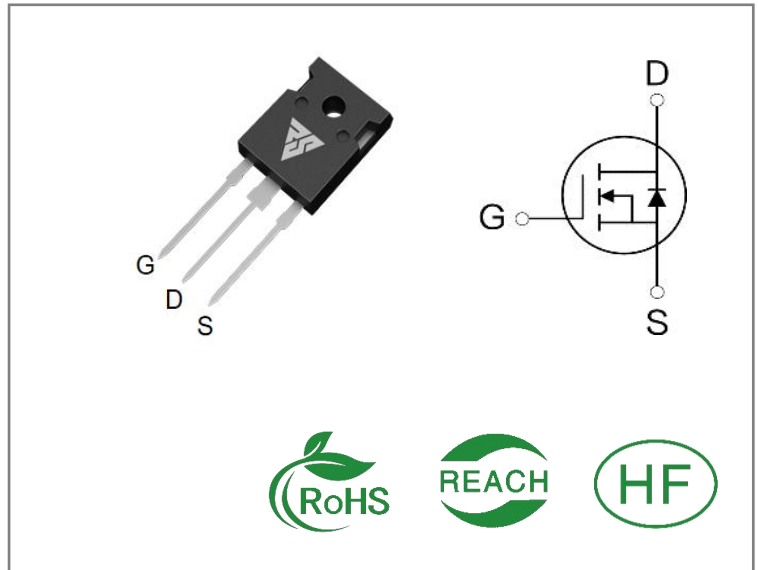
ID	$R_{DS(ON)}$ (Typ)	VDSS
28A	0.14 $\Omega$	500V

#### Applications:

- Switch Mode Power Supply(SMPS)
- Uninterruptible Power Supply (UPS)
- Power Factor Correction (PFC)

#### Features:

- Fast switching speed
- 100% avalanche tested
- Improved dv/dt capability



#### Ordering Information

Part Number	Package	Marking	Packing	Qty.
RS28N50W	T0-247-3	RS28N50W	Tube	30 PCS

#### Absolute Maximum Ratings $T_c = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	RS28N50W	Units
VDSS	Drain-to-Source Voltage	500	V
ID	Continuous Drain Current $T_C = 25^\circ\text{C}$	28	A
ID	Continuous Drain Current $T_C = 100^\circ\text{C}$	15	
IDM	Pulsed Drain Current (Note*1)	112	
PD	Power Dissipation	120	W
VGS	Gate- to- Source Voltage	$\pm 30$	V
EAS	Single Pulse Avalanche Engergy $L = 10\text{mH}$ , $V_{DD} = 50\text{V}$ , $R_G = 25\Omega$	520	mJ
TL TPKG	Maximum Temperature for Soldering	300 260	$^\circ\text{C}$
	Leads at 0.063in(1.6mm)from Case for 10 seconds		
	Package Body for 10 seconds		
TJ and TSTG	Operating Junction and Storage Temperature Range	-55 to 150	

\* Drain Current Limited by Maximum Junction Temperature

Caution: Stresses greater than those listed in the“ Absolute Maximum Ratings” Table may cause permanent damage to the device.

### Thermal Resistance

Symbol	Parameter	RS28N50W	Units	Test Conditions
R $\theta$ JC	Junction-to-Case	0.29	$^{\circ}\text{C} / \text{W}$	Drain lead soldered to water cooled heatsink, PD adjusted for a peak junction temperature of + 150 $^{\circ}\text{C}$
R $\theta$ JA	Junction-to-Ambient	62		1 cubic foot chamber, free air.

### OFF Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BVDSS	Drain- to- source Breakdown Voltage	500	--	--	V	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$
IDSS	Drain- to- Source Leakage Current	--	--	1	$\mu\text{A}$	$V_{DS}=500\text{V}, V_{GS}=0\text{V}$
IGSS	Gate- to- Source Forward Leakage	--	--	100	nA	$V_{GS}=30\text{V}, V_{DS}=0\text{V}$
	Gate- to- Source Reverse Leakage	--	--	-100		$V_{GS}=-30\text{V}, V_{DS}=0\text{V}$

### ON Characteristics $T_J = 25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
RDS(on)	Static Drain- to- Source On-Resistance(Note*2)	--	0.14	0.18	$\Omega$	$V_{GS}=10\text{V}, I_D=14\text{A}$
VGS(TH)	Gate Threshold Voltage	3	--	4	V	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$

### Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
td(ON)	Turn- on Delay Time	--	66	--	nS	$V_{DS}=250\text{V}$ $I_D=28\text{A}$ $R_G=25\Omega$
trise	Rise Time	--	59	--		
td(OFF)	Turn- OFF Delay Time	--	427	--		
tfall	Fall Time	--	108	--		

**Dynamic Characteristics** Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Ciss	Input Capacitance	--	4295	--	pF	VGS=0V VDS=25V f=1.0MHz
Coss	Output Capacitance	--	450	--		
Crss	Reverse Transfer Capacitance	--	32	--		
Qg	Total Gate Charge	--	22	--	nC	VDS=400V ID=28A VGS=10V
Qgs	Gate- to- Source Charge	--	4	--		
Qgd	Gate-to-Drain(" Miller") Charge	--	13	--		

**Source- Drain Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
IS	Continuous Source Current	--	--	28	A	Integral pn- diode in MOSFET
ISM	Maximum Pulsed Current	--	--	112	A	
VSD	Diode Forward Voltage	--	--	1.4	V	IS=14A,VGS=0V
trr	Reverse Recovery Time	--	482	--	nS	VGS=0V IS=14A,di/dt=100 A/μs
Qrr	Reverse Recovery Charge	--	7.6	--	μC	

**Notes:**

- \* 1. Repetitive rating, pulse width limited by maximum junction temperature.
- \* 2. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty Cycle  $\leq 1\%$

Typical Feature Curve

Figure 1. Output Characteristics ( $T_J = 25^\circ\text{C}$ )

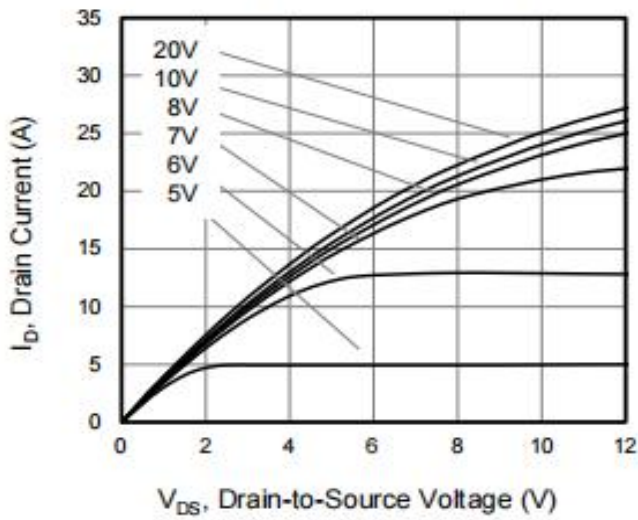


Figure 2. Body Diode Forward Voltage

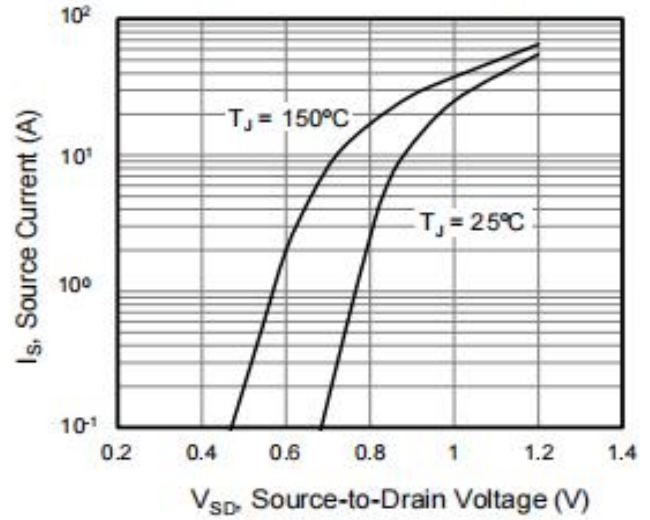


Figure 3. Drain Current vs. Temperature

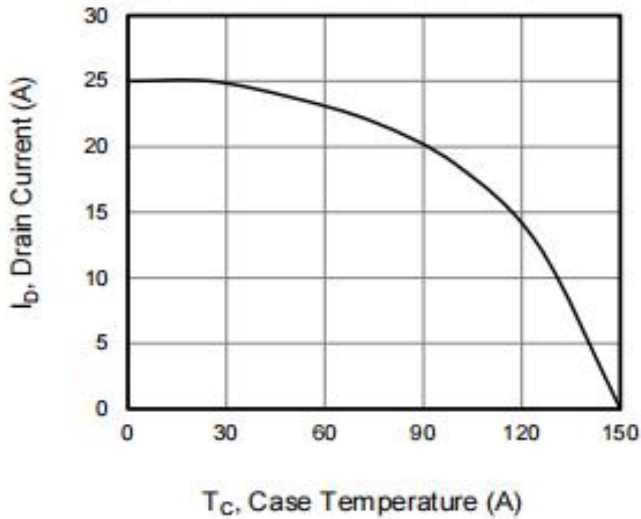


Figure 4.  $BV_{DSS}$  Variation vs. Temperature

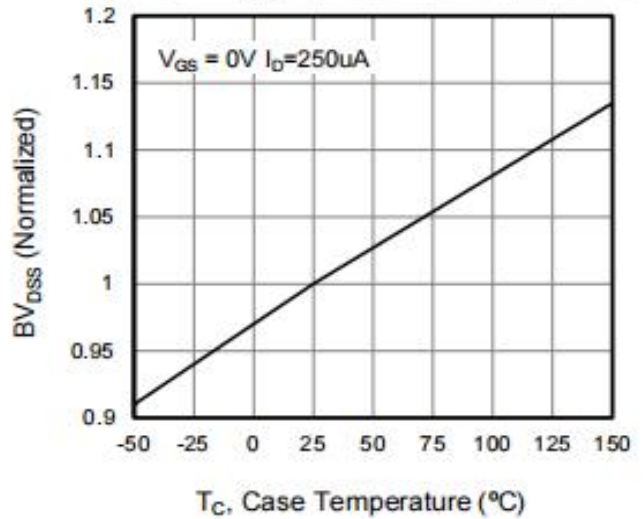


Figure 5. Transfer Characteristics

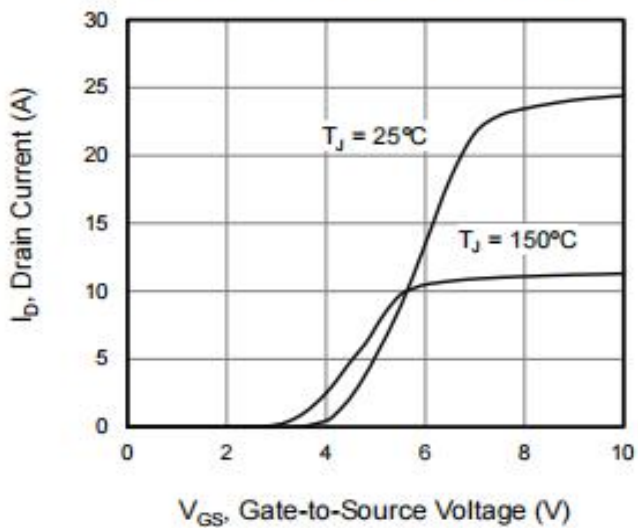
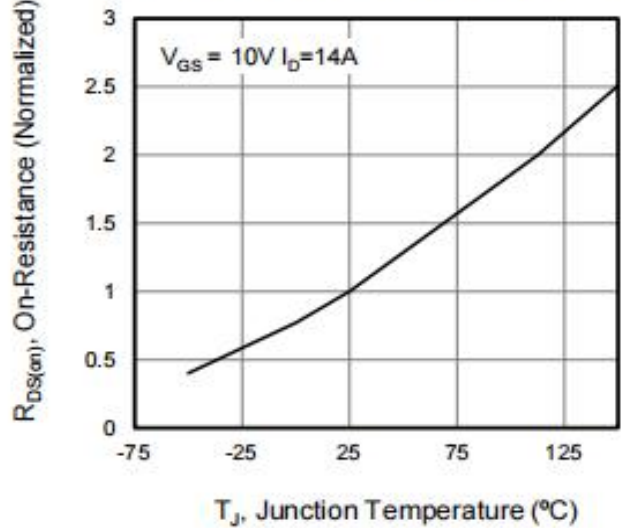
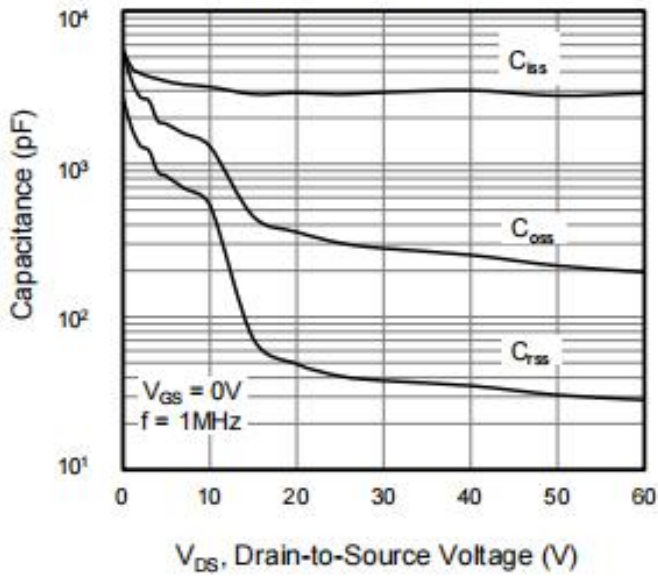


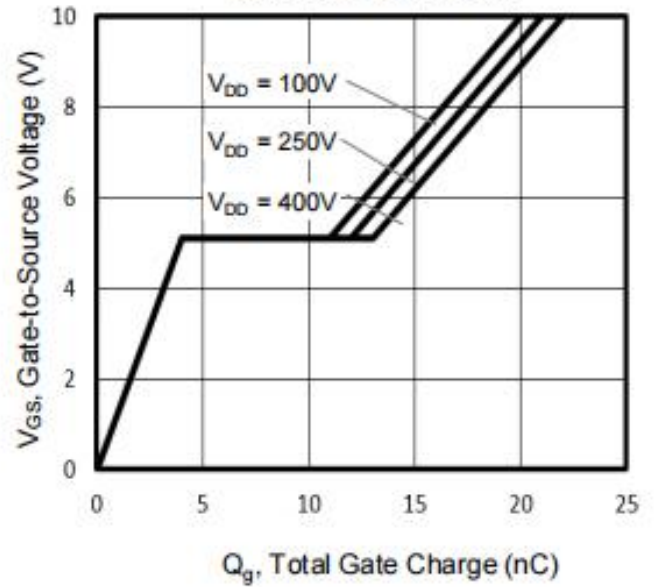
Figure 6. On-Resistance vs. Temperature



**Figure 7. Capacitance**

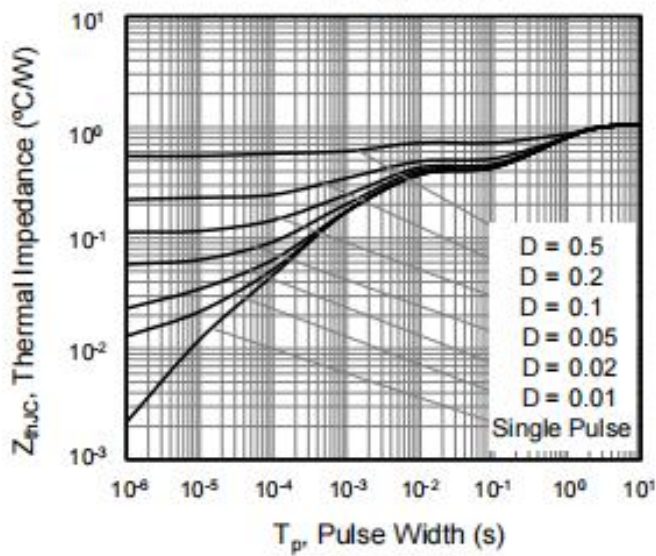


**Figure 8. Gate Charge**



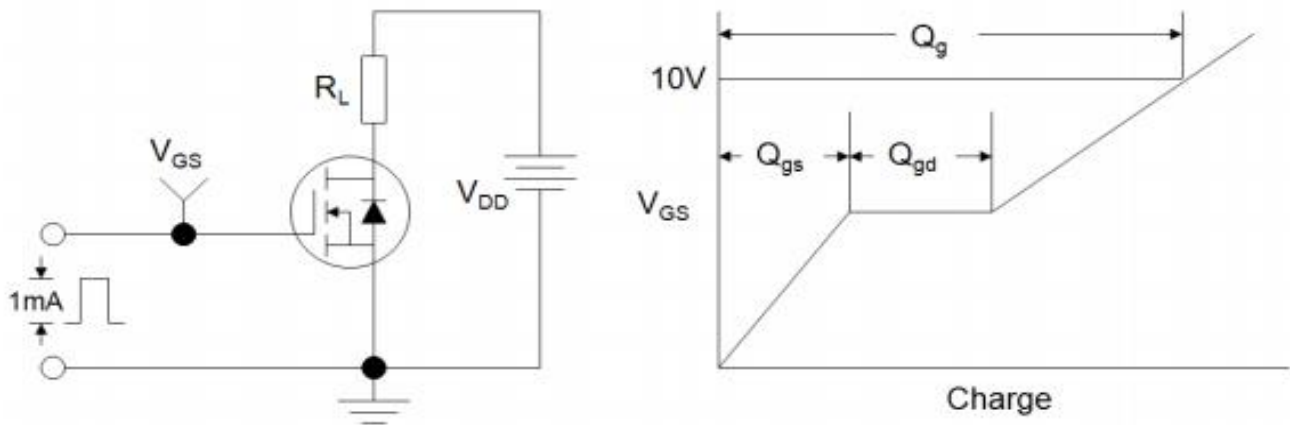
**Figure 9. Transient Thermal Impedance**

**TO-247/TO-3P**

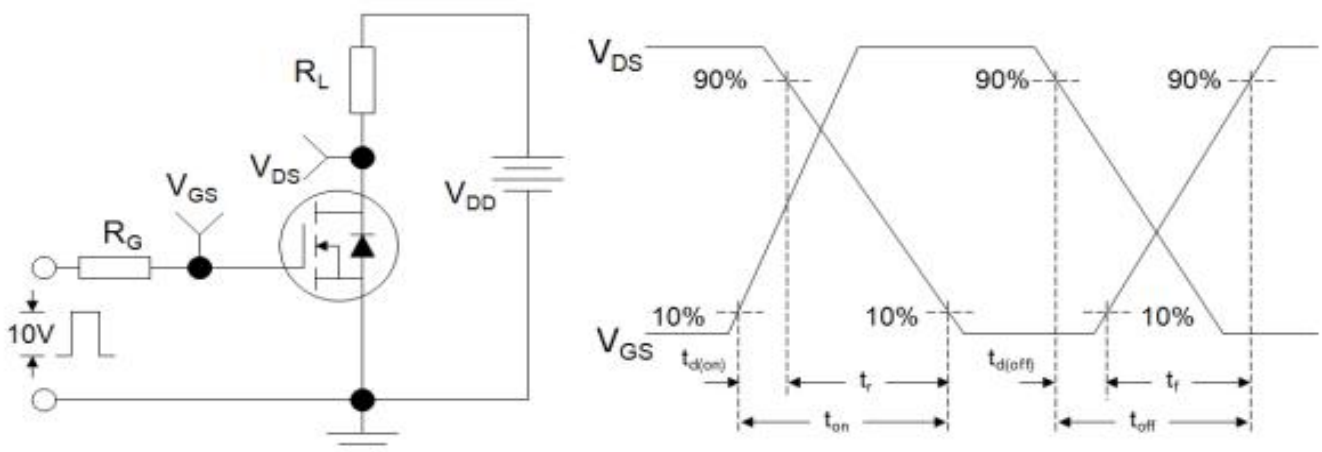


## Test Circuits and Waveforms

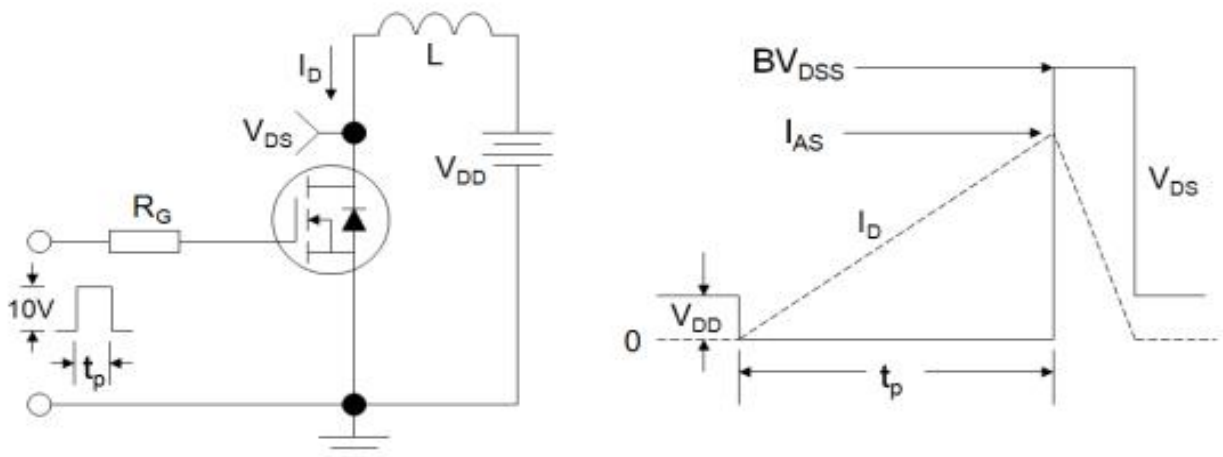
**Figure A: Gate Charge Test Circuit and Waveform**



**Figure B: Resistive Switching Test Circuit and Waveform**

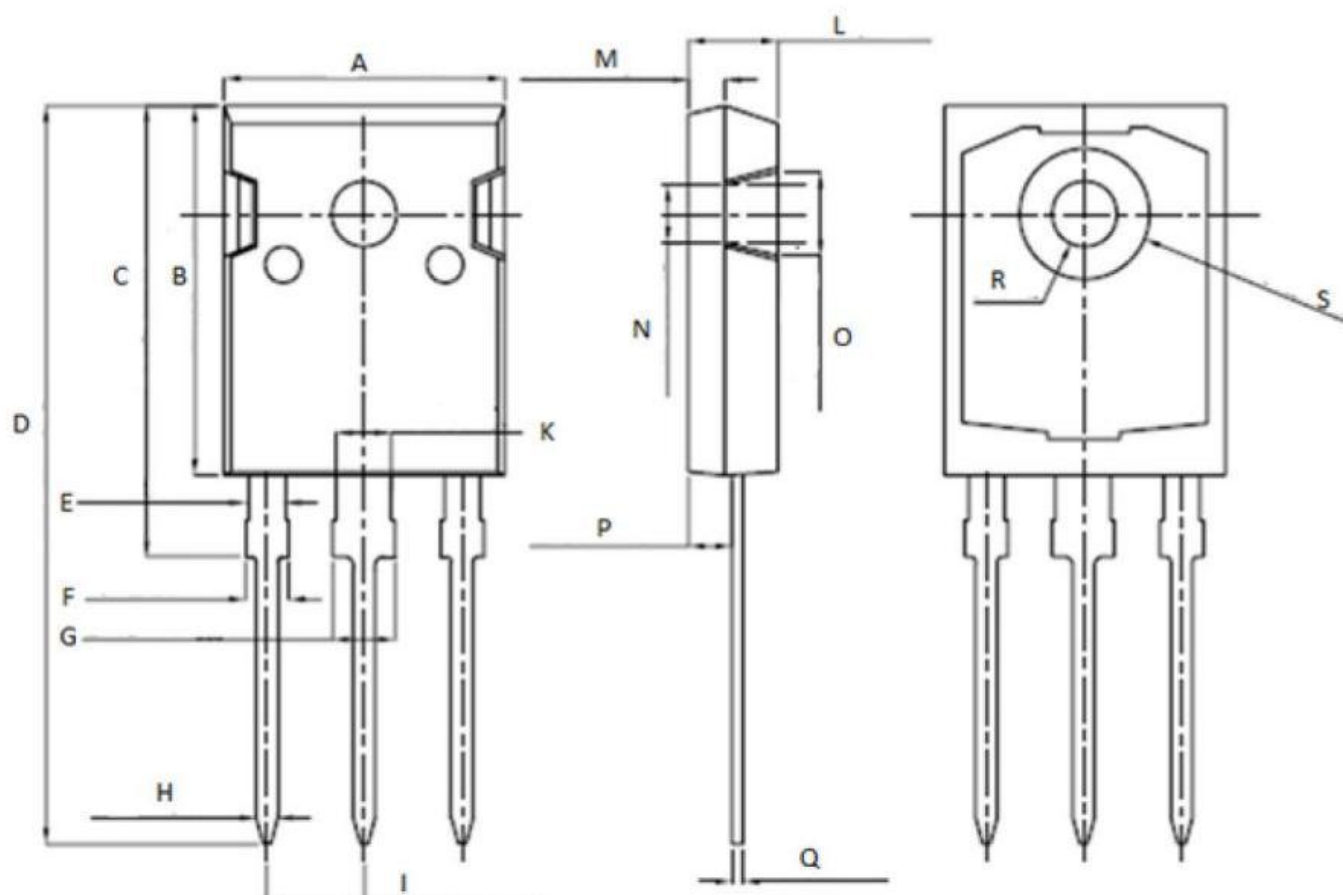


**Figure C: Unclamped Inductive Switching Test Circuit and Waveform**





**Package outline drawing(TO-247 Unit: mm )**



Unit: mm		
Symbol	Min.	Max.
A	15.95	16.25
B	20.85	21.25
C	20.95	21.35
D	40.5	40.9
E	1.9	2.1
F	2.1	2.25
G	3.1	3.25
H	1.1	1.3
I	5.40	5.50

Unit: mm		
Symbol	Min.	Max.
K	2.90	3.10
L	4.90	5.30
M	1.90	2.10
N	4.50	4.70
O	5.40	5.60
P	2.29	2.49
Q	0.51	0.71
R	φ 3.5	φ 3.7
S	φ 7.1	φ 7.3

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