PSoC™ Automotive Multitouch Generation 6XL Hybrid In-cell

Datasheet

Features

- In-Cell touchscreen controller
- Multitouch capacitive touchscreen controller
  - 32-bit Arm® Cortex® CPU
  - Register-configurable
  - Noise-suppression technologies for display and EMI
    - AutoArmor improves both electromagnetic emissions and immunity
  - Water rejection and wet-finger tracking using DualSense
  - Multitouch glove with automatic mode switching
    - Ten fingers with thin glove (≤ 1 mm thick)
    - Two fingers with thick glove (≤ 5 mm thick)
  - Fingernail tracking
  - Large object rejection
  - Automatic baseline tracking to environmental changes
  - Field upgrades via bootloader
  - Manufacturing Test Kit (MTK)
  - Touchscreen sensor self-test
- System performance (configuration dependent)
  - Screen sizes up to 15-inch diagonal
    - 6.0 mm electrode pitch; 16:10 aspect ratio
  - Up to 54 RX channels, 1836 intersections; 16:10 aspect ratio (34 TX × 54 RX)
  - Reports up to ten fingers
  - Small finger support down to 5 mm
  - Refresh rate up to 250 Hz; other rates configurable
- Power (configuration-dependent)
  - 1.71 V to 1.95 V and 3.0 V to 5.5 V logic and digital I/Os supply
  - 3.0 V to 5.5 V analog supply
  - 30 mW average power
  - 30 µW typical deep-sleep power
- Sensor and system design (configuration-dependent)
  - Supports In-Cell sensors
    - TX/VCOM share the same layer
    - RX ITO layer on/above the color filter
- Communication interface
  - I^2C slave at 100 and 400 kbps
- Package
  - 100-pin TQFP 14 × 14 × 1.4 mm (0.5-mm pitch)
- Ambient temperature range
  - Automotive-A: –40°C to 85°C
  - Automotive-S: –40°C to 105°C

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1 Touchscreen System overview

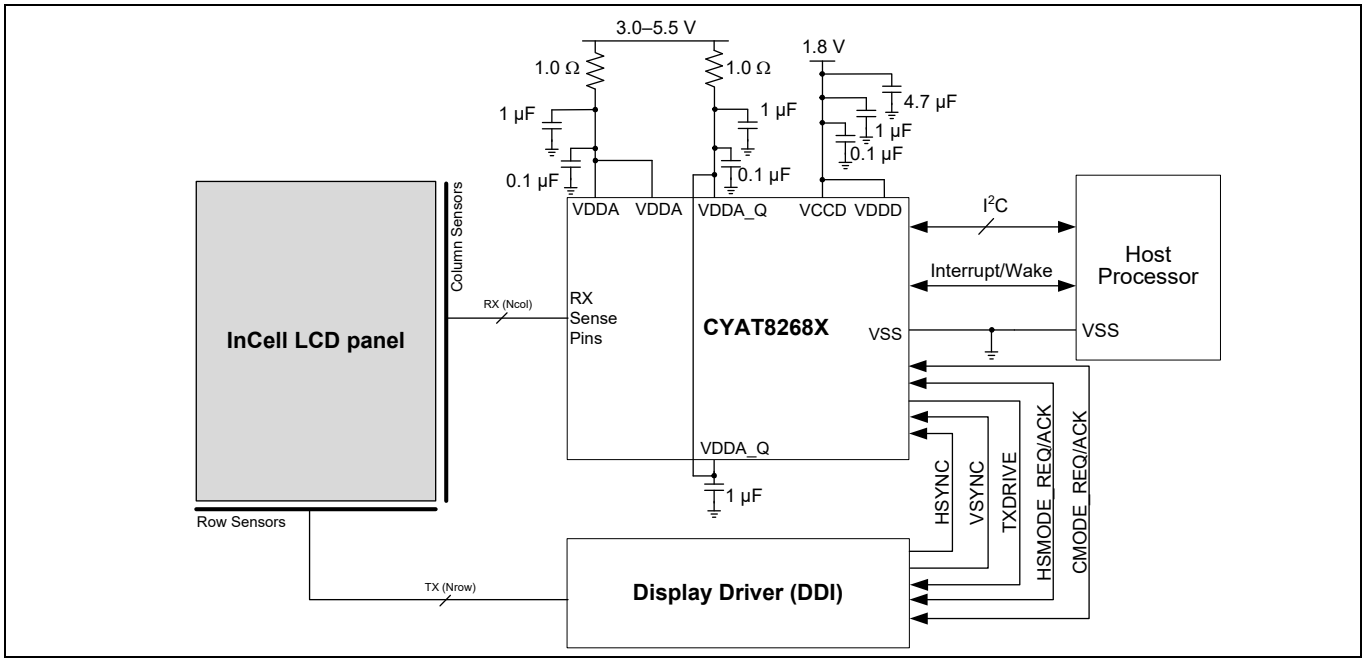


Figure 1 CYAT8268X typical system diagram

2 CYAT8268X overview

A capacitive touchscreen detects changes in capacitance to determine the location of one or more fingers on the surface of the touchscreen. A typical touchscreen system consists of a capacitive touchscreen sensor, an FPC bonded to the sensor, and the touchscreen controller mounted on the FPC. The FPC connects the touchscreen controller to the host processor. Users can interact with the displayed user interface through finger movements and gestures on the surface of the touchscreen.

CYAT8268X is a capacitive touchscreen controller with the sensing and processing technology to resolve the locations and report the positions of up to ten fingers on the touchscreen. The touchscreen controller converts an array of sensor capacitances into an array of digital values, which are processed by touch-detection and position-resolution algorithms in the controller. These algorithms determine the location and signal magnitude of each finger on the touchscreen.

Infineon provides:

- Application firmware
- Design guidance for the sensor and FPC
- Touchscreen sensor MTK

The CYAT8268X functional block diagram is shown in **Figure 2**. This device contains a high-performance Arm® 32-bit CPU with an integrated hardware multiply unit. This CPU controls all sensing and processing of measured capacitance results to allow tracking and reporting touches. The controller is optimized for low power and fast response time, with built-in support for manufacturing test. The touchscreen controller communicates with a host through an I^2C slave interface at up to 400 kbps.

CYAT8268X collects the touchscreen sensor information using the touch subsystem.

Touchscreen subsystem communicates with the external display driver (DDI) to enable TX drive in the embedded display lines and receives signals from RX sensors through the RX channels of the touchscreen controller. Therefore the capacitive scan is executed synchronously with the display refresh.

Infineon reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@cypress.com**.

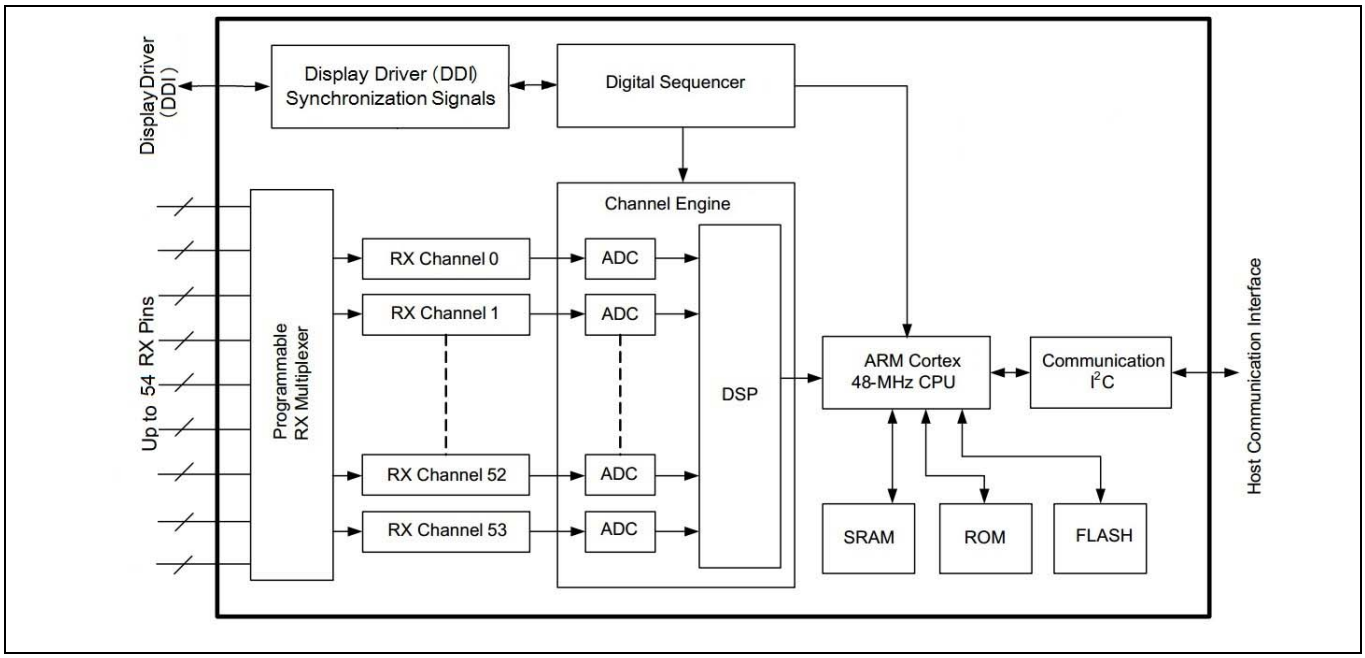


Figure 2 CYAT8268X functional block diagram

3 Features overview

3.1 AutoArmor

AutoArmor improves both electromagnetic emissions and immunity. It ensures no false finger touches when CYAT8268X is exposed to electromagnetic waves.

3.2 Water rejection

Water droplets can cause false touches to be reported. However, CYAT8268X continues to operate in the presence of water droplets or condensation. CYAT8268X enables water rejection using DualSense, Infineon's patented self- and mutual-capacitance sensing ability.

3.3 Wet-finger tracking

In a touchscreen system, moisture on fingers can cause false touches to be reported and make tracking of fingers across the screen difficult. CYAT8268X can detect and track fingers that are wet and enable more robust functionality of the touchscreen, using DualSense. This includes sweaty fingers touching the screen or fingers moving across a mist-covered screen.

3.4 Glove

CYAT8268X detects and tracks gloved fingers. Glove support allows navigating the touchscreen without having to remove gloves or without the use of expensive conductive gloves. Tracking of gloved fingers is supported by automatic mode switching, which automatically transitions between tracking gloved fingers and other touch-tracking modes. Ten-finger glove-touch is supported for thin gloves (≤ 1 mm thick) and two-finger operation is supported for thick gloves (≤ 5 mm thick).

3.5 Automatic Mode switching

CYAT8268X supports automatic mode switching which detects and tracks a new touch object type without requiring manual selection of the touch type from the user. Automatic mode switching allows an uninterrupted user experience when switching between a bare finger, gloved finger, fingernail, or wet finger.

3.6 Large finger tracking

A well-designed touchscreen system must correctly report a large finger or thumb as only a single touch. If this is not supported, a large finger can incorrectly be reported as two or more touches, hampering the user experience. When an object, such as a thumb, is pressed against the touchscreen sensor, CYAT8268X ensures that only one touch is reported at the center of the object.

3.7 Large object detection and rejection

It is important to be able to detect the presence of a large object on the touchscreen sensor. Common example is a palm touching the screen when typing. CYAT8268X can determine the presence of a large object, such as a fist or palm, from the touchscreen data. This presence may either be rejected or reported to the host.

4 Touchscreen System specifications

This section specifies the touchscreen system performance delivered by CYAT8268X. For definitions, justification of parameters, and test methodologies, refer to the Infineon specification ***PSoC™ Automotive Multitouch Touchscreen Controller User Interface Performance Definitions*** **(001-49389)**[1].

4.1 System Performance specifications

The system performance specifications in **Table 1**[2] and **Table 2**[3] are valid under these conditions: –40°C ≤ T_A ≤ 85°C[4] for Grade-A devices, –40°C ≤ T_A ≤ 105°C[4] for Grade-S devices; 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, 3.0 V ≤ V_{DDA} ≤ 5.5 V, unless otherwise noted. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core low dropout regulator (LDO) disabled, and V_{DDA} = 3 V, unless otherwise noted. Data is validated using a 10.1-inch sensor with 4.2 mm electrode pitch. Contact your local Infineon sales representative for information on the system performance conditions to guarantee the specifications provided in **Table 1**. The performance conditions and specifications are valid only for sensors approved by Infineon for use with CYAT8268X and produced by qualified Infineon partners. Contact **automotive@cypress.com** to discuss any deviations.

Table 1 Typical system performance specifications (Configuration dependent)

Category	Conditions	Core	Units
Accuracy	5–12 mm diameter finger	0.5	mm
	Glove (≤ 1 mm thick)	2	mm
	Glove (1 < thick ≤ 5 mm)	4	mm
Linearity	5–12 mm diameter finger	0.25	mm
	Glove (≤ 1 mm thick)	2	mm
	Glove (1< thick ≤ 5 mm)	4	mm

Notes

1. Infineon reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@cypress.com**.
2. Typical, as represented by 85% of the sample data measured. Accuracy is measured at points across the entire panel at 1.1-mm intervals. Linearity is measured on lines drawn across the panel (vertically, horizontally, and diagonally) separated by 1.1 mm.
3. Typical, as represented by the average values from the Infineon specification, *PSoC™ Automotive Multitouch Touchscreen Controller User Interface Performance Definitions* (001-49389).
4. System performance specifications are dependent on the combination of touchscreen controller, display, touchscreen, and environment noise and temperature. Infineon guarantees the performance of the touchscreen controller over this temperature range, but system performance may be impacted by the response of these other elements.

Table 2 System performance specifications (Configuration dependent)

Category	Description	Conditions	Min	Typ	Max	Units
Jitter	Delta in reported X, Y position, for non-moving finger	5–12 mm diameter finger	–	0.4	–	mm
Refresh rate	–	One finger on panel	100	120	250[5]	Hz
Response time	Active response time	First finger down	–	–	30	ms
Power	In Active state	1 finger, 120-Hz refresh rate	–	–	120	mW
	Average power[6]	Active state for 25% of touch activity and in Deep Sleep state for 75% of touch activity.	–	30	–	mW
	In Deep Sleep state	–	–	30	–	µW

Notes
5. Requires setting TX pulses for mutual-cap and self-cap to 8 and no noise in the environment.
6. Average power is the power consumed during the Active and Deep Sleep states, and is calculated using this equation: 0.25 × 120 mW + 0.75 × 0.030 mW = 30 mW.

5 Power supply information

CYAT8268X contains five external power domains: VDDA, VDDA_Q, VDDD, and VCCD. VDDA supplies power to the chip's TX pump and drivers. VDDA_Q supplies power to the RX analog circuitry. VDDD supplies power to the digital I/Os, core LDO regulator, supply monitors, and external reset circuitry (XRES). VCCD supplies power to the CPU core, and may be configured as an input or output, depending on if a 1.71–1.95-V V_{DDD} supply is used.

5.1 Required external components

The touch controller device requires external components for proper device operation. Quantities are dependent on the power supply configuration used. External capacitors require an X5R dielectric characteristic or better. It is recommended to use an X7R dielectric characteristic or better for high-frequency 0.1-µF/0.22-µF capacitors.

VDDA:

- 1.0-Ω, 5% tolerance resistor
- 0.1-µF capacitor
- 1-µF capacitor

VDDA_Q:

- 0.1-µF capacitor (only required on one of the VDDA_Q pins)
- Two 1.0-µF capacitors (one at each end of the package)
- 1.0-Ω, 5% tolerance resistor

VDDD:

- 1-µF capacitor if VCCD and VDDD are connected (shown in **Figure 3** and **Figure 4**) or 0.1-µF capacitor if VDDD ≥ 3.0 V.

VCCD:

- 1-µF capacitor if VCCD and VDDD are connected (shown in **Figure 3** and **Figure 4**)
- 100-nF capacitor

5.2 Voltage coefficient

The actual capacitance of external capacitors may be reduced with higher bias voltage. Check the capacitor datasheet for the voltage coefficient. Capacitors used for power supply decoupling or filtering are operated under a continuous DC-bias. Many capacitors used with DC power across them provide less than their target capacitance, and their capacitance is not constant across their working voltage range. When selecting capacitors for use with this device verify that the selected components provide the required capacitance under the specific operating conditions of temperature and voltage used in your design. While the temperature ratings of a capacitor are normally found as part of its catalog part number (for example, X7R, C0G, Y5V), the matching voltage coefficient may only be available on the component datasheet or direct from the manufacturer. Use of components that do not provide the required capacitance under the actual operating conditions may cause the device to perform to less than the datasheet specifications.

Power supply information

The available power configurations are shown.

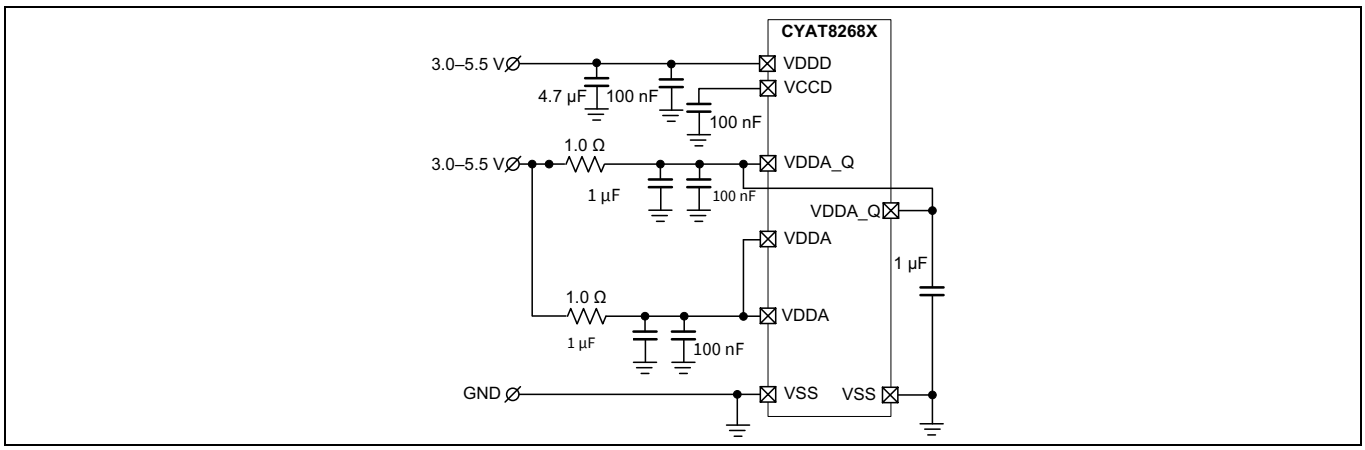


Figure 3 Dual supplies (no 1.8 V)

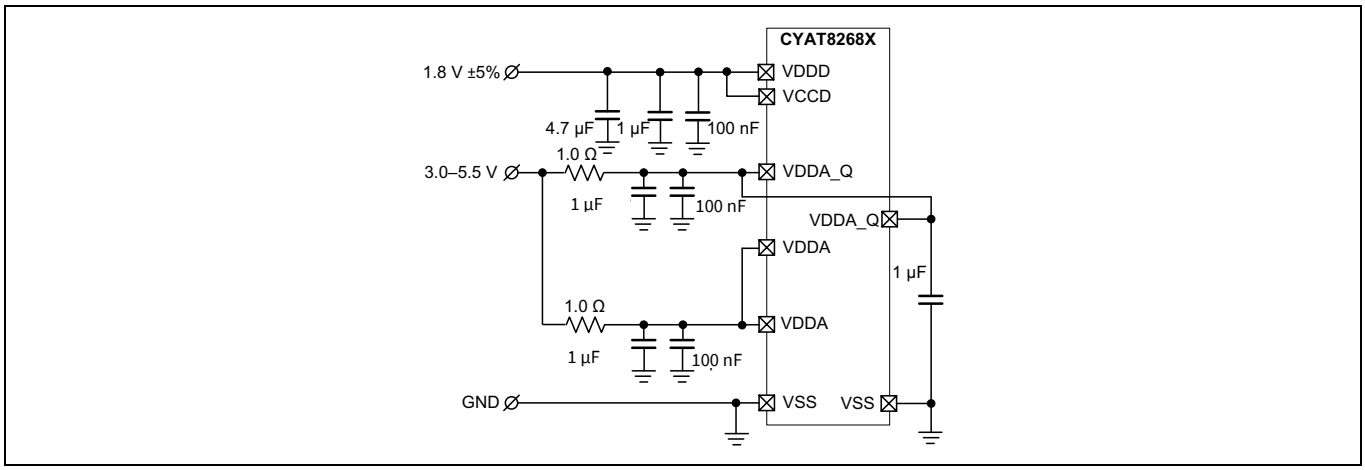


Figure 4 Dual supplies (inc. 1.8 V)

6 Pin information

CYAT8268X is available in 100-pin TQFP package. This section lists pin names, descriptions, and mappings to the physical package. Input and output pins may have more than one possible configuration. Guidance for each configuration option is provided below:

Y: Y pins may be configured as receive (RX) sense, allowing each design to be optimized based on the sensor pattern and layout. See Infineon specification, *PSoC™ Automotive Multitouch Touchscreen Controller Module Design Best Practices* (001-50467), for guidelines. Unused Y pins should be left unconnected. RX pins are tied to VSS internally during the Deep Sleep power state.

P0/P1/P2: Unused port 0, port 1, and port 2 pins should be left unconnected.

External Reset ($\overline{\text{XRES}}$): If the $\overline{\text{XRES}}$ pin is unused, it must be connected to V_{DDD} (either directly or through an external resistor).

SWD: Serial wire debug (SWD) is the recommended programming mode for all designs. If SWD is not used on the target board, use the bootloader to upgrade firmware.

Do Not Use (DNU): DNU pins must be left unconnected to ensure proper device operation.

COMM_INT: The COMM_INT pin is required. This interrupt pin is used for the host communication. If resistive mode is used, note that all I/Os are Hi-Z during chip initialization (after XRES or Bootloader Exit), so an additional external resistor is recommended.

Pin configurations: Multiple pin configurations are supported using Touch Tuning Host Emulator (TTHE) software. Pins are configured using the TTHE Pin Configuration Wizard.

Table 3 100-pin TQFP, 31 RX, CYAT8268X [7]

Pin No.	Name	Type		Description
		Digital	Analog	
1	Y12	–	I/O	RX channel 12
2	Y11	–	I/O	RX channel 11
3	Y10	–	I/O	RX channel 10
4	Y09	–	I/O	RX channel 9
5	Y08	–	I/O	RX channel 8
6	Y07	–	I/O	RX channel 7
7	Y06	–	I/O	RX channel 6
8	Y05	–	I/O	RX channel 5
9	Y04	–	I/O	RX channel 4
10	Y03	–	I/O	RX channel 3
11	Y02	–	I/O	RX channel 2
12	Y01	–	I/O	RX channel 1
13	Y00	–	I/O	RX channel 0
14	DNU	–	–	Do not use
15	DNU	–	–	Do not use
16	DNU	–	–	Do not use
17	DNU	–	–	Do not use
18	DNU	–	–	Do not use
19	DNU	–	–	Do not use
20	DNU	–	–	Do not use
21	DNU	–	–	Do not use
22	DNU	–	–	Do not use
23	DNU	–	–	Do not use
24	DNU	–	–	Do not use
25	DNU	–	–	Do not use
26	DNU	–	–	Do not use
27	DNU	–	–	Do not use
28	VSS	Power		Connect to ground
29	$\overline{\text{XRES}}$	I	–	External active LOW reset
30	P0[0]	I/O	–	I2C SCL
31	P0[1]	I/O	–	I2C SDA
32	P1[0]	I/O	–	HSMODE_REQ (Request High Sensitivity Mode - lower touch refresh rate - output)
33	P1[1]	I/O	–	HSYNC (Horizontal Timing signal - input)
34	P1[2]	I/O	–	TXDRIVE (Drive TX signal hi/lo - output)

Note
7. See **"Pin information"** on page 10 for details on pin configuration.

Table 3 100-pin TQFP, 31 RX, CYAT8268X [7] (continued)

Pin No.	Name	Type		Description
		Digital	Analog	
35	P1[3]	I/O	–	VSYNC (Vertical blanking timing signal - input)
36	P1[4]	I/O	–	ERROR (Set high when internal error is detected - output)
37	P1[5]	I/O	–	HSMODE_ACK (Acknowledge High Sensitivity Mode - lower touch refresh rate - input)
38	P1[6]	I/O	–	COMM_INT
39	P2[0]	I/O	–	SWDIO / CMODE_REQ (Request Custom Mode - output)
40	P2[1]	I/O	–	SWDCLK / CMODE_ACK (Acknowledge Custom Mode - input)
41	VCCD	Power		Digital core power supply input/output
42	VDDD	Power		Digital power supply input
43	VSS	Power		Connect to ground
44	VSS	Power		Connect to ground
45	VDDA	Power		TX analog power supply input
46	VDDA_Q	Power		RX analog power supply input
47	VDDA	Power		TX analog power supply input
48	DNU	–	–	Do not use
49	DNU	–	–	Do not use
50	DNU	–	–	Do not use
51	DNU	–	–	Do not use
52	DNU	–	–	Do not use
53	DNU	–	–	Do not use
54	DNU	–	–	Do not use
55	DNU	–	–	Do not use
56	DNU	–	–	Do not use
57	DNU	–	–	Do not use
58	VSS	Power		Connect to ground
59	DNU	–	–	Do not use
60	DNU	–	–	Do not use
61	DNU	–	–	Do not use
62	DNU	–	–	Do not use
63	DNU	–	–	Do not use
64	DNU	–	–	Do not use
65	DNU	–	–	Do not use
66	DNU	–	–	Do not use
67	DNU	–	–	Do not use
68	DNU	–	–	Do not use
69	DNU	–	–	Do not use

Note
7. See **"Pin information"** on page 10 for details on pin configuration.

Table 3 100-pin TQFP, 31 RX, CYAT8268X [7] (continued)

Pin No.	Name	Type		Description
		Digital	Analog	
70	DNU	–	–	Do not use
71	DNU	–	–	Do not use
72	DNU	–	–	Do not use
73	DNU	–	–	Do not use
74	DNU	–	–	Do not use
75	DNU	–	–	Do not use
76	DNU	–	–	Do not use
77	DNU	–	–	Do not use
78	DNU	–	–	Do not use
79	DNU	–	–	Do not use
80	DNU	–	–	Do not use
81	Y30	–	I/O	RX channel 30
82	Y29	–	I/O	RX channel 29
83	Y28	–	I/O	RX channel 28
84	Y27	–	I/O	RX channel 27
85	VDDA_Q	Power		RX analog power supply input
86	VSS	Power		Connect to ground
87	Y26	–	I/O	RX channel 26
88	Y25	–	I/O	RX channel 25
89	Y24	–	I/O	RX channel 24
90	Y23	–	I/O	RX channel 23
91	Y22	–	I/O	RX channel 22
92	Y21	–	I/O	RX channel 21
93	Y20	–	I/O	RX channel 20
94	Y19	–	I/O	RX channel 19
95	Y18	–	I/O	RX channel 18
96	Y17	–	I/O	RX channel 17
97	Y16	–	I/O	RX channel 16
98	Y15	–	I/O	RX channel 15
99	Y14	–	I/O	RX channel 14
100	Y13	–	I/O	RX channel 13

Note
7. See **"Pin information"** on page 10 for details on pin configuration.

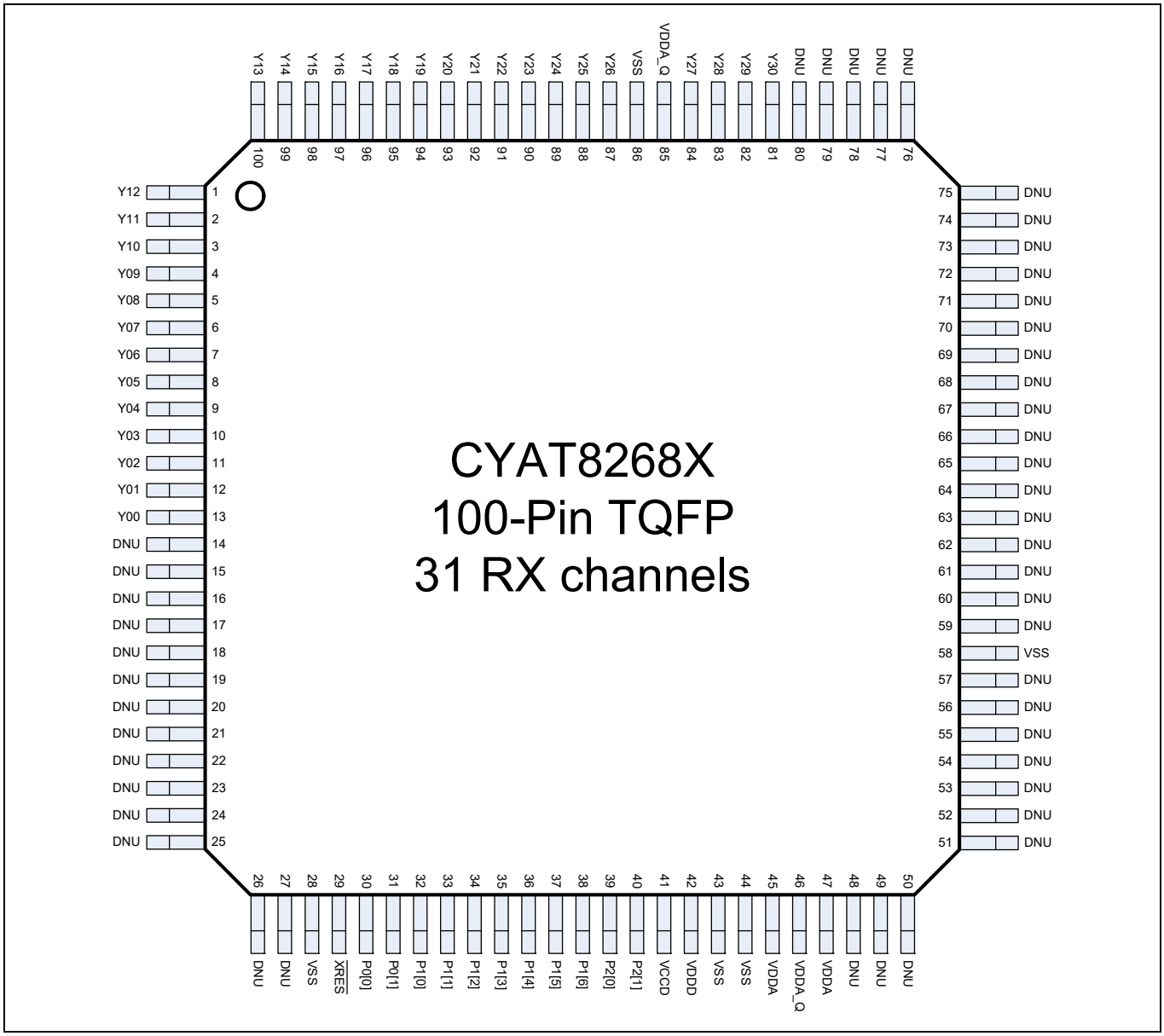


Figure 5 100-pin TQFP, 31 RX, CYAT8268X

Table 4 100-pin TQFP, 39 RX, CYAT8268X [8]

Pin No.	Name	Type		Description
		Digital	Analog	
1	Y12	–	I/O	RX channel 12
2	Y11	–	I/O	RX channel 11
3	Y10	–	I/O	RX channel 10
4	Y09	–	I/O	RX channel 9
5	Y08	–	I/O	RX channel 8
6	Y07	–	I/O	RX channel 7
7	Y06	–	I/O	RX channel 6
8	Y05	–	I/O	RX channel 5
9	Y04	–	I/O	RX channel 4
10	Y03	–	I/O	RX channel 3
11	Y02	–	I/O	RX channel 2
12	Y01	–	I/O	RX channel 1
13	Y00	–	I/O	RX channel 0
14	DNU	–	–	Do not use
15	DNU	–	–	Do not use
16	DNU	–	–	Do not use
17	DNU	–	–	Do not use
18	DNU	–	–	Do not use
19	DNU	–	–	Do not use
20	DNU	–	–	Do not use
21	DNU	–	–	Do not use
22	DNU	–	–	Do not use
23	DNU	–	–	Do not use
24	DNU	–	–	Do not use
25	DNU	–	–	Do not use
26	DNU	–	–	Do not use
27	DNU	–	–	Do not use
28	VSS	Power		Connect to ground
29	$\overline{\text{XRES}}$	I	–	External active LOW reset
30	P0[0]	I/O	–	I2C SCL
31	P0[1]	I/O	–	I2C SDA
32	P1[0]	I/O	–	HSMODE_REQ (Request High Sensitivity Mode - lower touch refresh rate - output)
33	P1[1]	I/O	–	HSYNC (Horizontal Timing signal - input)
34	P1[2]	I/O	–	TXDRIVE (Drive TX signal hi/lo - output)

Note
8. See **"Pin information"** on page 10 for details on pin configuration.

Table 4 100-pin TQFP, 39 RX, CYAT8268X [8] (continued)

Pin No.	Name	Type		Description
		Digital	Analog	
35	P1[3]	I/O	–	VSYNC (Vertical blanking timing signal - input)
36	P1[4]	I/O	–	ERROR (Set high when internal error is detected - output)
37	P1[5]	I/O	–	HSMODE_ACK (Acknowledge High Sensitivity Mode - lower touch refresh rate - input)
38	P1[6]	I/O	–	COMM_INT
39	P2[0]	I/O	–	SWDIO / CMODE_REQ (Request Custom Mode - output)
40	P2[1]	I/O	–	SWDCLK / CMODE_ACK (Acknowledge Custom Mode - input)
41	VCCD	Power		Digital core power supply input/output
42	VDDD	Power		Digital power supply input
43	VSS	Power		Connect to ground
44	VSS	Power		Connect to ground
45	VDDA	Power		TX analog power supply input
46	VDDA_Q	Power		RX analog power supply input
47	VDDA	Power		TX analog power supply input
48	DNU	–	–	Do not use
49	DNU	–	–	Do not use
50	DNU	–	–	Do not use
51	DNU	–	–	Do not use
52	DNU	–	–	Do not use
53	DNU	–	–	Do not use
54	DNU	–	–	Do not use
55	DNU	–	–	Do not use
56	DNU	–	–	Do not use
57	DNU	–	–	Do not use
58	VSS	Power		Connect to ground
59	DNU	–	–	Do not use
60	DNU	–	–	Do not use
61	DNU	–	–	Do not use
62	DNU	–	–	Do not use
63	DNU	–	–	Do not use
64	DNU	–	–	Do not use
65	DNU	–	–	Do not use
66	DNU	–	–	Do not use
67	DNU	–	–	Do not use
68	DNU	–	–	Do not use
69	DNU	–	–	Do not use

Note
8. See **"Pin information"** on page 10 for details on pin configuration.

Table 4 100-pin TQFP, 39 RX, CYAT8268X [8] (continued)

Pin No.	Name	Type		Description
		Digital	Analog	
70	DNU	–	–	Do not use
71	DNU	–	–	Do not use
72	DNU	–	–	Do not use
73	Y38	–	I/O	RX channel 38
74	Y37	–	I/O	RX channel 37
75	Y36	–	I/O	RX channel 36
76	Y35	–	I/O	RX channel 35
77	Y34	–	I/O	RX channel 34
78	Y33	–	I/O	RX channel 33
79	Y32	–	I/O	RX channel 32
80	Y31	–	I/O	RX channel 31
81	Y30	–	I/O	RX channel 30
82	Y29	–	I/O	RX channel 29
83	Y28	–	I/O	RX channel 28
84	Y27	–	I/O	RX channel 27
85	VDDA_Q	Power		RX analog power supply input
86	VSS	Power		Connect to ground
87	Y26	–	I/O	RX channel 26
88	Y25	–	I/O	RX channel 25
89	Y24	–	I/O	RX channel 24
90	Y23	–	I/O	RX channel 23
91	Y22	–	I/O	RX channel 22
92	Y21	–	I/O	RX channel 21
93	Y20	–	I/O	RX channel 20
94	Y19	–	I/O	RX channel 19
95	Y18	–	I/O	RX channel 18
96	Y17	–	I/O	RX channel 17
97	Y16	–	I/O	RX channel 16
98	Y15	–	I/O	RX channel 15
99	Y14	–	I/O	RX channel 14
100	Y13	–	I/O	RX channel 13

Note
8. See **“Pin information”** on page 10 for details on pin configuration.

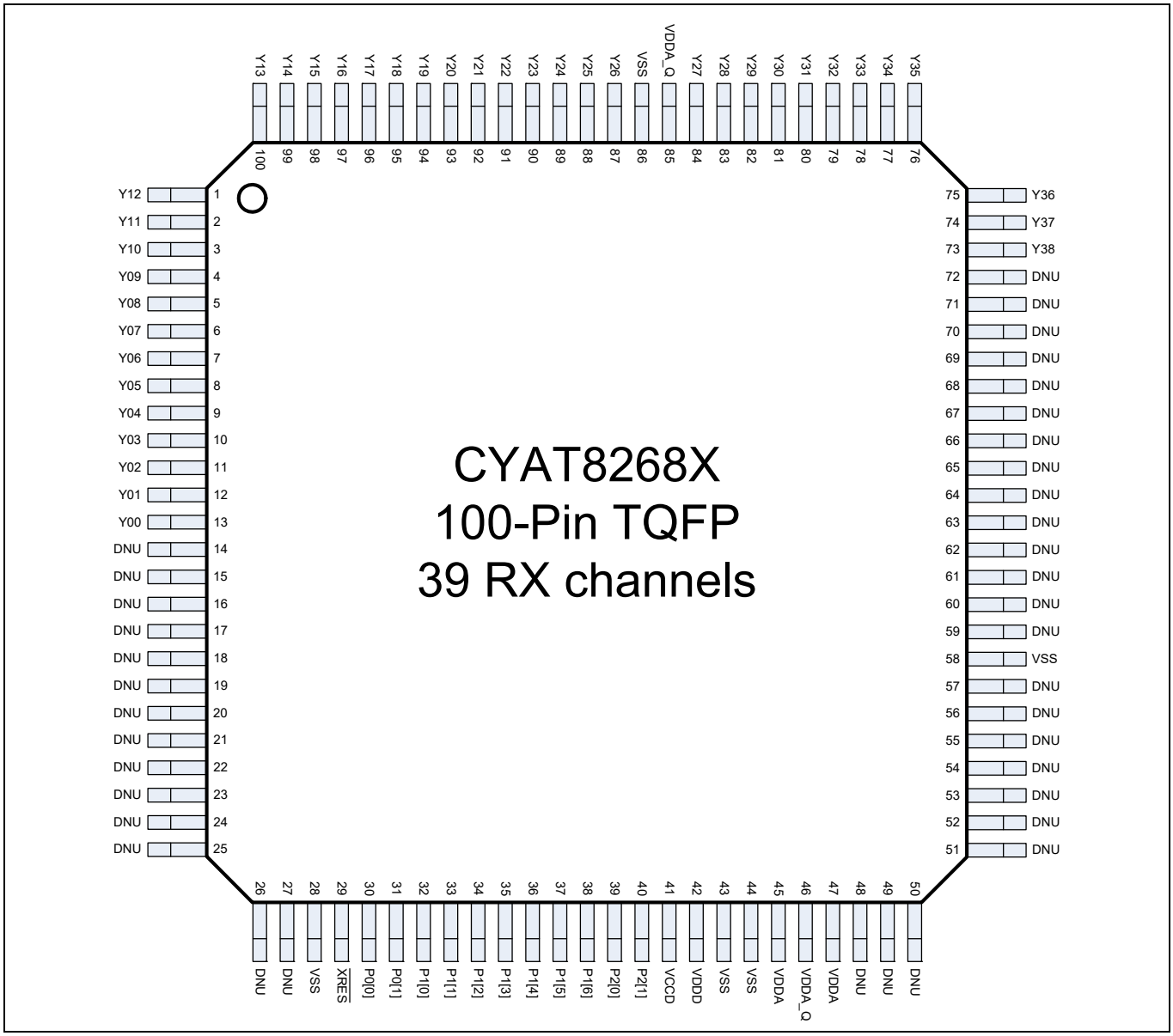


Figure 6 100-pin TQFP, 39 RX, CYAT8268X

Table 5 100-pin TQFP, 46 RX, CYAT8268X [9]

Pin No.	Name	Digital	Analog	Description
1	Y12	–	I/O	RX channel 12
2	Y11	–	I/O	RX channel 11
3	Y10	–	I/O	RX channel 10
4	Y09	–	I/O	RX channel 9
5	Y08	–	I/O	RX channel 8
6	Y07	–	I/O	RX channel 7
7	Y06	–	I/O	RX channel 6
8	Y05	–	I/O	RX channel 5
9	Y04	–	I/O	RX channel 4
10	Y03	–	I/O	RX channel 3
11	Y02	–	I/O	RX channel 2
12	Y01	–	I/O	RX channel 1
13	Y00	–	I/O	RX channel 0
14	DNU	–	–	Do not use
15	DNU	–	–	Do not use
16	DNU	–	–	Do not use
17	DNU	–	–	Do not use
18	DNU	–	–	Do not use
19	DNU	–	–	Do not use
20	DNU	–	–	Do not use
21	DNU	–	–	Do not use
22	DNU	–	–	Do not use
23	DNU	–	–	Do not use
24	DNU	–	–	Do not use
25	DNU	–	–	Do not use
26	DNU	–	–	Do not use
27	DNU	–	–	Do not use
28	VSS	Power		Connect to ground
29	$\overline{\text{XRES}}$	I	–	External active LOW reset
30	P0[0]	I/O	–	I2C SCL
31	P0[1]	I/O	–	I2C SDA
32	P1[0]	I/O	–	HSMODE_REQ (Request High Sensitivity Mode - lower touch refresh rate - output)
33	P1[1]	I/O	–	HSYNC (Horizontal Timing signal - input)
34	P1[2]	I/O	–	TXDRIVE (Drive TX signal hi/lo - output)
35	P1[3]	I/O	–	VSYNC (Vertical blanking timing signal - input)

Note
9. See **"Pin information"** on page 10 for details on pin configuration.

Table 5 100-pin TQFP, 46 RX, CYAT8268X [9] (continued)

Pin No.	Name	Digital	Analog	Description
36	P1[4]	I/O	–	ERROR (Set high when internal error is detected - output)
37	P1[5]	I/O	–	HSMODE_ACK (Acknowledge High Sensitivity Mode - lower touch refresh rate - input)
38	P1[6]	I/O	–	COMM_INT
39	P2[0]	I/O	–	SWDIO / CMODE_REQ (Request Custom Mode - output)
40	P2[1]	I/O	–	SWDCLK / CMODE_ACK (Acknowledge Custom Mode - input)
41	VCCD	Power		Digital core power supply input/output
42	VDDD	Power		Digital power supply input
43	VSS	Power		Connect to ground
44	VSS	Power		Connect to ground
45	VDDA	Power		TX analog power supply input
46	VDDA_Q	Power		RX analog power supply input
47	VDDA	Power		TX analog power supply input
48	DNU	–	–	Do not use
49	DNU	–	–	Do not use
50	DNU	–	–	Do not use
51	DNU	–	–	Do not use
52	DNU	–	–	Do not use
53	DNU	–	–	Do not use
54	DNU	–	–	Do not use
55	DNU	–	–	Do not use
56	DNU	–	–	Do not use
57	DNU	–	–	Do not use
58	VSS	Power		Connect to ground
59	DNU	–	–	Do not use
60	DNU	–	–	Do not use
61	DNU	–	–	Do not use
62	DNU	–	–	Do not use
63	DNU	–	–	Do not use
64	DNU	–	–	Do not use
65	DNU	–	–	Do not use
66	Y45	–	I/O	RX channel 45
67	Y44	–	I/O	RX channel 44
68	Y43	–	I/O	RX channel 43
69	Y42	–	I/O	RX channel 42
70	Y41	–	I/O	RX channel 41
71	Y40	–	I/O	RX channel 40

Note
9. See **"Pin information"** on page 10 for details on pin configuration.

Table 5 100-pin TQFP, 46 RX, CYAT8268X [9] (continued)

Pin No.	Name	Digital	Analog	Description
72	Y39	–	I/O	RX channel 39
73	Y38	–	I/O	RX channel 38
74	Y37	–	I/O	RX channel 37
75	Y36	–	I/O	RX channel 36
76	Y35	–	I/O	RX channel 35
77	Y34	–	I/O	RX channel 34
78	Y33	–	I/O	RX channel 33
79	Y32	–	I/O	RX channel 32
80	Y31	–	I/O	RX channel 31
81	Y30	–	I/O	RX channel 30
82	Y29	–	I/O	RX channel 29
83	Y28	–	I/O	RX channel 28
84	Y27	–	I/O	RX channel 27
85	VDDA_Q	Power		RX analog power supply input
86	VSS	Power		Connect to ground
87	Y26	–	I/O	RX channel 26
88	Y25	–	I/O	RX channel 25
89	Y24	–	I/O	RX channel 24
90	Y23	–	I/O	RX channel 23
91	Y22	–	I/O	RX channel 22
92	Y21	–	I/O	RX channel 21
93	Y20	–	I/O	RX channel 20
94	Y19	–	I/O	RX channel 19
95	Y18	–	I/O	RX channel 18
96	Y17	–	I/O	RX channel 17
97	Y16	–	I/O	RX channel 16
98	Y15	–	I/O	RX channel 15
99	Y14	–	I/O	RX channel 14
100	Y13	–	I/O	RX channel 13

Note
9. See **"Pin information"** on page 10 for details on pin configuration.

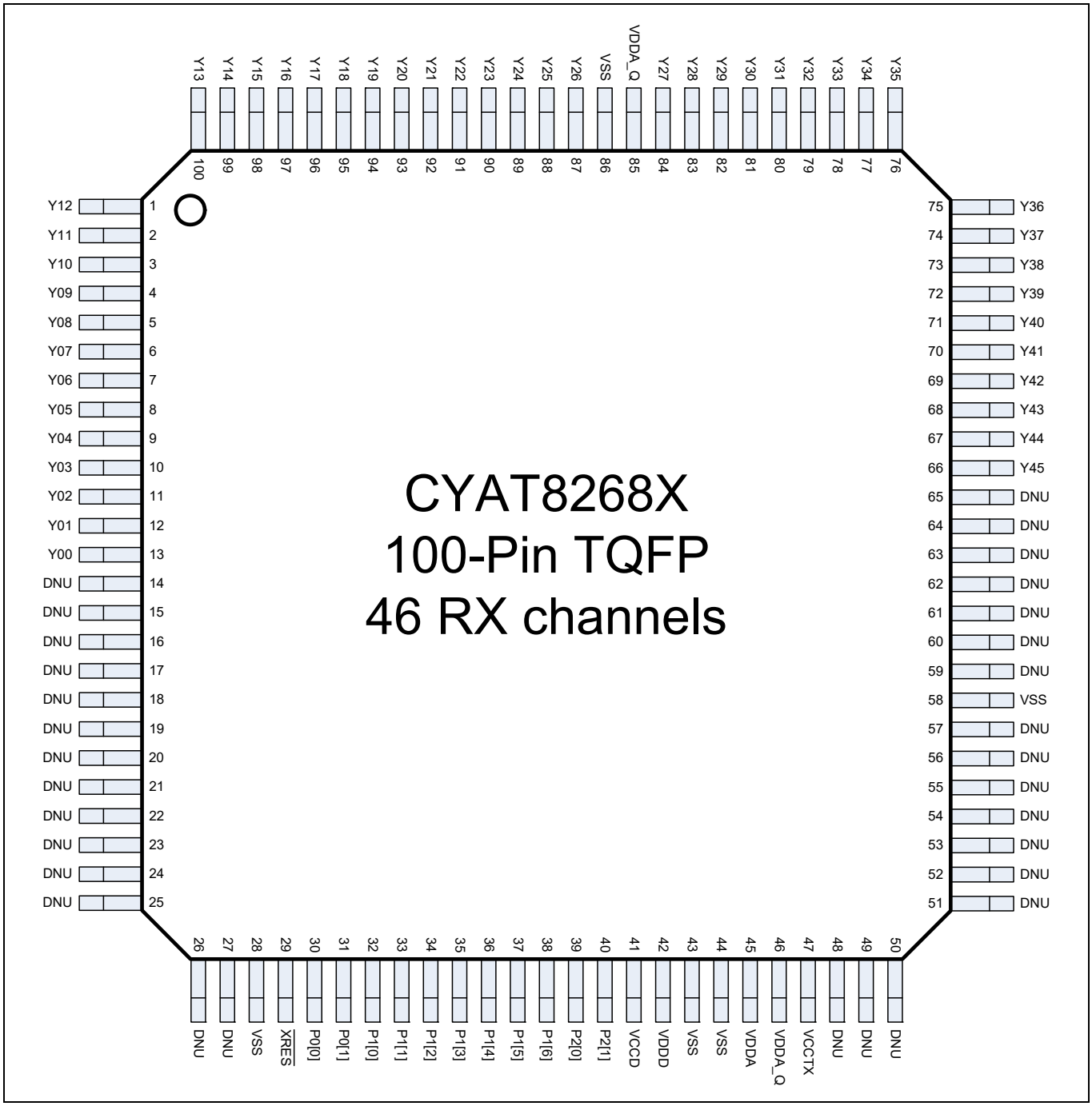


Figure 7 100-pin TQFP, 46 RX, CYAT8268X

Table 6 100-pin TQFP, 54 RX, CYAT8268X [10]

Pin No.	Name	Type		Description
		Digital	Analog	
1	Y12	–	I/O	RX channel 12
2	Y11	–	I/O	RX channel 11
3	Y10	–	I/O	RX channel 10
4	Y09	–	I/O	RX channel 9
5	Y08	–	I/O	RX channel 8
6	Y07	–	I/O	RX channel 7
7	Y06	–	I/O	RX channel 6
8	Y05	–	I/O	RX channel 5
9	Y04	–	I/O	RX channel 4
10	Y03	–	I/O	RX channel 3
11	Y02	–	I/O	RX channel 2
12	Y01	–	I/O	RX channel 1
13	Y00	–	I/O	RX channel 0
14	DNU	–	–	Do not use
15	DNU	–	–	Do not use
16	DNU	–	–	Do not use
17	DNU	–	–	Do not use
18	DNU	–	–	Do not use
19	DNU	–	–	Do not use
20	DNU	–	–	Do not use
21	DNU	–	–	Do not use
22	DNU	–	–	Do not use
23	DNU	–	–	Do not use
24	DNU	–	–	Do not use
25	DNU	–	–	Do not use
26	DNU	–	–	Do not use
27	DNU	–	–	Do not use
28	VSS	Power		Connect to ground
29	XRES	I	–	External active LOW reset
30	P0[0]	I/O	–	I2C SCL
31	P0[1]	I/O	–	I2C SDA
32	P1[0]	I/O	–	HSMODE_REQ (Request High Sensitvity Mode - lower touch refresh rate - output)
33	P1[1]	I/O	–	HSYNC (Horizontal Timing signal - input)
34	P1[2]	I/O	–	TXDRIVE (Drive TX signal hi/lo - output)
35	P1[3]	I/O	–	VSYNC (Vertical blanking timing signal - input)

Note
10.See **"Pin information"** on page 10 for details on pin configuration.

Table 6 100-pin TQFP, 54 RX, CYAT8268X [10] (continued)

Pin No.	Name	Type		Description
		Digital	Analog	
36	P1[4]	I/O	–	ERROR (Set high when internal error is detected - output)
37	P1[5]	I/O	–	HSMODE_ACK (Acknowledge High Sensitivity Mode - lower touch refresh rate - input)
38	P1[6]	I/O	–	COMM_INT
39	P2[0]	I/O	–	SWDIO / CMODE_REQ (Request Custom Mode - output)
40	P2[1]	I/O	–	SWDCLK / CMODE_ACK (Acknowledge Custom Mode - input)
41	VCCD	Power		Digital core power supply input/output
42	VDDD	Power		Digital power supply input
43	VSS	Power		Connect to ground
44	VSS	Power		Connect to ground
45	VDDA	Power		TX analog power supply input
46	VDDA_Q	Power		RX analog power supply input
47	VCCTX	Power		TX pump reservoir and filter capacitor connection point
48	DNU	–	–	Do not use
49	DNU	–	–	Do not use
50	DNU	–	–	Do not use
51	DNU	–	–	Do not use
52	DNU	–	–	Do not use
53	DNU	–	–	Do not use
54	DNU	–	–	Do not use
55	DNU	–	–	Do not use
56	DNU	–	–	Do not use
57	Y53	–	I/O	RX channel 53
58	VSS	Power		Connect to ground
59	Y52	–	I/O	RX channel 52
60	Y51	–	I/O	RX channel 51
61	Y50	–	I/O	RX channel 50
62	Y49	–	I/O	RX channel 49
63	Y48	–	I/O	RX channel 48
64	Y47	–	I/O	RX channel 47
65	Y46	–	I/O	RX channel 46
66	Y45	–	I/O	RX channel 45
67	Y44	–	I/O	RX channel 44
68	Y43	–	I/O	RX channel 43
69	Y42	–	I/O	RX channel 42
70	Y41	–	I/O	RX channel 41
71	Y40	–	I/O	RX channel 40

Note
10.See **"Pin information"** on page 10 for details on pin configuration.

Table 6 100-pin TQFP, 54 RX, CYAT8268X [10] (continued)

Pin No.	Name	Type		Description
		Digital	Analog	
72	Y39	–	I/O	RX channel 39
73	Y38	–	I/O	RX channel 38
74	Y37	–	I/O	RX channel 37
75	Y36	–	I/O	RX channel 36
76	Y35	–	I/O	RX channel 35
77	Y34	–	I/O	RX channel 34
78	Y33	–	I/O	RX channel 33
79	Y32	–	I/O	RX channel 32
80	Y31	–	I/O	RX channel 31
81	Y30	–	I/O	RX channel 30
82	Y29	–	I/O	RX channel 29
83	Y28	–	I/O	RX channel 28
84	Y27	–	I/O	RX channel 27
85	VDDA_Q	Power		RX analog power supply input
86	VSS	Power		Connect to ground
87	Y26	–	I/O	RX channel 26
88	Y25	–	I/O	RX channel 25
89	Y24	–	I/O	RX channel 24
90	Y23	–	I/O	RX channel 23
91	Y22	–	I/O	RX channel 22
92	Y21	–	I/O	RX channel 21
93	Y20	–	I/O	RX channel 20
94	Y19	–	I/O	RX channel 19
95	Y18	–	I/O	RX channel 18
96	Y17	–	I/O	RX channel 17
97	Y16	–	I/O	RX channel 16
98	Y15	–	I/O	RX channel 15
99	Y14	–	I/O	RX channel 14
100	Y13	–	I/O	RX channel 13

Note
10.See **"Pin information"** on page 10 for details on pin configuration.

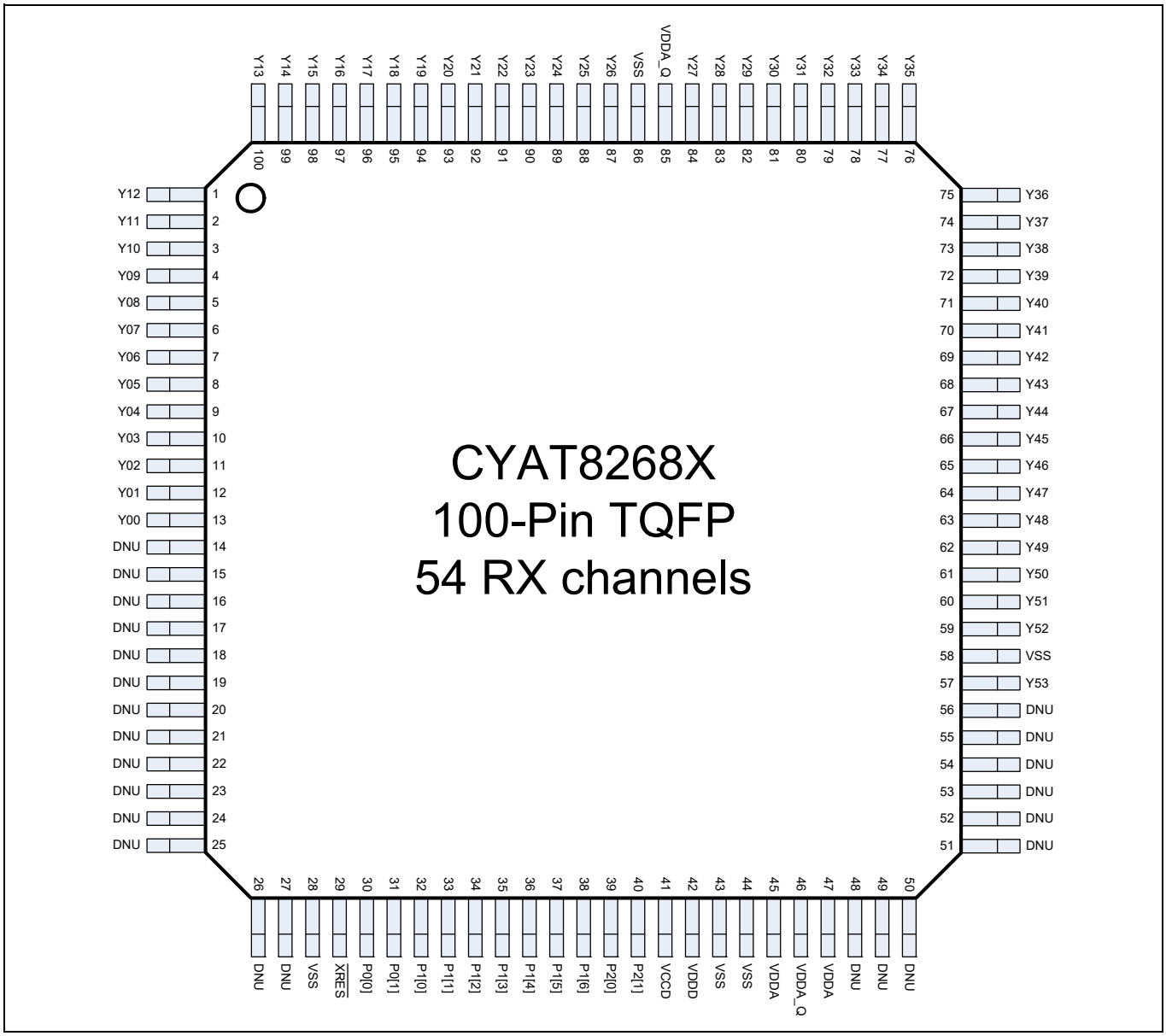


Figure 8 100-pin TQFP, 54 RX, CYAT8268X

7 Electrical specifications

This section lists CYAT8268X DC and AC electrical specifications.

7.1 Absolute maximum ratings

Table 7 Absolute maximum ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{STG}	Storage temperature	–	–55	25	125[11]	°C
V_{DDD}	Digital supply voltage	–	V_{SS} – 0.5	–	6	V
V_{DDA}	Analog supply voltage	–	V_{SS} – 0.5	–	6	
V_{DDDR}	Amplitude (V_{PP}) of digital (V_{DDD}) supply ripple riding on the DC voltage	DC to 20 MHz	–	–	100	mV
V_{DDAR}[12]	Amplitude (V_{PP}) of analog (V_{DDA}) supply ripple riding on the DC voltage (TX pump enabled)	DC to 20 MHz	–	–	100	
	Amplitude (V_{PP}) of analog (V_{DDA}) supply ripple riding on the DC voltage (TX pump disabled)	DC to 150 kHz[13]	–	–	15	
		150 kHz[13] to 20 MHz	–	–	15 + 20 dB/decade > 150 kHz[13]	
V_{CCD}	Core supply voltage	–	V_{SS} – 0.5	–	2.3	V
V_{GPIO}	Port 0 pin voltage	Driver enabled	V_{SS} – 0.5	–	6	
	Port 0 pin voltage	Driver disabled	V_{SS} – 0.5	–	7	
	Port 1 / Port 2 pin voltage	–	V_{SS} – 0.5	–	V_{DDD} + 0.5	
I_{IO}	Current into I/O pin	–	–25	–	50	mA
ESD_{CDM}	Electrostatic discharge voltage, charge device model	–	750	–	–	V
ESD_{HBM}	Electrostatic discharge voltage, human body model	100-pin TQFP	6000	–	–	
		128-pin TQFP	4000	–	–	

7.2 Operating temperature

Table 8 Operating temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T_A	Ambient temperature (A-grade)	–	–40	–	85	°C
T_A	Ambient temperature (S-grade)	–	–40	–	105	

Notes

11. Storing programmed devices at or above the ambient temperature specified by $Flash_{DR}$ may reduce flash data retention time.
12. Analog supply ripple specifications are valid for the supply presented to the external resistor (for example, label “V” **Figure 4**), not at the device VDDA and VDDA_Q pin.
13. If a 2.2-µF capacitor is used in place of a 1-µF capacitor, the threshold is 80 kHz.

7.3 DC specifications

The specifications in this section are valid under these conditions:
–40°C ≤ T_A ≤ 85°C for Grade-A devices, –40°C ≤ T_A ≤ 105°C for Grade-S devices.

7.3.1 Flash specifications

The specifications in **Table 9** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 9 Flash specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	10,000	–	–	cycles
$Flash_{DR}$	Flash data retention	Following maximum Flash write cycles ($Flash_{ENPB}$), T_A ≤ 55°C	20[14]	–	–	years
		Following maximum Flash write cycles ($Flash_{ENPB}$), T_A > 55°C	10[14]	–	–	

Note
14. Storing programmed devices at or above the ambient temperature specified by $Flash_{DR}$ may reduce flash data retention time. Infineon provides a retention calculator to calculate the retention lifetime based on customer's individual temperature profiles for operation over the ambient temperature range for the device's temperature rating. For more information, contact our support team at **support@infineon.com**.

7.3.2 Chip-level DC specifications

The specifications in **Table 10** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 10 Chip-level DC specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Digital supply voltage	Core LDO enabled (V_{CCD} output)	3.0	–	5.5	V
		Core LDO disabled (V_{CCD} input)[15]	1.71	1.8	1.95	
V_{CCD}	Digital core supply voltage	Core LDO enabled (V_{CCD} output)	–	1.8	–	
		Core LDO disabled (V_{CCD} input)[15]	1.71	1.8	1.95	
V_{DDA}[15]	Analog supply voltage	TX pump disabled	3.0	–	5.5	
PSA_{RAMP}	V_{DDA} ramp rate from ground to minimum voltage	–	–	–	100	V/ms
PSD_{RAMP}	V_{DDD} ramp rate from ground to minimum voltage	–	1[16]	–	40	
$PSD_{RAMPDOWN}$	V_{DDD} ramp down rate from 1.5 V to 1.0 V	–	1[16]	–	40	
I_{DDD_ACT}	V_{DDD} active current	–	–	20	50	mA
I_{DDA_ACT}	V_{DDA} active current	–	–	15	20	
I_{DDD_DS}	V_{DDD} deep sleep current	–	–	3	–	µA
I_{DDA_DS}	V_{DDA} deep sleep current	–	–	2	–	
I_{DDD_XR}	V_{DDD} current, $\overline{XRES}$ = LOW	1.71 V ≤ V_{DDD} ≤ 1.95 V	–	5	–	
		3.0 V ≤ V_{DDD} ≤ 5.5 V	–	1	–	
I_{DDA_XR}	V_{DDA} current, $\overline{XRES}$ = LOW	–	–	25	–	
I_{DDD_P}	V_{DDD} flash programming and flash verify current	–	–	5	25	mA

Notes

15. These Min and Max limits are inclusive of noise. For proper operation, V_{DDA} or V_{DDD} with combined noise cannot go below or above the specified Min or Max limits.
16. If minimum ramp rate cannot be met, XRES should be asserted during voltage ramp (1.5 V > V_{DDD} > 1.0 V for ramp-down or until voltage is stable for ramp-up). Note that a glitch on the I^2C bus could occur during voltage ramp in this case.

7.3.3 I/O Port 0 (P0[0:1]) DC specifications

The Port 0 specifications in **Table 11** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 11 I/O Port 0 (P0[0:1]) DC specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input high voltage	CMOS mode	0.7 × V_{DDD}	–	–	V
		1.8 V mode, V_{EXT}[18] = 1.8 V, 3.0 V ≤ V_{DDD} ≤ 5.5 V	0.7 × V_{EXT}	–	–	
V_{IL}	Input low voltage	CMOS mode	–	–	0.3 × V_{DDD}	
		1.8 V mode, V_{EXT}[18] = 1.8 V, 3.0 V ≤ V_{DDD} ≤ 5.5 V	–	–	0.3 × V_{EXT}	
V_{OH}	High output voltage	Reference to V_{DDD}, I_{OH} = 1 mA, V_{DDD} = 1.8 V	V_{DDD} – 0.5	–	–	
		Reference to V_{DDD}, I_{OH} = 4 mA, V_{DDD} = 3.0 V	V_{DDD} – 0.6	–	–	
V_{OL}	Low output voltage	V_{DDD} ≥ 1.71 V, I_{OL} = 10 mA	–	–	0.6	
		V_{DDD} ≥ 1.71 V, I_{OL} = 3 mA	–	–	0.4	
V_H	Input hysteresis	–	0.1 × V_{DDD}	–	–	
T_{RISE_OV}	Output rise time Fast-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	2	–	12	ns
	Output rise time Slow-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	10	–	60	
T_{FALL_OV}	Output fall time Fast-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	1.5	–	12	
	Output fall time Slow-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	10	–	60	
I_{IL}[17]	Input leakage current (absolute value)	T_A = 25°C, V_{DDD} = 3.0 V	–	–	14	nA
		T_A = 25°C, V_{DDD} = 0.0 V	–	–	10	µA
C_{IN}	Input pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	pF
C_{OUT}	Output pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	
R_{INT}	Internal pull-up / pull-down resistance	Pin configured for internal pull-up or pull-down; note that all I/Os are Hi-Z during chip initialization (after XRES or Bootloader Exit)	3.5	5.6	8.5	kΩ

Notes

17. Gang tested with all I/Os to 1 µA.
18. V_{EXT} is the external supply used to bias the pull-up resistor when used on an I^2C bus.

7.3.4 I/O Port 1 (P1[0:6]), Port 2 (P2[0:1]), and $\overline{\text{XRES}}$ DC specifications

The specifications in **Table 12** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 12 I/O Port 1 (P1[0:6]), Port 2 (P2[0:1]), and $\overline{\text{XRES}}$ DC specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold	1.8 V configuration	1.26	–	–	V
		CMOS configuration	0.7 × V_{DDD}	–	–	
		XRES	1.35	–	–	
V_{IL}	Input voltage low threshold	1.8 V configuration	–	–	0.54	
		CMOS configuration	–	–	0.3 × V_{DDD}	
		XRES	–	–	0.45	
V_{OH}	High output voltage	I_{OH} = 4 mA, V_{DDD} = 3.0 V	V_{DDD} – 0.6	–	–	
		I_{OH} = 1 mA, V_{DDD} = 1.8 V	V_{DDD} – 0.5	–	–	
V_{OL}	Low Output Voltage	I_{OL} = 8 mA, V_{DDD} = 3.3 V	–	–	0.6	
		I_{OL} = 4 mA, V_{DDD} = 1.8 V	–	–	0.6	
V_H	Input hysteresis voltage	–	0.1 × V_{DDD}	–	–	
T_{RISE_G}	Output rise time Fast-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	2	–	12	ns
	Output rise time Slow-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	–	–	60	
T_{FALL_G}	Output fall time Fast-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	2	–	12	
	Output fall time Slow-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	–	–	60	
I_{IL}[19]	Input leakage (absolute value)	–	–	–	2	nA
C_{IN}	Input pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	pF
C_{OUT}	Output pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	
R_{INT}[20]	Internal pull-up/pull-down resistance	Pin configured for internal pull-up or pull-down	3.5	5.6	8.5	kΩ

Notes
19. Gang tested with all I/Os to 1 µA.
20. XRES is input only with no internal pull-up or pull-down resistor.

7.4 AC specifications

The specifications in this section are valid under these conditions:
–40°C ≤ T_A ≤ 85°C for Grade-A devices, –40°C ≤ T_A ≤ 105°C for Grade-S devices.

7.4.1 SWD interface AC specifications

The specifications in **Table 13** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, 3.0 V ≤ V_{DDA} ≤ 5.5 V, and C_{LOAD} = 25 pF. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 13 SWD interface AC specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
f_{SWDCLK}	SWDCLK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	14	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	8	
T_{SWDI_SETUP}	SWDIO input setup before SWDCLK HIGH	T = 1 / f_{SWDCLK}	T / 4	–	–	ns
T_{SWDI_HOLD}	SWDCIO input hold after SWDCLK HIGH	T = 1 / f_{SWDCLK}	T / 4	–	–	
T_{SWDO_VALID}	SWDCLK HIGH to SWDIO output valid	T = 1 / f_{SWDCLK}	–	–	T / 2	
T_{SWDO_HOLD}	SWDIO output hold after SWDCLK HIGH	T = 1 / f_{SWDCLK}	1	–	–	

7.4.2 Chip-level AC specifications

The specifications in **Table 14** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 14 Chip-level AC specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{XRST}	External reset ($\overline{XRES}$) pulse width	After V_{DDD} is valid	10	–	–	µs
T_{READY}	Time from deassertion of XRES to COMM_INT	–	–	–	35	ms
T_{CAL}	Calibration routine execution time	–	–	–	2500	
$F_{IMOTOL1}$	Frequency variation at 37 MHz and 48 MHz	–	–	–	±2	%

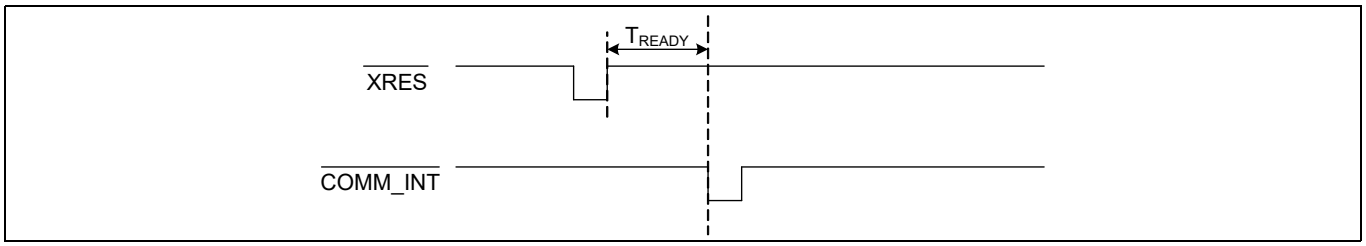


Figure 9 COMM_INT timing diagram

7.4.3 I²C specifications

The specifications in **Table 15** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V. CYAT8268X does not require a clock-stretch capable host, but is fully compatible with systems that perform clock-stretching.

To ensure proper I²C functionality in extreme bus conditions, refer to Infineon's application note *Using CY8CTMA4/5XX I²C in Systems With Slow Clock Edges* (001-81514)[21].

Important Note: The P0[0] and P0[1] pins have I/O cells optimized for use on multi-drop buses. When the touch device is powered off, the pin drivers do not load the attached bus, such that other devices attached to them may continue to communicate.

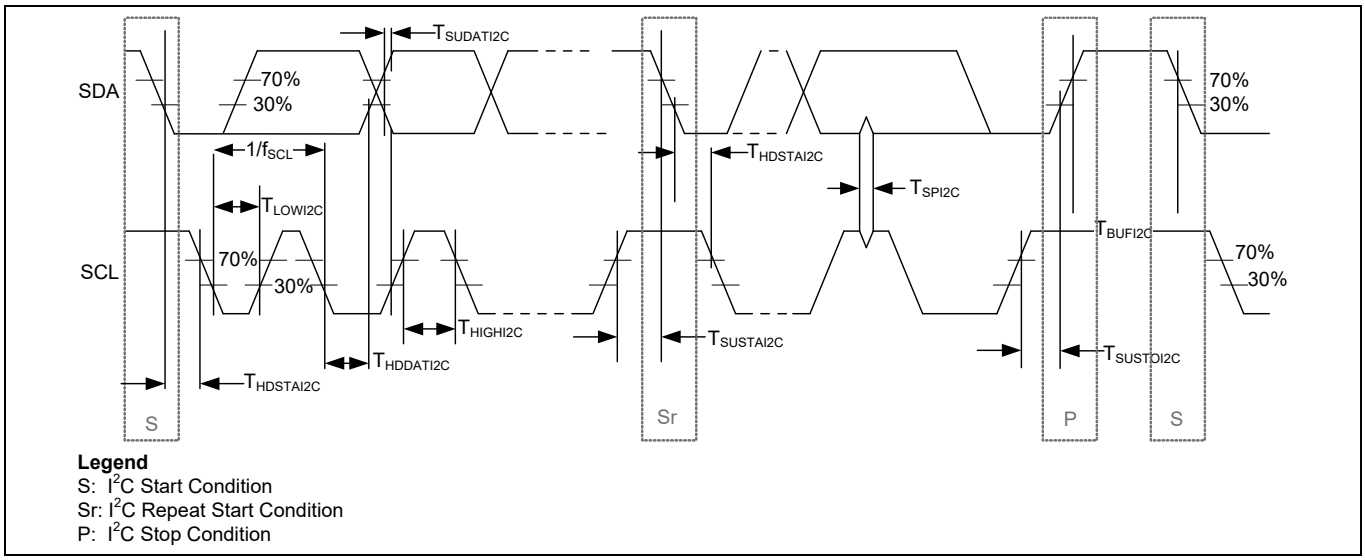


Figure 10 I²C Bus timing diagram for Fast/Standard Mode

Note

21. Extreme bus conditions are considered to be a combination of the following conditions: High-capacitive bus load, slow SCL fall time, and fast SDA rise/fall time. Infineon reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@cypress.com**.

Table 15 AC characteristics of the I²C SDA and SCL pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	4	–	0.6	–	µs
T_{LOWI2C}	LOW period of SCL clock	4.7	–	1.3	–	
$T_{HIGHI2C}$	HIGH period of SCL clock	4	–	0.6	–	
$T_{SUSTAI2C}$	Setup time for repeated start condition	4.7	–	0.6	–	
$T_{HDDATI2C}$	Data hold time	0	–	0	–	
$T_{SUDATI2C}$	Data setup time	250	–	100	–	
$T_{VDDATI2C}$	Data valid time	–	3.45	–	0.9	
$T_{VDACKI2C}$	Data acknowledge time	–	3.45	–	0.9	
$T_{SUSTOI2C}$	Setup time for stop condition	4	–	0.6	–	
V_{HH}	Input hysteresis high voltage, $1.71\ V \le V_{DDD} \le 1.95\ V$ or $3.0\ V \le V_{DDD} \le 5.5\ V$	$0.1 \times V_{DDD}$	–	$0.1 \times V_{DDD}$	–	V
T_{BUFI2C}	Bus free time between a stop and start condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes that are suppressed by input filter	–	–	50	–	ns
C_{BUS}	Capacitance load for SDA or SCL	–	400	–	400	pF
V_{IL_I2C}	Input low voltage	–0.5	$0.3 \times V_{DDD}$	–0.5	$0.3 \times V_{DDD}$	V
V_{IH_I2C}	Input high voltage	$0.7 \times V_{DDD}$	–	$0.7 \times V_{DDD}$	–	
$V_{OL\_I2C\_L}$	Output low voltage ($V_{DDD} \le 2$ V, 3 mA sink)	–	$0.2 \times V_{DDD}$	–	$0.2 \times V_{DDD}$	
$V_{OL\_I2C\_H}$	Output low voltage ($V_{DDD} > 3$ V, 3 mA sink)	–	0.4	–	0.4	
I_{OL_I2C}	Output low current	–	3	–	3	mA
	Output low current $V_{OL} = 0.6$ V	–	–	–	6	
V_{H_I2C}	Input hysteresis	$0.1 \times V_{DDD}$	–	$0.1 \times V_{DDD}$	–	mV

8 Packaging diagrams

This section provides the CYAT8268X device packaging specifications.

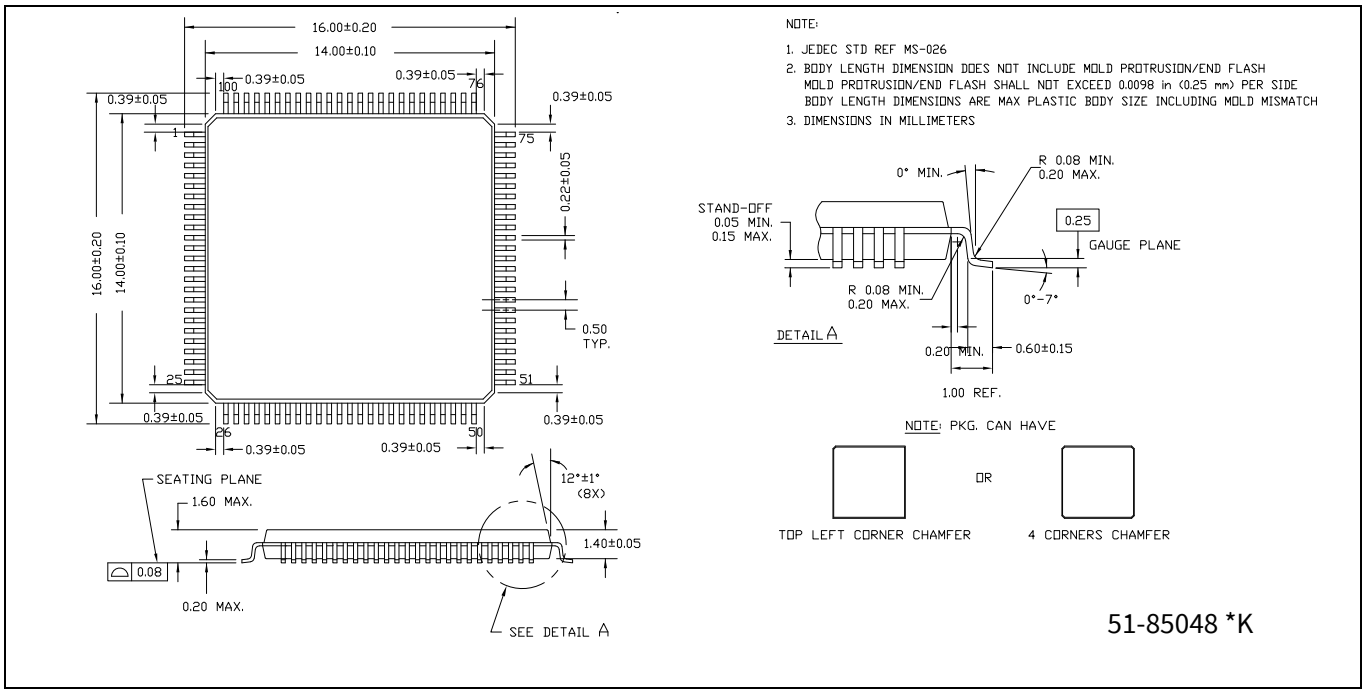


Figure 11 100-pin TQFP (14 × 14 × 1.4 mm) A100SA/AZ0AB package outline, 51-85048

8.1 Thermal impedance and moisture sensitivity

Table 16 Thermal impedance and moisture sensitivity

Package	Typical θ_{JMAX}	Typical θ_{JA}	Typical θ_{JC}	Moisture sensitivity level
100-pin TQFP	150°C	46°C/W [22]	6°C/W [22]	3

8.2 Solder reflow specifications

Table 17 lists the maximum solder reflow peak temperature.

Important Note

Thermal ramp rate during preheat should be 3°C/s or lower. The packaged device supports Pb-free solder reflow profile as per section 5.6 of J-STD-020.D1.

Table 17 Solder reflow specifications

Package	Maximum peak temperature	Time at maximum temperature
All packages	260°C	30 seconds

Note

22.Measured at 25°C ambient on a 4-layer PCB.

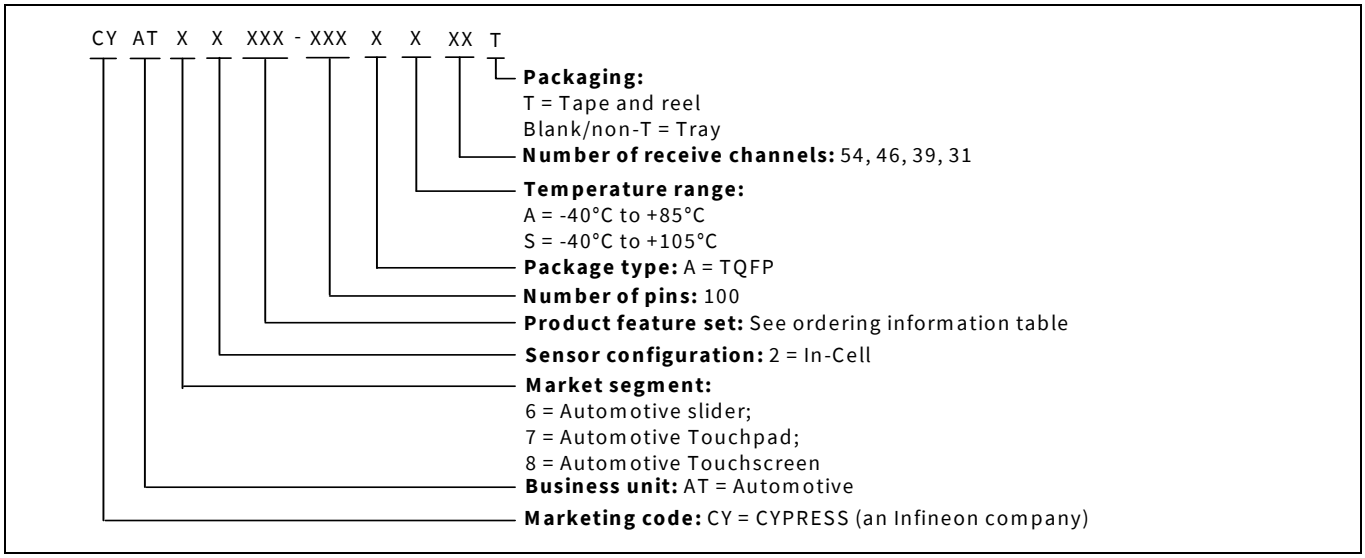
9 Ordering information

Table 18 lists the CYAT8268X touchscreen controllers.

Table 18 Ordering information [23]

MPN	Number of receive channels	Number of fingers	Water rejection	Gesture	Thick overlay/ Thick glove support
CYAT82687-100AA31	31	10	✓	✓	✓
CYAT82687-100AS31	31	10	✓	✓	✓
CYAT82687-100AA39	39	10	✓	✓	✓
CYAT82687-100AS39	39	10	✓	✓	✓
CYAT82687-100AA46	46	10	✓	✓	✓
CYAT82687-100AS46	46	10	✓	✓	✓
CYAT82687-100AA54	54	10	✓	✓	✓
CYAT82687-100AS54	54	10	✓	✓	✓

9.1 Ordering code definitions



Note
23. All devices have the following base features: Water Rejection, DisplayArmor™, AutoArmor™, DualSense™, CAPSENSE™ buttons, and Large Object Detection and Rejection.

10 Acronyms

Table 19 Acronyms used in this document

Acronym	Description
CPU	central processing unit
DNU	do not use
DSD	dual-solid diamond pattern
EMI	electromagnetic interference
EP	exposed pad
ESD	electrostatic discharge
FPC	flexible printed circuit
GPS	global positioning system
I^2C	inter-integrated circuit
I/O	input/output
ITO	indium tin oxide
LCD	liquid crystal display
LDO	low dropout regulator
MH3	Manhattan-3 pattern
MTK	manufacturing test kit
PCB	printed circuit board
PET	polyethylene terephthalate
PIP	packet interface protocol
PSoC™	programmable system-on-chip
QFN	quad flat no-lead
RF	radio frequency
SCL	serial I^2C clock
SD	signal disparity
SDA	serial I^2C data
SOL	sensor-on-lens
SMT	surface mount technology
SNR	signal-to-noise ratio
SSD	single-solid diamond pattern
SWD	serial wire debug
SWDCLK	serial wire debug clock
TRM	technical reference manual
TTHE	touch tuning host emulator
V_{PP}	volts peak-to-peak

11 Reference documents

Infineon has created a collection of documents to support the design of PSoC™ Automotive Multitouch touchscreen controllers.

The following list will guide you in identifying the proper document for your task:

- PCB/FPC schematic and layout design
- ITO panel design
- Driver development
- Manufacturing (MFG)
- System performance evaluation

Infineon's PSoC™ Automotive Multitouch technology is Infineon confidential information and is protected through a Non-Disclosure Agreement (NDA). These documents are not publicly available on the Infineon website. Contact your local Infineon office to request any of these documents pursuant to the aforementioned NDA. You can also direct your requests to **automotive@cypress.com**.

Table 20 Reference specifications

Document number	Document title	Description	PCB FPC	ITO panel	Driver	MFG	System
Solution specifications							
001-49389	PSoC™ Automotive Multitouch Touchscreen Controller Performance Parameters	Contains Infineon touchscreen performance parameter definitions, justification for parameters, and parameter test methodologies.	–	✔	–	–	✔
001-50467	PSoC™ Automotive Multitouch Touchscreen Controller Module Design Best Practices	A system-level design guide for building a capacitive touchscreen module, covering topics such as touchscreen traces, shielding, mechanical design, FPC/PCB design, and LCD considerations.	✔	✔	–	–	–
001-81514	Using CY8CTMA4/5XX I^2C in Systems With Slow Clock Edges	Discusses how to ensure proper I^2C functionality in extreme bus conditions[24].	✔	–	–	–	–
001-83948	Touch Tuning Host Emulator Guide	Describes the Touch Tuning Host Emulator Software	–	–	–	–	✔
001-63571	CY3295-MTK PSoC™ Multitouch Manufacturing Test Kit User Guide	Describes the CY3295-MTK Manufacturing Test Kit	–	–	–	✔	–
001-81891	The Touch Driver for Android (TTDA) User Guide	Contains information on the example Android touch driver	–	–	✔	–	–
External specifications: These specifications are not created or owned by Infineon, but directions on how to acquire or access them can be provided upon request by contacting **automotive@cypress.com**.							
UM10204	I^2C-bus specification and user manual		✔	–	–	–	✔
ISO11452	Component test methods for electrical disturbances in Road Vehicles Package		✔	–	–	–	✔
CISPR25	Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers		✔	–	–	–	✔
J-STD-020D.1	Moisture/Reflow Sensitivity	Classification for Nonhermetic Surface Mount Devices	✔	–	–	–	✔

Note
24. Extreme bus conditions are considered to be a combination of the following conditions: High-capacitive bus load, slow SCL fall time, and fast SDA rise/fall time.

12 Document conventions

12.1 Units of measure

Table 21 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
µA	microampere
µF	microfarad
µs	microsecond
µW	microwatt
Ω	ohm
Hz	hertz
kΩ	kilo-ohm
kbps	kilobits per second
kHz	kilohertz
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
mW	milliwatt
Mbps	megabits per second
MHz	megahertz
nA	nanoampere
ns	nanosecond
pF	picofarad
s	second

12.2 Port nomenclature

Px[y] describes a particular bit “y” available within an I/O port “x.” For example, P4[2] reads “port 4, bit 2."

Px[y:z] describes a particular range of bits “y to z” within an I/O port named “Px.” For example, P4[0:5] refers to bits 0 through 5 within an I/O port named P4.

13 Glossary

Table 22 Glossary

Term	Definition
accuracy	The maximum position error across the touchscreen, measured in millimeters, along a straight line between the actual finger position and the reported finger position. Accuracy is measured across the core and full panel. See Infineon's *PSoC™ Automotive Multitouch Touchscreen Controller Performance Parameters* (001-49389)[25] specification for more information.
All-Points	Cypress brand name for PSoC™ Automotive Multitouch devices capable of tracking the motion of multiple fingers.
AMOLED/OLED	Type of display using Active Matrix (AM) Organic Light Emitting Diodes (OLED).
conversion	The process of measuring the capacitance of an electrode connected to a pin (self capacitance) or the capacitance between a pair of electrodes connected to different pins (mutual capacitance). The result is a number that can be processed by the channel engine and CPU.
core	That portion of the touchscreen, responsive to touch, less a perimeter area whose width is the larger of 3.5 mm or half the width of the finger (for example, less a perimeter band 4.5-mm wide for a 9-mm finger).
core LDO	Low Drop Out Regulator that sources power to the digital core when enabled. Input to the LDO is VDDD. Output of the LDO is connected to the digital supply pin VCCD. When the core LDO is disabled, power must be externally applied to the digital core supply pin VCCD.
cover lens	The top layer in the touchscreen stackup that provides mechanical stability and protection for the touchscreen sensor.
DCVCOM	Type of Liquid Crystal Display where the common electrode (VCOM) is driven by DC voltage.
linearity	The deviation of the position data from a best-fit straight line across the touchscreen, measured in millimeters. Linearity is measured across the core and full panel. See Infineon's *PSoC™ Automotive Multitouch Touchscreen Controller Performance Parameters* (001-49389)[25] specification for more information.
mutual capacitance	The capacitance between two touchscreen electrodes.
refresh rate	The frequency at which consecutive frames of touchscreen data are made available in a data buffer while a finger is present on the touchscreen. See Infineon's *PSoC™ Automotive Multitouch Touchscreen Controller Performance Parameters* (001-49389)[25] specification for more information.
RX	Receive. A touchscreen electrode or touchscreen controller sense pin, mapped or switched to a charge sensing circuit within the controller (known as a receive channel).
scan	The conversion of all sensor capacitances to digital values.
sense pin	A pin that can be multiplexed to RX or TX.
signal-to-noise ratio (SNR)	The ratio between a capacitive finger signal and system noise.
signal disparity (SD)	The ratio of maximum measured signal when the touchscreen is grounded and maximum measured signal when the touchscreen is isolated from ground.

Note

25. Cypress reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@cypress.com**.

Table 22 Glossary (continued)

Term	Definition
stackup	Layers of materials, in defined assembly order, that make up a touchscreen sensor.
TX	Transmit. A touchscreen electrode or touchscreen controller sense pin, mapped or switched to a charge forcing circuit within the controller. This charge forcing circuit drives a periodic waveform onto one or more touchscreen electrodes, which are coupled through mutual capacitance to adjacent receive electrodes.

Revision history

Document revision	Date	Description of changes
**	2016-09-30	New datasheet.
*A	2016-10-26	Updated **Pin information**: Updated **Figure 7**. Updated **Table 6**. Updated to new template.
*B	2017-09-01	Updated **Ordering information**: No change in part numbers. Updated **Ordering code definitions**. Updated to new template. Completing Sunset Review.
*C	2020-04-13	Updated **Packaging diagrams**: spec 51-85048 – Changed revision from *J to *K.
*D	2020-10-29	Obsolete document. Completing Sunset Review.
*E	2021-03-30	Reactivated document. Updated to new template.
*F	2021-04-22	Updated **Touchscreen System overview**: Updated **Figure 1**. Updated **Power supply information**: Updated **Figure 3**. Updated **Figure 4**. Updated **Electrical specifications**: Updated **DC specifications**: Updated **Chip-level DC specifications**: Updated **Table 10**. Updated **I/O Port 0 (P0[0:1]) DC specifications**: Referred Note "$\overline{\text{XRES}}$ is input only with no internal pull-up or pull-down resistor." in R_{INT} parameter in **Table 11**. Updated **AC specifications**: Updated **Chip-level AC specifications**: Updated **Table 14**. Updated **I2C specifications**: Updated **Table 15**. Updated **Packaging diagrams**: No change in revisions. Updated **Thermal impedance and moisture sensitivity**: Added Note 22 and referred the same note in values of Typical θ_{JA} and Typical θ_{JC} corresponding to 100-pin TQFP in **Table 16**.

Revision history

Document revision	Date	Description of changes
*G	2021-08-18	Updated **Pin information**: Updated description. Updated **Electrical specifications**: Updated **Absolute maximum ratings**: Updated all details corresponding to V_{DDDR} and V_{DDAR} parameters in **Table 7**. Updated **DC specifications**: Updated **Chip-level DC specifications**: Updated all details corresponding to PSD_{RAMP} and added $PSD_{RAMPDOWN}$ parameters in **Table 10**. Updated **I/O Port 0 (P0[0:1]) DC specifications**: Removed Note "$\overline{XRES}$ is input only with no internal pull-up or pull-down resistor." and its reference in R_{INT} parameter in **Table 11**. Updated details under "Conditions" column corresponding to R_{INT} parameter in **Table 11**. Updated **Packaging diagrams**: Updated **Thermal impedance and moisture sensitivity**: Updated and added details corresponding to 100-pin TQFP in **Table 16**.
*H	2022-05-19	Updated to the PSoC™ Automotive Multitouch branding guidelines. Updated **Electrical specifications**: Updated **Absolute maximum ratings**: Updated all details corresponding to ESD_{HBM} parameter in **Table 7**.
*I	2022-08-08	Updated Document Title to read as "CYAT8268X, PSoC™ Automotive Multitouch Generation 6XL Hybrid In-cell Datasheet". Updated **Electrical specifications**: Updated **Absolute maximum ratings**: Updated **Table 7**. Migrated to Infineon template.

Revision history

Document revision	Date	Description of changes
*J	2023-05-09	Updated **Touchscreen System specifications**: Updated **System Performance specifications**: Updated description. Updated **Electrical specifications**: Updated **DC specifications**: Added description. Updated **Flash specifications**: Updated description. Updated **Table 9**. Updated Note 11. Updated **Chip-level DC specifications**: Updated description. Updated **I/O Port 0 (P0[0:1]) DC specifications**: Updated description. Updated **Table 11**. Updated **I/O Port 1 (P1[0:6]), Port 2 (P2[0:1]), and XRES DC specifications**: Updated description. Updated **Table 12**. Updated **AC specifications**: Added description. Updated **SWD interface AC specifications**: Updated description. Updated **Chip-level AC specifications**: Updated description. Updated **I2C specifications**: Updated description. Updated to new template. Completing Sunset Review.

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