AIROC™ Bluetooth® LE module

General description

The CYBLE-3x307x-02 is a fully integrated Bluetooth® smart ready wireless module. The CYBLE-3x307x-02 includes an onboard crystal oscillator, passive components, flash memory, and the CYW20835 silicon device. Refer to the **CYW20835** datasheet for additional details on the capabilities of the silicon device used in this module.

The CYBLE-3x307x-02 supports peripheral functions (ADC and PWM), UART, I^2C, and SPI communication, and a PCM/I^2S audio interface. The CYBLE-3x307x-02 includes a royalty-free Bluetooth® stack compatible with Bluetooth® 5.0 in a 13.31 × 21.89 × 1.95 mm package.

The CYBLE-3x307x-02 includes 512 KB of onboard serial flash memory and is designed for standalone operation. The CYBLE-3x307x-02 uses an integrated power amplifier to achieve Class I or Class II output power capability.

The CYBLE-3x307x-02 is fully qualified by Bluetooth® SIG and is targeted at applications requiring cost-optimized Bluetooth® wireless connectivity.

The CYBLE-3x307x-02 is offered in four certified versions CYBLE-343072-02, CYBLE-333073-02, and CYBLE-333074-02. The CYBLE-343072-02 includes an integrated trace antenna. The CYBLE-333073-02 supports an external antenna through a RF solder pad output. The CYBLE-333074-02 supports an external antenna via a u-FL connector.

Module description

- Module size: 13.31 × 21.89 × 1.95 mm
- Bluetooth® 5.0 qualified smart ready module
  - QDID: TBD
  - Declaration ID: TBD
- Certified to FCC, ISED, MIC, and CE regulations
- Castelated solder pad connections for ease-of-use
- 512-KB on-module serial flash memory
- Up to 24 GPIOs
- Temperature range: –30 °C to +85 °C
- Cortex-M4 32-bit processor
- Maximum TX output power
  - +12 dBm for Bluetooth® Low Energy
    - Bluetooth® LE connection range of up to 250 meters at 12 dBm[1]
- RX receive sensitivity:
  - Bluetooth® Low Energy: –94.5 dBm

Power consumption

- Bluetooth® LE current consumption
  - RX current: 8 mA
  - TX current: 18 mA @ 12 dBm
  - Interval Bluetooth® LE ADV average current consumption: 30 µA
  - HIDOFF (Deep Sleep): 1 µA

Functional capabilities

- 1x MIPI DMI-C interface
- 6x 16-bit PWMs
- Programmable key-scan matrix interface, up to 8 × 20 key scanning matrix

- Quadrature decoder
- Watchdog timer (WDT)
- 1x peripheral UART, 1x UART for programming and HCI
- 1x SPI (master or slave mode)
- 1x I2C master
- One ADC (10-ENoB for DC measurement and 12-ENOB for audio measurement)
- Hardware security engine

Benefits

CYBLE-3x307x-02 provides all necessary components required to operate Bluetooth® LE communication standards.

- Proven ready-to-use hardware design
- Cost optimized for applications without space constraints
- Nonvolatile memory for self-sufficient operation and over-the-air updates
- Bluetooth® SIG listed with QDID and declaration ID
- Fully certified module eliminates the time needed for design, development, and certification processes
- ModusToolbox™ provides an easy-to-use integrated design environment (IDE) to configure, develop, and program a Bluetooth® application

More information

Infineon provides a wealth of data at **www.cypress.com** to help you to select the right module for your design, and to help you to quickly and effectively integrate the module into your design.

References

- Overview: **AIROC™ Bluetooth® LE & Bluetooth® portfolio**, **Module roadmap**
- **CYW20835 Bluetooth® silicon datasheet**
- Development kits:
  - **CYBLE-343072-EVAL**, CYBLE-343072-02 evaluation board
  - **CYBLE-333074-EVAL**, CYBLE-333074-02 evaluation board
- Test and debug tools:
  - **CYSmart**, Bluetooth® LE test and debug tool (Windows)
  - **CYSmart Mobile**, Bluetooth® LE test and debug tool (Android/iOS Mobile App)
- Knowledge base article
  - **KBA97095** - EZ-Bluetooth® LE module placement
  - **TBD** - TBD
  - **KBA213976** - FAQ for Bluetooth® LE and regulatory certifications with EZ-BLE modules
  - **KBA210802** - Queries on Bluetooth® LE qualification and declaration processes
  - **KBA218122** - 3D Model Files for EZ-BLE/EZ-BT modules
  - **TBD** - Platform files for CYBLE-343072-EVAL and CYBLE-333074-EVAL
  - **KBA223428** - Programming an EZ-BT WICED module

Note

1. Connection range tested module-to-module in full line-of-sight environment, free of obstacles or interference sources with output power of +12.0 dBm. Actual range will vary based on end product design, environment, receive sensitivity, and transmit output power of the central device.

Development environments

ModusToolbox™ software is a modern, extensible development environment supporting a wide range of Infineon microcontroller devices. It provides a flexible set of tools and a diverse, high-quality collection of application-focused software. These include configuration tools, low-level drivers, libraries, and operating system support, most of which are compatible with Linux®, macOS®, and Windows®-hosted environments. ModusToolbox™ software does not include proprietary tools or custom build environments. This means you choose your compiler, your IDE, your RTOS, and your ecosystem without compromising usability or access to our industry leading CAPSENSE™, AIROC™, Bluetooth®, Wi-Fi, security, and low-power features.

Technical support

- **Cypress community:** Whether you are a customer, partner, or a developer interested in the latest innovations, the developer community offers you a place to learn, share, and engage with both Infineon experts and other embedded engineers around the world.
- **Frequently asked questions (FAQs)**: Learn more about our Bluetooth® ecosystem.
- Visit our **support** page and create a **technical support case** or contact a **local sales representatives**. If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 2 at the prompt.

Contents

1 Overview

1.1 Functional block diagram

Figure 1 illustrates the CYBLE-3x307x-02 functional block diagram.

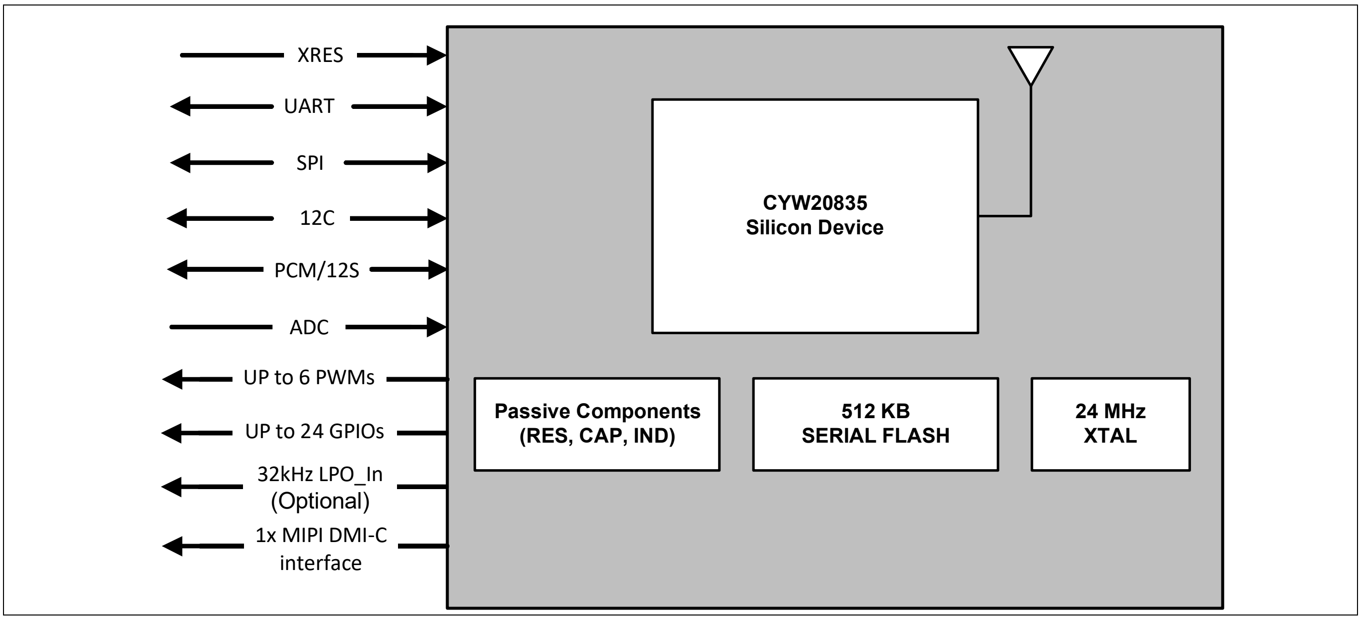


Figure 1 Functional block diagram (GPIOs)

1.2 Module description

The CYBLE-3x307x-02 module is a complete module designed to be soldered to the application's main board.

1.2.1 Module dimensions and drawing

Infineon reserves the right to select components from various vendors to achieve the Bluetooth® module functionality. Such selections will still guarantee that all mechanical specifications and module certifications are maintained. Designs should be held within the physical dimensions shown in the mechanical drawings in Figure 2 on page 7. All dimensions are in millimeters (mm).

Table 1 Module design dimensions

Dimension item		Specification
Module dimensions	Length (X)	13.31 ± 0.15 mm
	Width (Y)	21.89 ± 0.15 mm
Antenna connection location dimensions	Length (X)	13.31 mm
	Width (Y)	4.65 mm
PCB thickness	Height (H)	0.50 ± 0.05 mm
Shield height	Height (H)	1.45-mm typical
Maximum component height	Height (H)	1.45-mm typical
Total module thickness (bottom of module to highest component)	Height (H)	1.95-mm typical

See **Figure 2** for the mechanical reference drawing for CYBLE-3x307x-02.

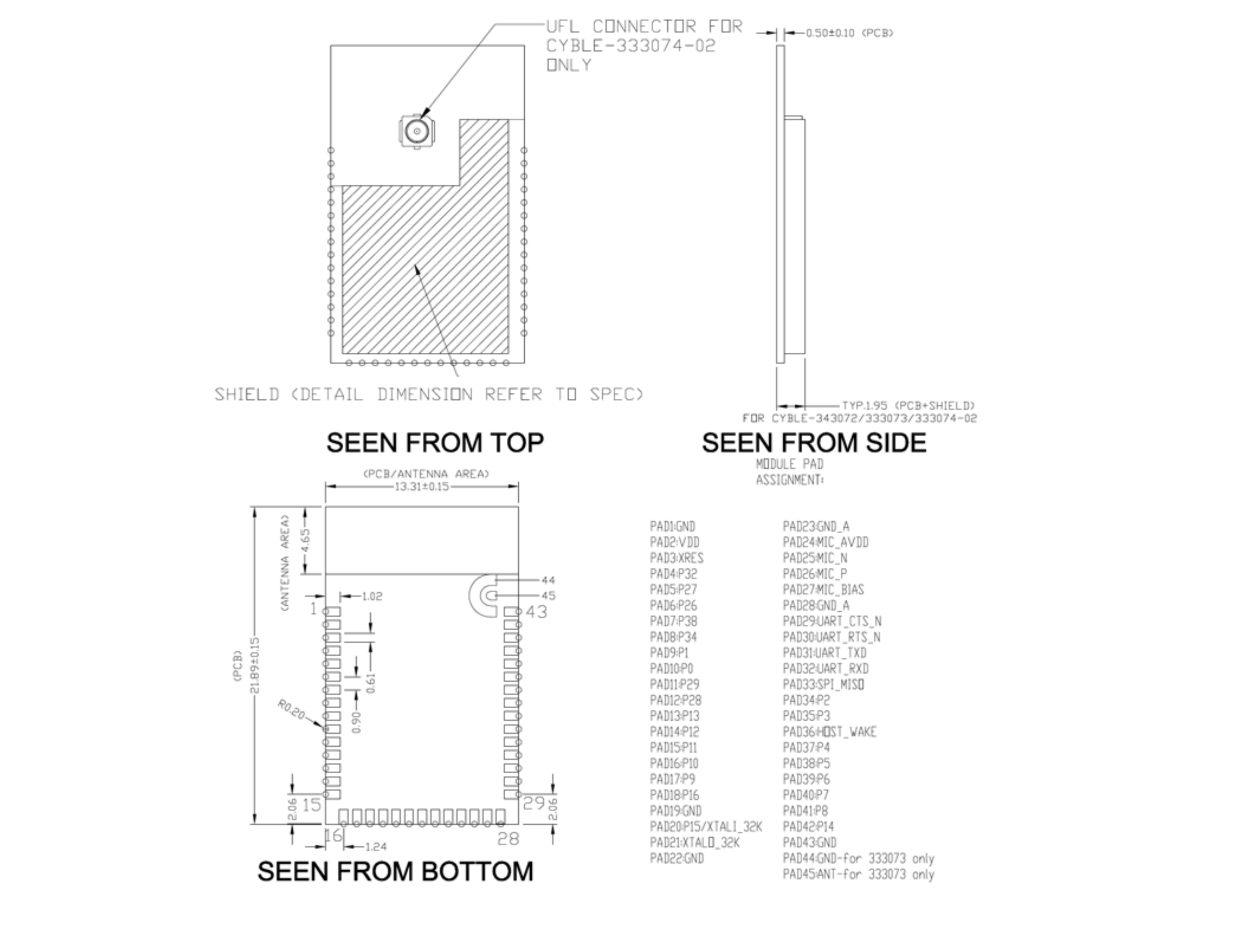


Figure 2 Module mechanical drawing

Notes

2. No metal should be located beneath or above the antenna area. Only bare PCB material should be located beneath the antenna area. For more information on recommended host PCB layout, see **"Recommended host PCB layout"** on page 10.
3. The CYBLE-343072-02, CYBLE-333073-02, CYBLE-333074-02 includes castellated pad connections, denoted as the circular openings at the pad location above.

2 Pad connection interface

As shown in the bottom view of **Figure 2 on page 7**, the CYBLE-3x307x-02 connects to the host board via solder pads on the backside of the module. **Table 2** and **Figure 3** detail the solder pad length, width, and pitch dimensions of the CYBLE-3x307x-02 module.

Table 2 Connection description

Part number	Name	Connections	Connection type	Pad length dimension	Pad width dimension	Pad pitch
CYBLE-343072-02	SP	43	Solder pads	1.02 mm	0.61 mm	0.90 mm
CYBLE-333073-02	SP	45	Solder pads	1.02 mm	0.61 mm	0.90 mm
CYBLE-333074-02	SP	43	Solder pads	1.02 mm	0.61 mm	0.90 mm

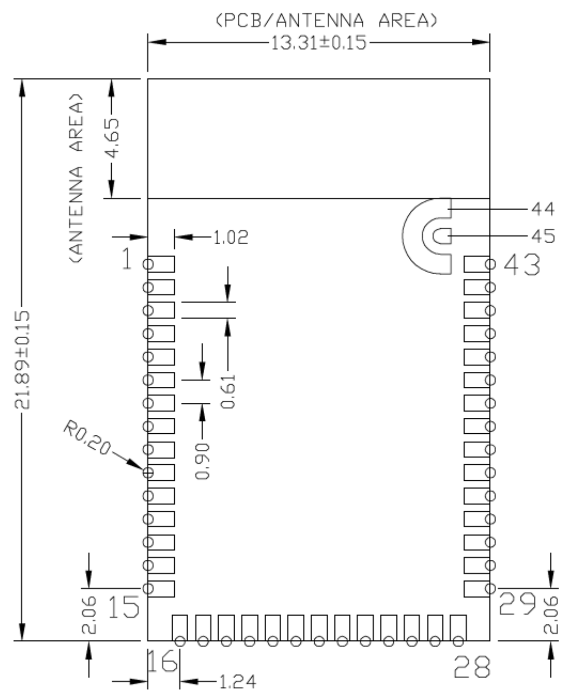


Figure 3 Solder pad dimensions (seen from bottom)

To maximize RF performance, the host layout should follow these recommendations:

1. Antenna Area Keepout: The host board directly below the antenna area of the module (see **Figure 2 on page 7**) must not contain ground or signal traces. This keepout area requirement applies to all layers of the host board.
2. Module Placement: The ideal placement of the Bluetooth® module is in a corner of the host board with the PCB trace antenna located at the far corner. This placement minimizes the additional recommended keepout area stated in item 2. Refer to **AN96841** for module placement best practices.

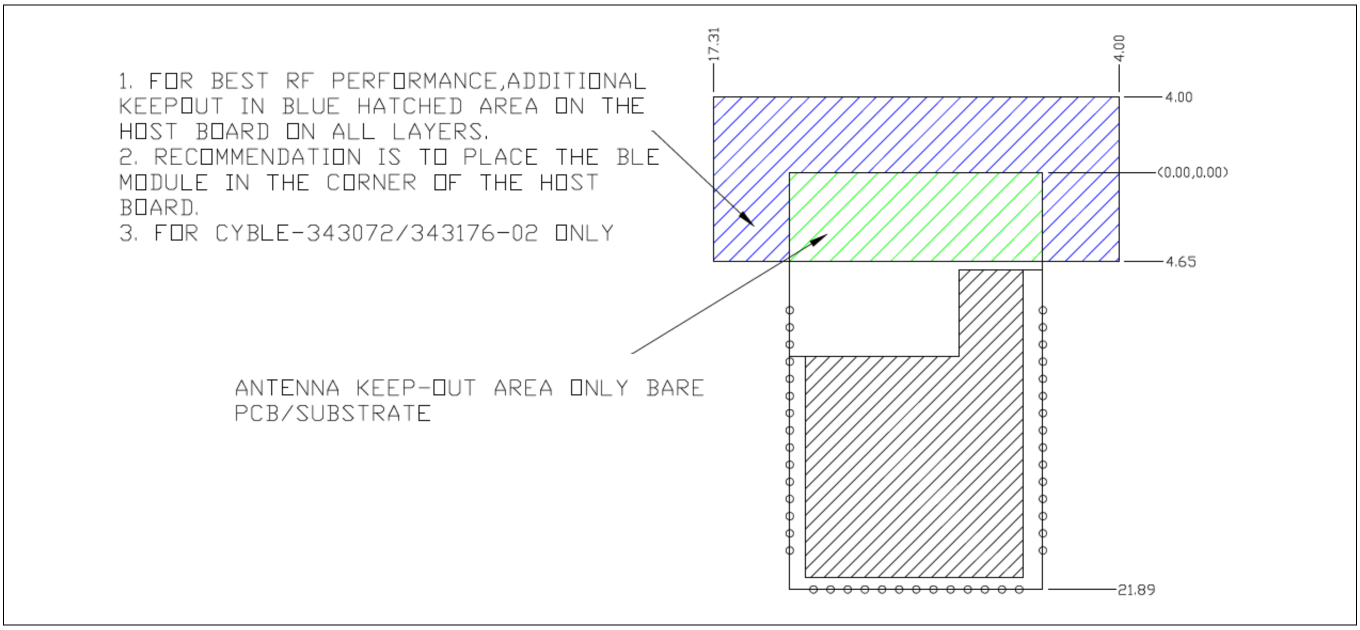


Figure 4 **Recommended host PCB keepout area around the CYBLE-3x307x-02 antenna**

3 Recommended host PCB layout

Figure 5, **Figure 6**, **Figure** , and **Table 3** provide details that can be used for the recommended host PCB layout pattern for the CYBLE-3x307x-02. Dimensions are in millimeters unless otherwise noted. Pad length of 1.26 mm (0.64 mm from center of the pad on either side) shown in **Figure 4** is the minimum recommended host pad length. The host PCB layout pattern can be completed using either **Figure 5**, **Figure 6**, or **Figure** . It is not necessary to use all figures to complete the host PCB layout pattern.

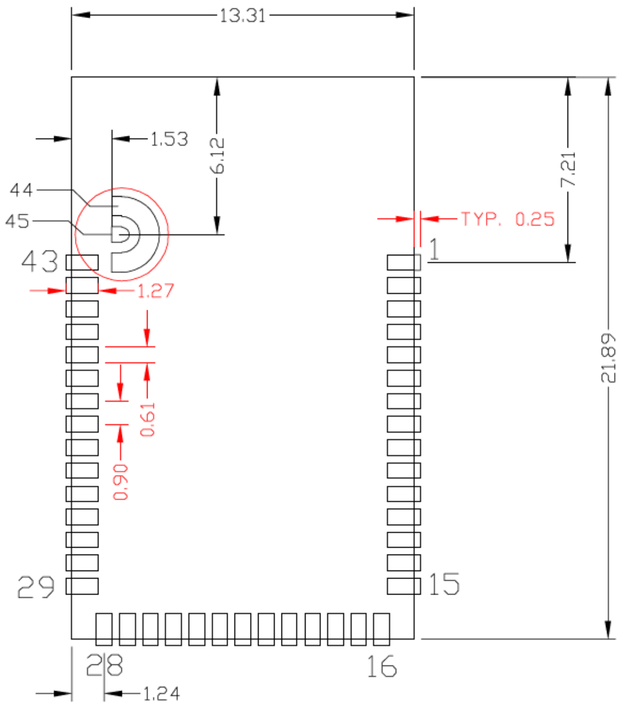


Figure 5 CYBLE-3x307x-02 host layout (dimensioned)

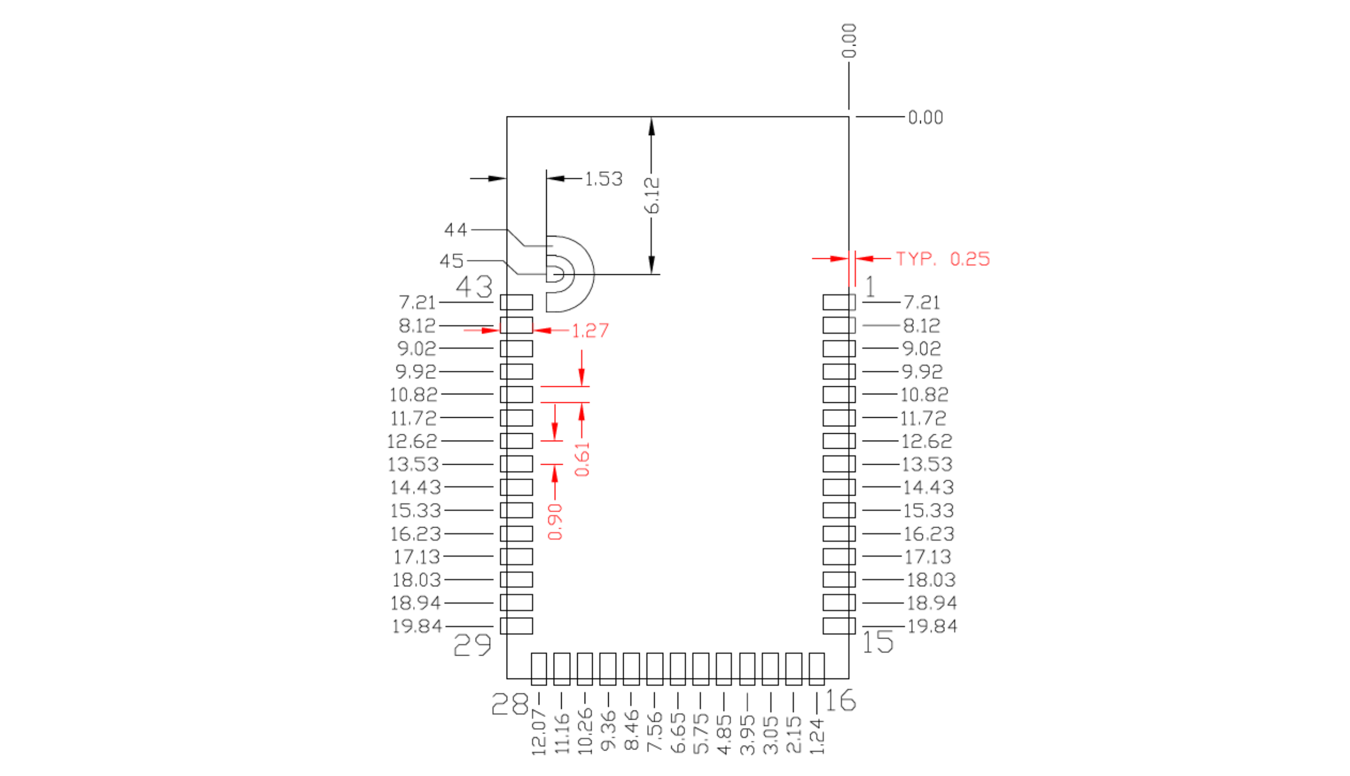


Figure 6 **CYBLE-3x307x-02 host layout (relative to origin)**

Table 3 provides the center location for each solder pad on the CYBLE-3x307x-02. All dimensions are referenced to the center of the solder pad. Refer to **Figure 7** for the location of each module solder pad.

Table 3 **Module solder pad location**

Solder pad (center of pad)	Location (X,Y) from origin (mm)	Dimension from origin (mils)
1	(0.38, 7.21)	(14.96, 283.86)
2	(0.38, 8.12)	(14.96, 319.68)
3	(0.38, 9.02)	(14.96, 355.12)
4	(0.38, 9.92)	(14.96, 390.55)
5	(0.38, 10.82)	(14.96, 425.98)
6	(0.38, 11.72)	(14.96, 461.42)
7	(0.38, 12.62)	(14.96, 496.85)
8	(0.38, 13.53)	(14.96, 532.68)
9	(0.38, 14.43)	(14.96, 568.11)
10	(0.38, 15.33)	(14.96, 603.54)
11	(0.38, 16.23)	(14.96, 638.54)
12	(0.38, 17.13)	(14.96, 674.41)
13	(0.38, 18.03)	(14.96, 709.84)
14	(0.38, 18.94)	(14.96, 745.67)
15	(0.38, 19.84)	(14.96, 781.10)
16	(1.24, 21.51)	(48.82, 846.85)

Table 3 Module solder pad location *(continued)*

Solder pad (center of pad)	Location (X,Y) from origin (mm)	Dimension from origin (mils)
17	(2.15, 21.51)	(84.65, 846.85)
18	(3.05, 21.51)	(120.08, 846.85)
19	(3.95, 21.51)	(155.51, 846.85)
20	(4.85, 21.51)	(190.94, 846.85)
21	(5.75, 21.51)	(226.38, 846.85)
22	(6.65, 21.51)	(261.81, 846.85)
23	(7.56, 21.51)	(297.64, 846.85)
24	(8.46, 21.51)	(333.07, 846.85)
25	(9.36, 21.51)	(368.50, 846.85)
26	(10.26, 21.51)	(403.94, 846.85)
27	(11.16, 21.51)	(439.37, 846.85)
28	(12.07, 21.51)	(475.20, 846.85)
29	(12.93, 19.84)	(509.05, 781.10)
30	(12.93, 18.94)	(509.05, 745.67)
31	(12.93, 18.03)	(509.05, 709.84)
32	(12.93, 17.13)	(509.05, 674.41)
33	(12.93, 16.23)	(509.05, 638.98)
34	(12.93, 15.33)	(509.05, 603.54)
35	(12.93, 14.43)	(509.05, 568.11)
36	(12.93, 13.53)	(509.05, 532.68)
37	(12.93, 12.62)	(509.05, 496.85)
38	(12.93, 11.72)	(509.05, 461.42)
39	(12.93, 10.82)	(509.05, 425.98)
40	(12.93, 9.92)	(509.05, 390.55)
41	(12.93, 9.02)	(509.05, 355.12)
42	(12.93, 8.12)	(509.05, 319.68)
43	(12.93, 7.21)	(509.05, 283.86)

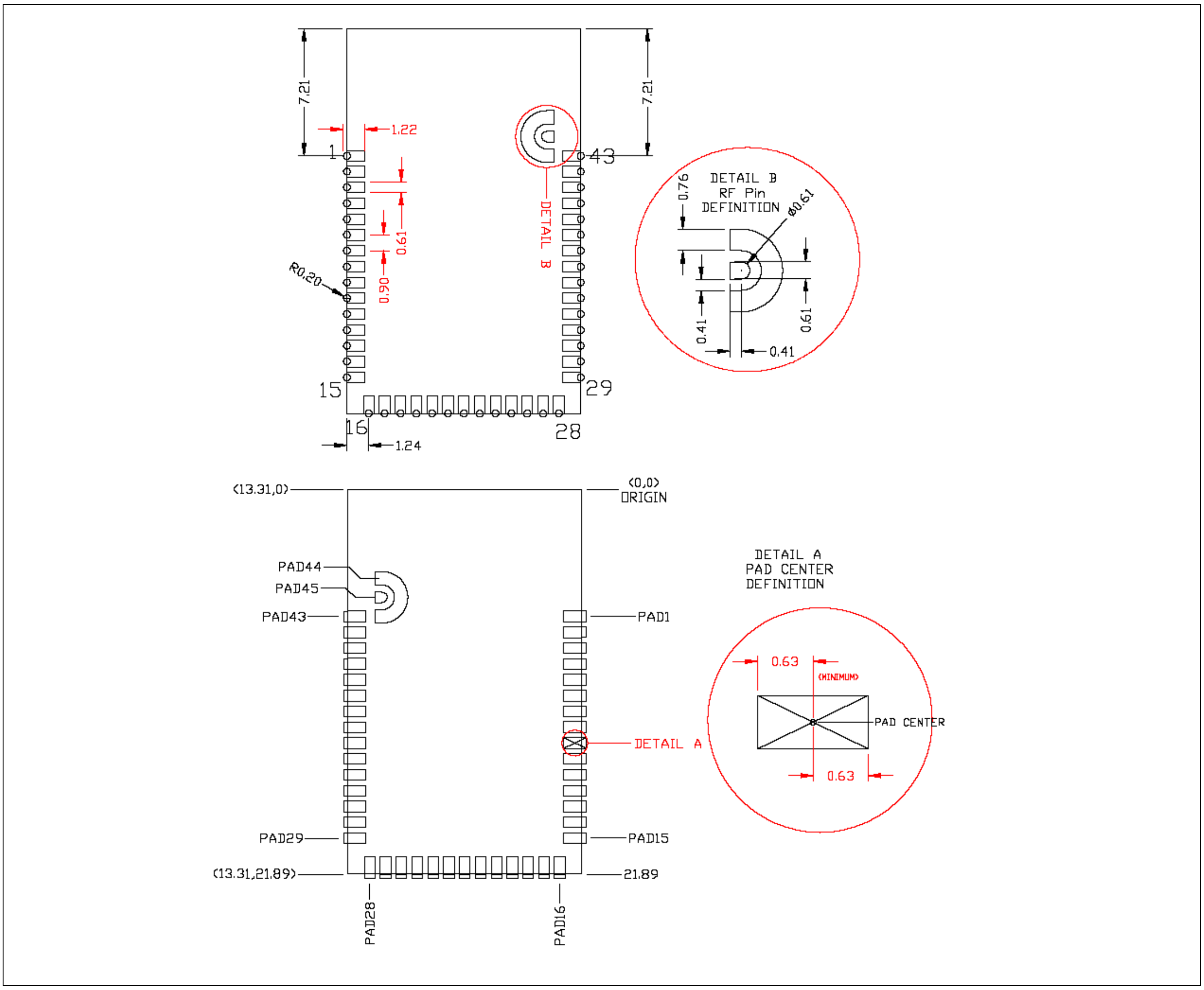


Figure 7 **Solder pad reference location**

4 Module connections

Table 4 details the solder pad connection definitions and available functions for the pad connections for the CYBLE-3x307x-02 module. **Table 4** lists the solder pads on the CYBLE-3x307x-02 module, the silicon device pin, and denotes what functions are available for each solder pad.

Table 4 Pin assignments

Module pad name	Pad number	Silicon pin name	I/O	Power domain	Description
Microphone		**Microphone**			
MIC_AVDD	24	MIC_AVDD	I	MIC_AVDD	Microphone supply
MIC_BIAS	27	MICBIAS	O	MIC_AVDD	Microphone bias supply
MIC_N	25	MICN	I	MIC_AVDD	Microphone negative input
MIC_P	26	MICP	I	MIC_AVDD	Microphone positive input
GND_A	23 28	Analog ground for microphone			
Power supply					
VDD	2	2.5V~3.6V			
Ground pins		**Ground pins**			
GND	1 19 22 43	HS-VSS	I	VSS	Digital ground
UART		**UART**			
UART_CTS_N	29	UART_CTS_N	I, PU	VDDO	CTS for HCI UART interface: NC if unused.
UART_RTS_N	30	UART_RTS_N	O, PU	VDDO	RTS for HCI UART interface. NC if unused.
UART_RXD	32	UART_RXD	I	VDDO	UART serial input. Serial data input for the HCI
					UART interface.
UART_TXD	31	UART_TXD	O, PU	VDDO	UART serial input. Serial data input for the HCI
					UART interface.
Interface		**Serial peripheral interface**			
SPI_MISO	33	SPI_MISO	I	VDDO	SPI Master In Slave Out
NA	NA	SPI_MOSI	O	VDDO	SPI Master Out Slave In
NA	NA	SPI_CSN	O	VDDO	SPI Chip Select
NA	NA	SPI_CLK	O	VDDO	SPI Clock
Crystal		**Crystal**			
NA	NA	BT_XTALI	I	PLLVDD1P2	Crystal oscillator input: see "Crystal Oscillator" on page 12 for options
NA	NA	BT_XTALO	O	PLLVDD1P2	Crystal oscillator output
XTALI_32K	20	XTALI_32K	I	VDDO	Low-power oscillator input
XTALO_32K	21	XTALO_32K	O	VDDO	Low-power oscillator output
Others		**Others**			
NA	NA	DEFAULT_STRAP	I	VDDO	Connect to VDDO

Table 4 **Pin assignments** *(continued)*

Module pad name	Pad number	Silicon pin name	I/O	Power domain	Description
HOST_WAKE	36	BT_HOST_WAKE	O	VDDO	Host wake-up. This is a signal from the Bluetooth® device to the host indicating that the Bluetooth® device requires attention. • Asserted: Host device must wake up or remain awake • Deasserted: Host device may sleep when sleep awake criteria is met. The polarity of this signal is software configurable and can be asserted high or low.
NA	NA	BT_RF	I/O	PAVDD2P5	RF antenna port
NA	NA	JTAG_SEL	–	–	ARM JTAG debug mode control: connect to GND for all applications
XRES	3	RST_N	I	VDDO	Active-low system reset with open-drain output and internal pull-up resistor

Table 5 **GPIO pin descriptions**

Module pad name	Pad number	Silicon pin name	Direction Default	POR state	Power domain	Default alternate function description
P0	10	P0	Input	Floating	VDDO	GPIO: P0
						A/D converter input 29 **Note** Not available during TM1 = 1.
P1	9	P1	Input	Floating	VDDO	GPIO: P1
						A/D converter input 28
P2	34	P2	Input	Floating	VDDO	GPIO: P2
P3	35	P3	Input	Floating	VDDO	GPIO: P3
P4	37	P4	Input	Floating	VDDO	GPIO: P4
P5	38	P5	Input	Floating	VDDO	GPIO: P5
P6	39	P6	Input	Floating	VDDO	GPIO: P6
P7	40	P7	Input	Floating	VDDO	GPIO: P7
P8	41	P8	Input	Floating	VDDO	GPIO: P8
						A/D converter input 27
P9	17	P9	Input	Floating	VDDO	GPIO: P9
						A/D converter input 26

Notes

4. The CYBLE-3x307x-02 contains a single SPI (SPI1) peripheral supporting both master or slave configurations. SPI2 is used for on-module serial memory interface.
5. In Master mode, any available GPIO can be configured as SPI1_CS. This function is not explicitly shown in **Table 20**.

Table 5 GPIO pin descriptions *(continued)*

Module pad name	Pad number	Silicon pin name	Direction Default	POR state	Power domain	Default alternate function description
P10	16	P10	Input	Floating	VDDO	GPIO: P10
						A/D converter input 25
P11	15	P11	Input	Floating	VDDO	GPIO: P11
						A/D converter input 24
P12	14	P12	Input	Floating	VDDO	GPIO: P12
						A/D converter input 23
P13	13	P13	Input	Floating	VDDO	GPIO: P13
						A/D converter input 22
P14	42	P14	Input	Floating	VDDO	GPIO: P14
						A/D converter input 21
P15	20	P15	Input	Floating	VDDO	GPIO: P15
						A/D converter input 20
P16	18	P16	Input	Floating	VDDO	GPIO: P16
						A/D converter input 19
P26	6	P26	Input	Floating	VDDO	GPIO: P26
		PWM0				Current: 16 mA sink
P27	5	P27	Input	Floating	VDDO	GPIO: P27
		PWM1				Current: 16 mA sink
P28	12	P28	Input	Floating	VDDO	GPIO: P28
		PWM2				A/D converter input 11
						Current: 16 mA sink
P29	11	P29	Input	Floating	VDDO	GPIO: P29
		PWM3				A/D converter input 10
						Current: 16 mA sink
P32	4	P32	Input	Floating	VDDO	GPIO: P32
						A/D converter input 7
P34	8	P34	Input	Floating	VDDO	GPIO: P34
						A/D converter input 5
P38	7	P38	Input	Floating	VDDO	GPIO: P38
						A/D converter input 1
NA	NA	P39	Input	Floating	VDDO	Reserved for system use. Leave this GPIO unconnected

5 Connections and optional external components

5.1 Power connections (VDDIN)

The CYBLE-3x307x-02 contains one power supply connection, VDDIN, which accepts a supply input range of 2.5 V to 3.6 V for CYBLE-3x307x-02. **Table 12** provides this specification. The maximum power supply ripple for this power connection is 100 mV, as shown in **Table 12**.

It is not required to place any power supply decoupling or noise reduction circuitry on the host PCB. If desired, an external ferrite bead between the supply and the module connection can be included, but is not necessary. If used, the ferrite bead should be positioned as close as possible to the module pin connection and the recommended ferrite bead value is 330 Ω, 100 MHz.

Considerations and Optional Components for Brown Out (BO) Conditions

Power supply design must be completed to ensure that the CYBLE-3x307x-02 module does not encounter a Brown Out condition, which can lead to unexpected functionality, or module lock up. A Brown Out condition may be met if power supply provided to the module during power up or reset is in the following range:

$$V_{IL} \leq VDDIN \leq V_{IH}$$

Refer to **Table 13** for the V_{IL} and V_{IH} specifications.

System design should ensure that the condition above is not encountered when power is removed from the system. In the event that this cannot be guaranteed (that is, battery installation, high-value power capacitors with slow discharge), it is recommended that an external voltage detection device be used to prevent the Brown Out voltage range from occurring during power removal. Refer to **Figure 8** for the recommended circuit design when using an external voltage detection IC.

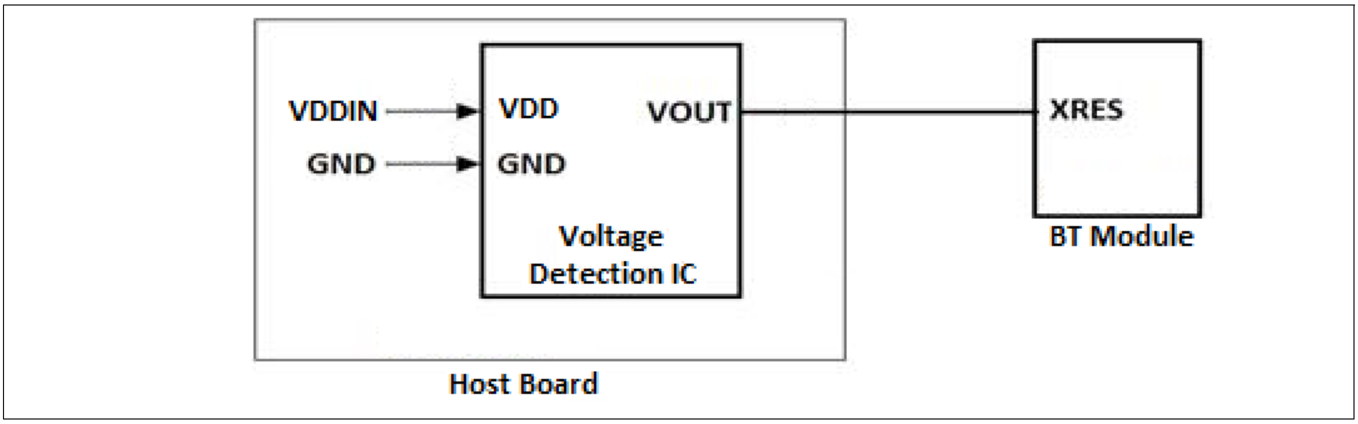


Figure 8 Reference circuit block diagram for external voltage detection IC

In the event that the module does encounter a Brown Out condition, and is operating erratically or is not responsive, power cycling the module will correct this issue and once reset, the module should operate correctly. Brown Out conditions can potentially cause issues that cannot be corrected, but in general, a power-on-reset operation will correct a Brown Out condition.

5.2 External reset (XRES)

The CYBLE-3x307x-02 has an integrated power-on reset circuit, which completely resets all circuits to a known power-on state. This action can also be evoked by an external reset signal, forcing it into a power-on reset state. The XRES signal is an active-low signal, which is an input to the CYBLE-3x307x-02 module (solder pad 3). The CYBLE-3x307x-02 module does not require an external pull-up resistor on the XRES input

During power-on operation, the XRES connection to the CYBLE-3x307x-02 is required to be held low 50 ms after the VDD power supply input to the module is stable. This can be accomplished in the following ways:

- The host device should connect a GPIO to the XRES of the CYBLE-3x307x-02 module and pull XRES low until VDD is stable. XRES is recommended to be released 50 ms after VDDIN is stable.

- If the XRES connection of the CYBLE-3x307x-02 module is not used in the application, a 10-µF capacitor may be connected to the XRES solder pad of the CYBLE-3x307x-02 to delay the XRES release. The capacitor value for this recommended implementation is approximate, and the exact value may differ depending on the VDDIN power supply ramp time of the system. The capacitor value should result in an XRES release timing of 50 ms after VDDIN stability.
- The XRES release timing may be controlled by an external voltage detection IC. XRES should be released 50 ms after VDD is stable.

Refer to **Figure on page 23** for XRES operating and timing requirements during power-on events.

Figure 9 illustrates the CYBLE-3x307x-02 schematic.

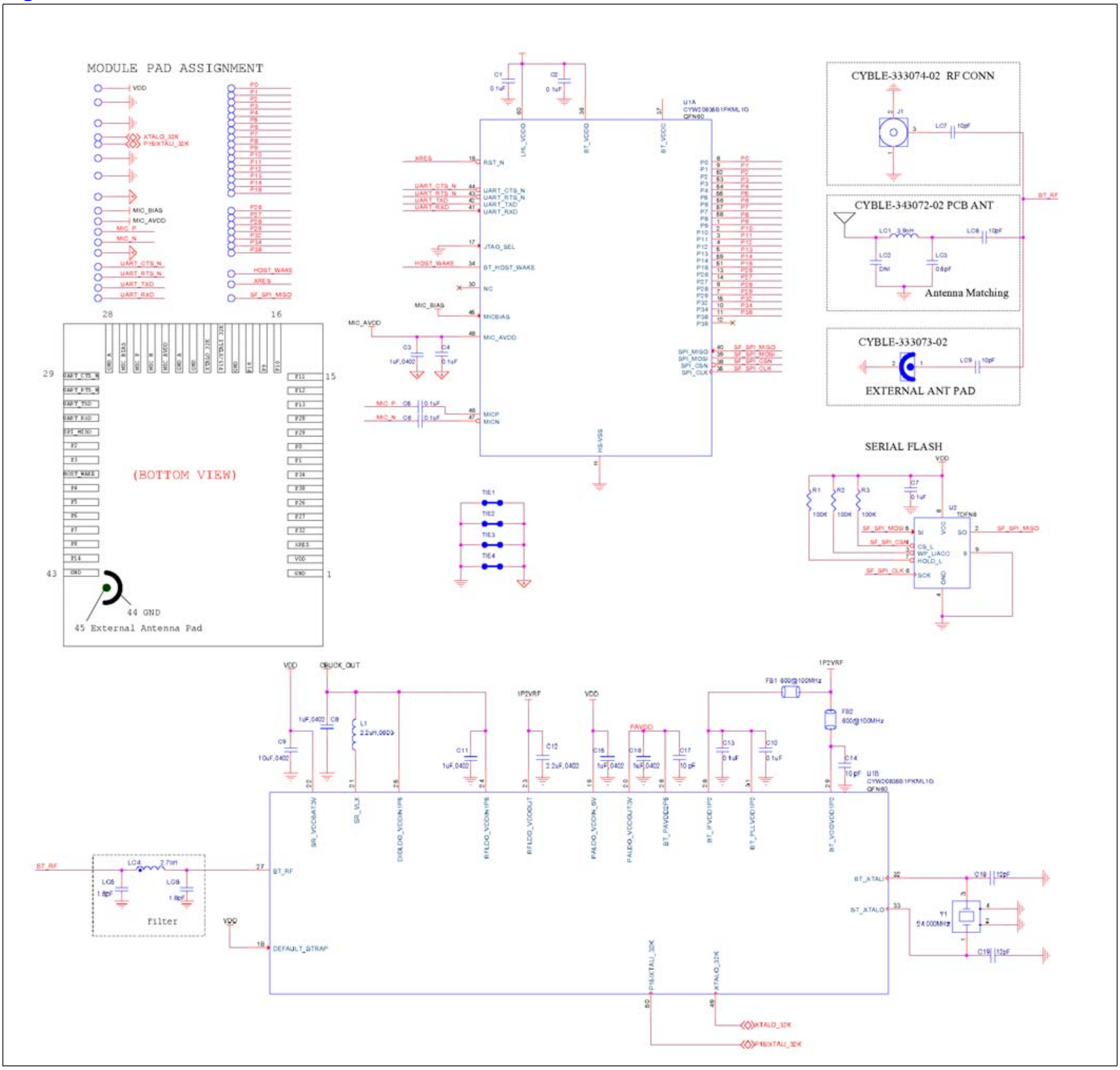


Figure 9 **CYBLE-3x307x-02 schematic diagram**

5.3 Critical components list

Table 6 details the critical components used in the CYBLE-3x307x-02 module.

Table 6 **Critical component list**

Component	Reference designator	description
Silicon	U1	60-pin QFN Bluetooth®/Bluetooth® LE silicon device - CYW20835
Silicon	U2	8-pin TDF8N, 512K Serial Flash
Crystal	Y1	24.000 MHz, 12PF

5.4 Antenna design

Table 7 details trace antenna used in the CYBLE-3x307x-02 module. For more information, see **Table 7**.

Table 7 Trace antenna specifications

Item	Description
Frequency range	2400–2500 MHz
Peak gain	–0.5-dBi typical
Return loss	10-dB minimum

6 Functional description

6.1 Bluetooth® baseband core

The Bluetooth® baseband core (BBC) implements all of the time-critical functions required for high-performance Bluetooth® LE 5.0 operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules LL and TX/RX transactions, monitors Bluetooth® LE 5.0 slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

Table 8 Bluetooth® features

Bluetooth® Low Energy 4.1	Bluetooth® Low Energy 4.2	Bluetooth® Low Energy 5.0
Bluetooth® Low Energy	Data packet length extension	Bluetooth® LE 2 Mbps
Low duty cycle advertising	LE secure connection	
LE-HID		
LE master and slave		
Common profiles	**Common profiles**	**Common profiles**
GATT	GATT	GATT, ATT
ATT	ATT	MESH
FMP	FMP	FMP
HOGP	HOGP	HOGP
HTP	HTP	HTP
PXP	PXP	PXP

6.1.1 Link control layer

The link control layer is part of the Bluetooth® LE 5.0 link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state or substate in the Bluetooth® Low Energy Link Controller.

- Bluetooth® LE states:
  - Advertising
  - Scanning
  - Connection
- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan

6.1.2 Test mode support

The CYBLE-3x307x-02 fully supports the Bluetooth® Test mode as described in Part I:1 of the Specification of the Bluetooth® System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth® Test Mode, the CYBLE-3x307x-02 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment.

6.1.3 Frequency hopping generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth® clock, and device address.

6.2 Microcontroller unit

The CYW20835 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is a Cortex-M4 32-bit RISC processor with embedded ICE-RT debug and serial wire debug (SWD) interface units.

The microprocessor also includes 2 MB of ROM memory for program storage and 384 KB of RAM for data scratch-pad. The internal ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At powerup, the lower-layer protocol stack is executed from internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and feature additions. The device also supports the integration of user applications and profiles.

6.2.1 Floating point unit

CYW20835 includes the CM4 single precision IEEE-754 compliant floating point unit. For details, see the Cortex-M4 manual.

6.2.2 OTP memory

The CYW20835 includes 2 KB of one-time programmable memory that can be used by the factory to store product-specific information.

Note Use of OTP requires that a 3V supply be present at all times.

6.2.3 NVRAM configuration data and storage

NVRAM contains configuration information about the customer application, including the following:

- Fractional-N information
- BD_ADDR
- UART baud rate
- SDP service record

- File system information used for code, code patches, or data. The CYW20835 uses SPI Serial Flash for NVRAM storage.

6.2.4 Power-on reset (POR)

The CYW20835 includes POR logic to allow the part to initialize correctly when power is applied. **Figure 10** shows the sequence used by the CYW20835 during initialization. An small external cap may be used on RESET_N to add delay as VDDIO ramps up.

6.3 External reset (XRES)

The CYBLE-3x307x-02 has an integrated power-on reset circuit that completely resets all circuits to a known power-on state. An external active low reset signal, XRES, can be used to put the CYBLE-3x307x-02 in the reset state. The XRES pin has an internal pull-up resistor and, in most applications, it does not require anything to be connected to it.

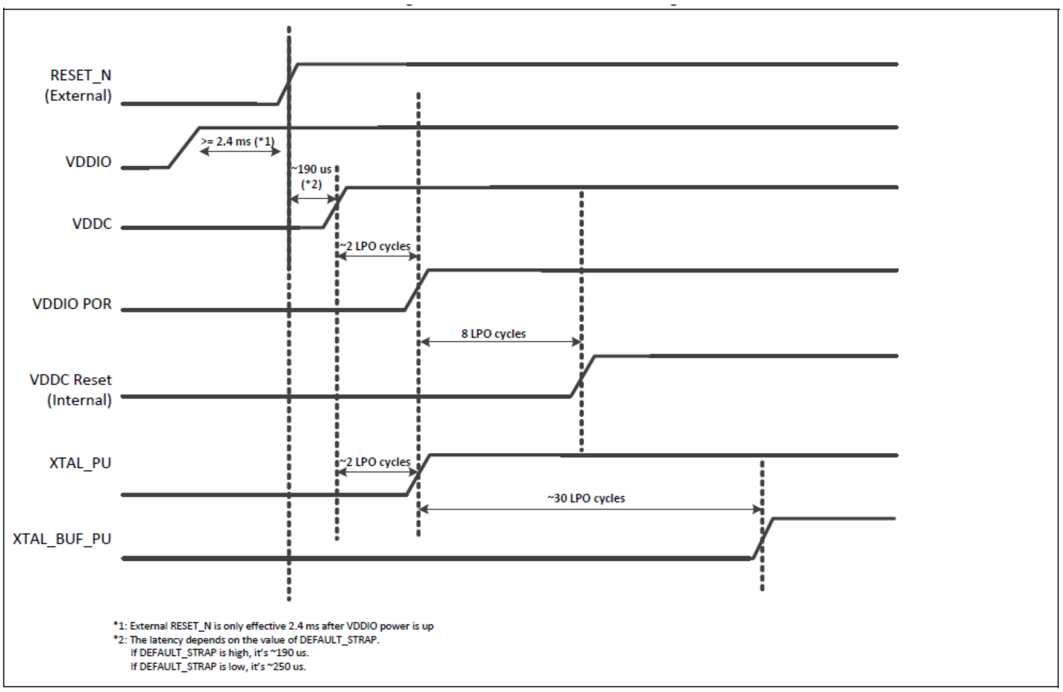


Figure 10 Power-on reset timing

6.3.1 Brownout detection

An external voltage detector reset IC may be used if brownout detection is required. The reset IC should release RESET_N only after the VDDO supply voltage level has been at or above a minimum operating voltage for 50 ms or longer.

7 Integrated radio transceiver

The CYBLE-3x307x-02 has an integrated radio transceiver that has been optimized for use in 2.4-GHz Bluetooth® wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4-GHz unlicensed ISM band. The CYBLE-3x307x-02 is fully compliant with the Bluetooth® LE 5.0 Radio Specification and meets or exceeds the requirements to provide the highest communication link quality of service.

7.1 Transmitter path

The CYBLE-3x307x-02 features a fully integrated transmitter. The baseband transmit data is GFSK modulated in the 2.4 GHz ISM band.

7.1.1 Digital modulator

The digital modulator performs the data modulation and filtering required for the GFSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal.

7.1.2 Power amplifier

The CYW20835 has an integrated power amplifier (PA) that can transmit up to +10 dBm for class 1 operations.

7.2 Receiver path

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the CYBLE-3x307x-02 to be used in most applications with minimal off-chip filtering.

7.2.1 Digital demodulator and bit synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

7.2.2 Receiver signal strength indicator

The radio portion of the CYBLE-3x307x-02 provides a receiver signal strength indicator (RSSI) to the baseband. This enables the controller to take part in a Bluetooth® power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

7.3 Local oscillator generation

The local oscillator (LO) provides fast frequency hopping (1600 hops/second) across the 39 maximum available channels. The LO generation sub-block employs an architecture for high immunity to LO pulling during PA operation. The CYBLE-3x307x-02 uses an internal loop filter.

7.4 Calibration

The CYBLE-3x307x-02 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration tunes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops, and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

8 Peripheral and communication interfaces

8.1 I^2C communication interface

The CYBLE-3x307x-02 provides a 2-pin master I^2C interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mouse devices. This interface is compatible with I^2C slave devices. I^2C does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by the I^2C:

- 100 kHz
- 400 kHz
- 800 kHz (not a standard I^2C-compatible speed.)
- 1 MHz (Compatibility with high-speed I^2C-compatible devices is not guaranteed.)

The following transfer types are supported by the I^2C:

- Read (Up to 8 bytes can be read)
- Write (Up to 8 bytes can be written)
- Read-then-Write (Up to 8 bytes can be read and up to 8 bytes can be written)
- Write-then-Read (Up to 8 bytes can be written and up to 8 bytes can be read)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pad (I2C_SCL) and data pad 2 (I2C_SDA) are both open-drain I/O pins. Pull-up resistors, external to the CYBLE-3x307x-02, are required on both the SCL and SDA pad for proper operation.

8.2 HCI UART interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 57600 bps to 6 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The CYBLE-3x307x-02 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth® UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 6 Mbps. The baud rate of the CYBLE-3x307x-02 UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

Table 9 contains example values to generate common baud rates with a 24 MHz UART clock.

Table 9 Common baud rate examples, 24 MHz clock

Baud rate (bps)	Baud rate adjustment		Mode	Error (%)
	High nibble	Low nibble		
3M	0xFF	0xF8	High rate	0.00
2M	0XFF	0XF4	High rate	0.00
1M	0X44	0XFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16

Table 9 Common baud rate examples, 24 MHz clock *(continued)*

Baud rate (bps)	Baud rate adjustment		Mode	Error (%)
	High nibble	Low nibble		
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16
38400	0x01	0x00	Normal	0.00

Table 10 contains example values to generate common baud rates with a 48 MHz UART clock.

Table 10 Common baud rate examples, 48 MHz clock

Baud rate (bps)	High rate	Low rate	Mode	Error (%)
6M	0xFF	0xF8	High rate	0
4M	0xFF	0xF4	High rate	0
3M	0x0	0xFF	Normal	0
2M	0x44	0xFF	Normal	0
1.5M	0x0	0xFE	Normal	0
1M	0x0	0xFD	Normal	0
921600	0x22	0xFD	Normal	0.16
230400	0x0	0xF3	Normal	0.16
115200	0x1	0xE6	Normal	–0.08
57600	0x1	0xCC	Normal	0.04

Normally, the UART baud rate is set by a configuration record downloaded after reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The CYBLE-3x307x-02 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

8.3 Triac control

The CYBLE-3x307x-02 includes hardware support for zero-crossing detection and trigger control for up to four triacs. The CYBLE-3x307x-02 detects zero-crossing on the AC zero detection line and uses that to provide a pulse that is offset from the zero crossing. This allows the CYBLE-3x307x-02 to be used in dimmer applications, as well as any other applications that require a control signal that is offset from an input event.

The zero-crossing hardware includes an option to suppress glitches.

8.4 Peripheral UART interface

The CYBLE-3x307x-02 has a second UART that may be used to interface to peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin. The CYBLE-3x307x-02 can map the peripheral UART to any LHL GPIO. The peripheral UART clock is fixed at 24 MHz. Both TX and RX have a 256-byte FIFO (see **Table 4 on page 14**).

8.5 Serial peripheral interface

The CYBLE-3x307x-02 has two independent SPI interfaces, both of which support single, dual, and quad mode SPI operations. Either interface can be a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the CYBLE-3x307x-02 has optional I/O ports that can be configured individually and separately for each functional pin. The CYBLE-3x307x-02 acts as an

SPI master device that supports 1.8 V or 3.3 V SPI slaves. The CYBLE-3x307x-02 can also act as an SPI slave device that supports a 1.8 V or 3.3 V SPI master.

Note SPI voltage depends on VDDO/VDDM; therefore, it defines the type of devices that can be supported.

8.6 Infrared modulator

The CYBLE-3x307x-02 includes hardware support for infrared TX. The hardware can transmit both modulated and unmodulated waveforms. For modulated waveforms, hardware inserts the desired carrier frequency into all IR transmissions. IR TX can be sourced from firmware-supplied descriptors, a programmable bit, or the peripheral UART transmitter.

If descriptors are used, they include IR on/off state and the duration between 1–32767/µs. The CYBLE-3x307x-02 IR TX firmware driver inserts this information in a hardware FIFO and makes sure that all descriptors are played out without a glitch due to under run (see **Figure 11**).

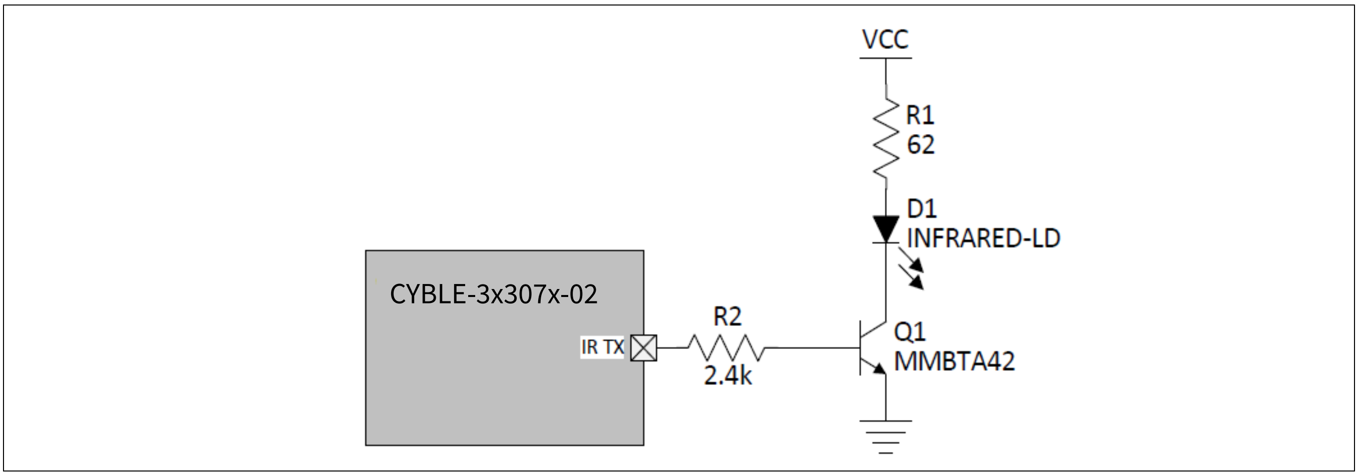


Figure 11 **Infrared TX**

8.7 PDM microphone

The CYBLE-3x307x-02 accepts a ΣΔ-based one-bit pulse density modulation (PDM) input stream and outputs filtered samples at either 8 kHz or 16 kHz sampling rates. The PDM signal derives from an external kit that can process analog microphone signals and generate digital signals. The digital signal passes through the chip IO and MUX inputs using an aux ADC signal. The PDM shares the filter path with the aux ADC.

Two types of data rates can be supported:

- 8 kHz
- 16 kHz

The external digital microphone accepts a 2.4 MHz clock generated by the CYBLE-3x307x-02 and outputs a PDM signal which is registered by the PDM interface with either the rising or falling edge of the 2.4 MHz clock selectable through a programmable control bit. The design can accommodate two simultaneous PDM input channels, so stereo voice is possible.

8.8 Security engine

The CYBLE-3x307x-02 includes a hardware security accelerator that greatly decreases the time required to perform typical security

operations. These functions include:

- Public key acceleration (PKA) cryptography
- AES-CTR/CBC-MAC/CCM acceleration
- SHA2 message hash and HMAC acceleration

- RSA encryption and decryption of modulus sizes up to 2048 bits
- Elliptic curve Diffie-Hellman in prime field GF(p)
- Generic modular math functions

9 Keyboard scanner

The keyboard scanner is designed to autonomously sample keys and store them into buffer registers without the need for the host microcontroller to intervene. The scanner has the following features:

- Ability to turn off its clock if no keys are pressed.
- Sequential scanning of up to 160 keys in an 8 × 20 matrix.
- Programmable number of columns from 1 to 20.
- Programmable number of rows from 1 to 8.
- 16-byte key code buffer (can be augmented by firmware).
- 128 kHz clock that allows scanning of full 160-key matrix in about 1.2 ms.
- N-key rollover with selective 2-key lockout if ghost is detected.
- Keys are buffered until host microcontroller has a chance to read it, or until overflow occurs.
- Hardware debouncing and noise/glitch filtering.
- Low-power consumption. Single-digit µA-level sleep current.

9.1 Theory of operation

The key scan block is controlled by a state machine with the following states: Idle, Scan, and Scan End.

9.1.1 Idle

The state machine begins in the idle state. In this state, all column outputs are driven high. If any key is pressed, a transition occurs on one of the row inputs. This transition causes the 128 kHz clock to be enabled (if it is not already enabled by another peripheral) and the state machine to enter the scan state. Also in this state, an 8-bit row-hit register and an 8-bit key-index counter is reset to '0'.

9.1.2 Scan

In the scan state, a row counter counts from 0 up to a programmable number of rows minus 1. After the last row is reached, the row counter is reset and the column counter is incremented. This cycle repeats until the row and column counters are both at their respective terminal count values. At that point, the state machine moves into the Scan-End state.

As the keys are being scanned, the key-index counter is incremented. This counter value is compared to the modifier key codes stored in RAM, or in the key code buffer if the key is not a modifier key. It can be used by the microprocessor as an index into a lookup table of usage codes.

Also, as the nth row is scanned, the row-hit register is ORed with the current 8-bit row input values if the current column contains two or more row hits. During the scan of any column, if a key is detected at the current row, and the row-hit register indicates that a hit was detected in that same row on a previous column, then a ghost condition may have occurred, and a bit in the status register is set to indicate this.

9.1.3 Scan End

This state determines whether any keys were detected while in the scan state. If yes, the state machine returns to the scan state. If no, the state machine returns to the idle state, and the 128 kHz clock request signal is made inactive.

Note The microcontroller can poll the key status register.

9.2 Mouse quadrature signal decoder

The mouse signal decoder is designed to autonomously sample two quadrature signals commonly generated by an optomechanical mouse. The decoder has the following features:

- Three pairs of inputs for X, Y, and Z (typical scroll wheel) axis signals. Each axis has two options:

  - For the X axis, choose P2 or P32 as X0 and P3 or P33 as X1.
  - For the Y axis, choose P4 or P34 as Y0 and P5 or P35 as Y1.
  - For the Z axis, choose P6 or P36 as Z0 and P7 or P37 as Z1.

- Control of up to four external high-current GPIOs to power external optoelectronics:
  - Turn-on and turn-off time can be staggered for each HC-GPIO to avoid simultaneous switching of high currents and having multiple high-current devices on at the same time.
  - Sample time can be staggered for each axis.
  - Sense of the control signal can be active high or active low.
  - Control signal can be tristated for off condition or driven high or low, as appropriate.

9.3 Theory of operation

The mouse decoder block has four 10-bit PWMs for controlling external quadrature devices and sampling the quadrature inputs at its core.

The GPIO signals may be used to control such items as LEDs, external ICs that may emulate quadrature signals, photodiodes, and photodetectors.

9.4 ADC port

The ADC block is a single switched-cap Σ-Δ ADC core for audio and DC measurement. It operates at the 12 MHz clock rate and has 32 DC input channels, including 28 GPIO inputs. The internal bandgap reference has ±5% accuracy without calibration. Different calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

10 Clock frequencies

The CYBLE-3x307x-02 has an integrated 24-MHz crystal on the module. There is no need to add an additional crystal oscillator.

11 GPIO port

GPIO ports for this device is shown in Table 4-2. The CYBLE-3x307x-02 uses 24 general-purpose I/Os (GPIOs). All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3 V or 4 mA at 1.8 V, except P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3 V or 8 mA at 1.8 V.

P28-P29, P32, P34, P38: all of these pins can be programmed as ADC inputs.

Port 26-Port 29: All four of these pins are capable of sinking up to 16 mA for LEDs. These pins also have the PWM function, which can be used for LED dimming.

12 PWM

The CYBLE-3x307x-02 has four PWMs. The PWM module consists of the following:

- PWM0-5. Each of the six PWM channels contains the following registers:
  - 16-bit initial value register (read/write)
  - 16-bit toggle register (read/write)
  - 16-bit PWM counter value register (read)
- PWM configuration register shared among PWM0-5 (read/write). This 18-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 12 shows the structure of one PWM.

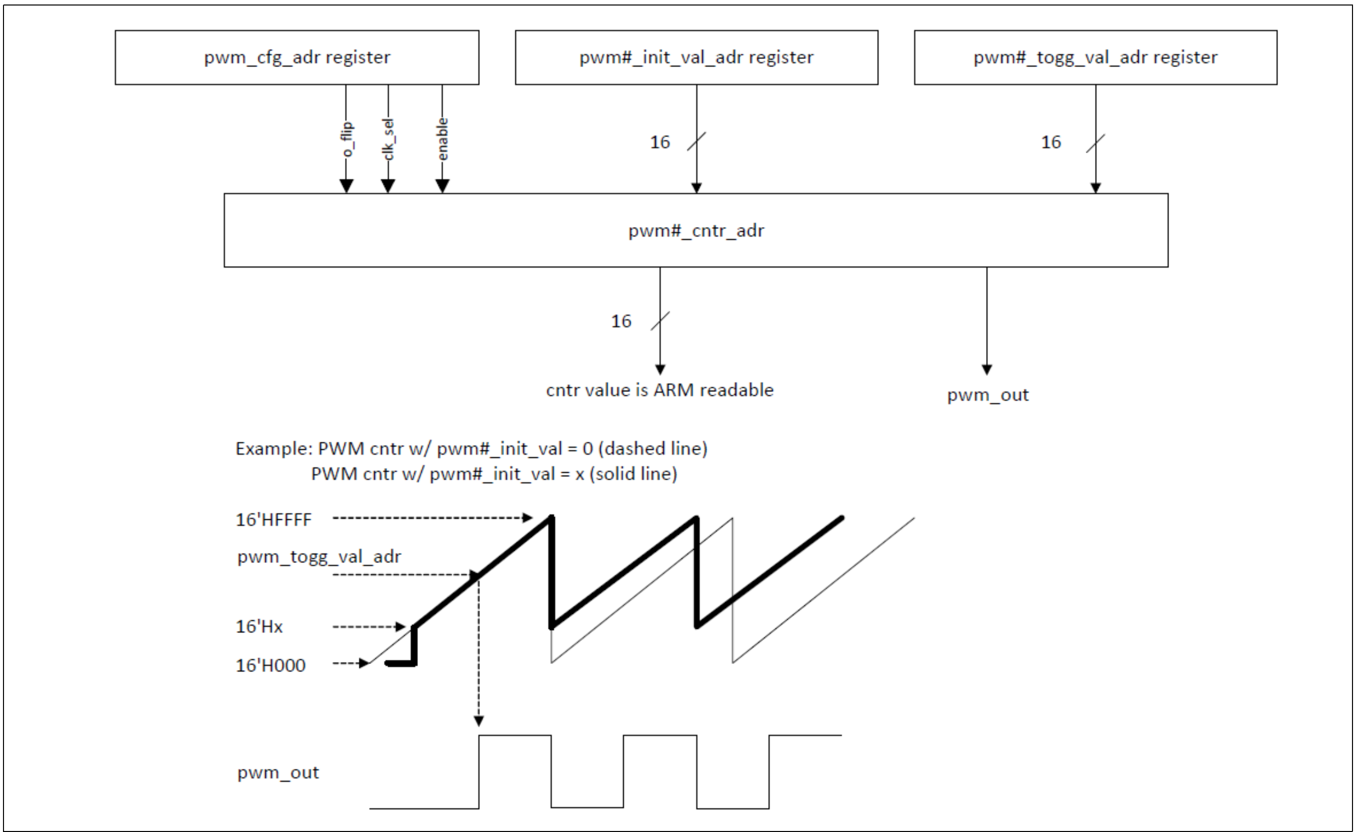


Figure 12 PWM block diagram

13 Power management unit

The Power management unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

13.1 RF power management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4-GHz transceiver, which then processes the power-down functions accordingly.

13.2 Host controller power management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in Deep Sleep (HIDOFF) mode.

13.3 BBC power management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth®-specified low-power connection mode. While in these low-power connection modes, the CYBLE-3x307x-02 runs on the low power oscillator and wakes up after a predefined time period.

The CYBLE-3x307x-02 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDOFF (Deep Sleep) mode

The CYBLE-3x307x-02 transitions to the next lower state after a programmable period of user inactivity. Busy mode is immediately entered when user activity resumes.

In HIDOFF (Deep Sleep) mode, the CYBLE-3x307x-02 baseband and core are powered off by disabling power to VDDC_OUT and PAVDD. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

14 Electrical characteristics

Table 11 shows the maximum electrical rating for voltages referenced to V_{DDIN} pad.

Table 11 Maximum electrical rating

Rating	Symbol	Value	Unit
V_{DDIN}	–	3.795	V
Voltage on input or output pin	–	VSS – 0.3 to VDD + 0.3	
Operating ambient temperature range	T_{opr}	–30 to +85	°C
Storage temperature range	T_{stg}	–40 to +85	

Table 12 shows the power supply characteristics for the range T_J = 0 to 125 °C.

Table 12 Power supply

Parameter	Description	Min[6]	Typ	Max[6]	Unit
V_{DDIN}	Power supply input (CYBLE-3x307x-02)	2.5	–	3.6	V
V_{DDIN_RIPPLE}	Maximum power supply ripple for V_{DDIN} input voltage	–	–	100	mV

Table 13 shows the specifications for the digital voltage levels.

Table 13 Digital Voltage Levels

Characteristics	Symbol	Min	Typ	Max	Unit
Input low voltage	V_{IL}	–	–	0.8	V
Input high voltage	V_{IH}	2.0	–	–	
Output low voltage	V_{OL}	–	–	0.4	
Output high voltage	V_{OH}	V_{DDIN} – 0.4	–	–	
Input capacitance (V_{DDMEM} domain)	C_{IN}	–	–	0.4	pF

Table 14 shows the current consumption measurements

Table 14 Bluetooth® LE current consumption

Operational mode	Conditions	Typ	Unit
Receiving	Receiver and baseband are both operating, 100% ON.	8	mA
Transmitting@12 dBm	Transmitter and baseband are both operating, 100% ON.	18	
Advertising	1.28s direct advertising in low power idle mode	30	µA
Scanning	TBD	TBD	mA
Connecting	1-second connection interval in low power idle mode	25	µA
HIDOFF (Deep Sleep)	–	1	

Note

6. Overall performance degrades beyond minimum and maximum supply voltages.The voltage range specified is determined by the minimum and maximum operating voltage of the SPI Serial Flash included on the module.

15 Chipset RF specifications

All specifications in **Table 15** are for industrial temperatures and are single-ended. Unused inputs are left open.

Table 15 Receiver RF Specifications

Parameter	Conditions	Min	Typ[7]	Max	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity[8]	–	–	–91.5	–	–
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Interference performance					
TBD					
Out-of-band blocking performance (CW)[9]					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	
2498–3000 MHz	0.1% BER	–	–27	–	
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	
Intermodulation performance[10]					
BT, Df = 4 MHz	–	–39.0	–	–	dBm
Spurious Emissions[11]					
30 MHz to 1 GHz	–	–	–	–62	dBm
1 GHz to 12.75 GHz	–	–	–	–47	
65 MHz to 108 MHz	FM RX	–	–147	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–147	–	
851–894 MHz	CDMA	–	–147	–	
925–960 MHz	EDGE/GSM	–	–147	–	
1805–1880 MHz	EDGE/GSM	–	–147	–	
1930–1990 MHz	PCS	–	–147	–	
2110–2170 MHz	WCDMA	–	–147	–	

Notes

7. Typical operating conditions are 1.22-V operating voltage and 25°C ambient temperature.
8. The receiver sensitivity is measured at BER of 0.1% on the device interface.
9. Meets this specification using front-end band pass filter.
10. f0 = –64 dBm Bluetooth®-modulated signal, f1 = –39 dBm sine wave, f2 = –39 dBm Bluetooth®-modulated signal, f0 = 2f1 – f2, and |f2 – f1| = n*1 MHz, where n is 3, 4, or 5. For the typical case, n = 4.
11. Includes baseband radiated emissions.

Table 16 Transmitter RF Specifications (TBD)

Parameter	Conditions	Min	Typ	Max	Unit
General					
Frequency range	–	2402	–	2480	MHz
Class 1: GFSK TX power	–	–	10	–	dBm
Power control step	–	2	4	8	dB
Out-of-Band Spurious Emissions					
30 MHz to 1 GHz	–	–	–	–36.0[12]	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0[13]	
1.8 GHz to 1.9 GHz	–	–	–	–47.0	
5.15 GHz to 5.3 GHz	–	–	–	–47.0	

Notes

12. Maximum value is the value required for Bluetooth® qualification.
13. Meets this spec using a front-end band-pass filter.

Table 17 Bluetooth® LE RF Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	N/A	2402	–	2480	MHz
RX sense[14]	GFSK, 0.1% BER, 1 Mbps	–	–94.5	–	dBm
TX power	N/A	–	12	–	
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max[15]	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	

Notes

14. Dirty TX is OFF.
15. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

16 Timing and AC characteristics

In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

16.1 UART timing

Table 18 UART timing specifications

Reference	Characteristics	Min	Max	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	1.50	Baud periods
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	0.67	
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	1.33	

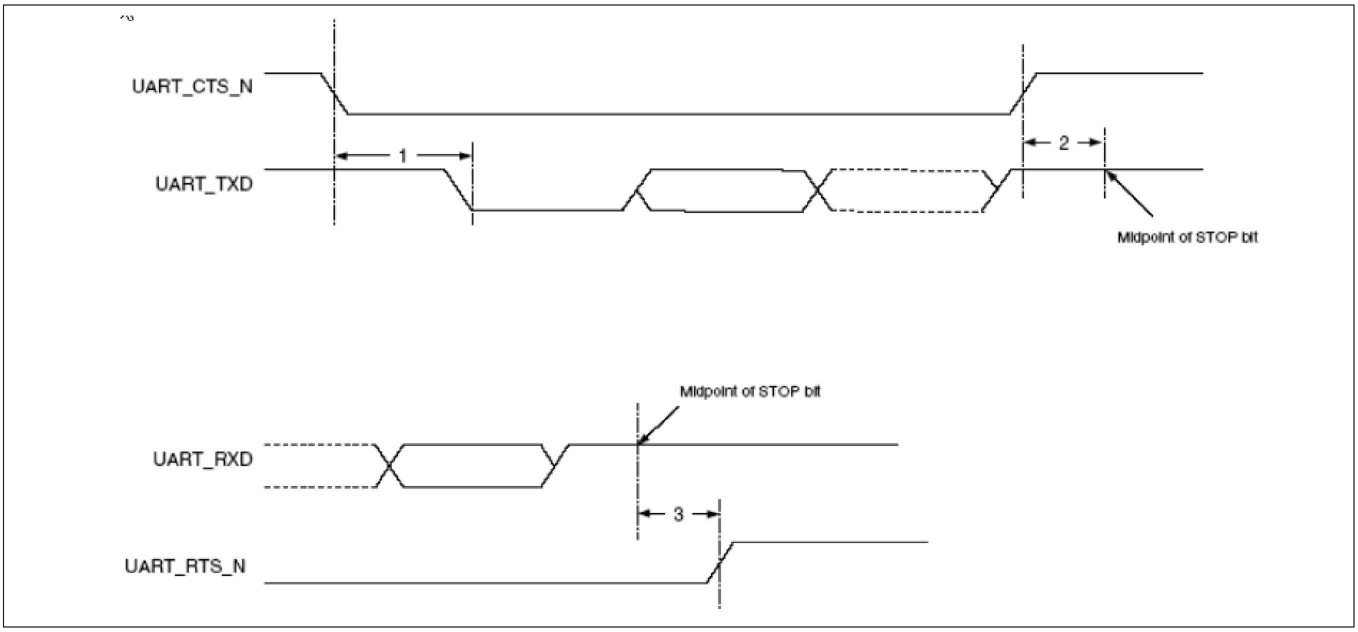


Figure 13 UART timing

16.2 SPI timing

The SPI interface supports clock speeds up to 12 MHz

Table 19 and Figure 14 show the timing requirements when operating in SPI Mode 0 and 2, and SPI Mode 1 and 3, respectively.

Table 19 SPI mode 0 and 2

Reference	Characteristics	Min	Max	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	∞	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	∞	
3	Time from master assert SPI_CSN to first clock edge	20	∞	
4	Setup time for MOSI data lines	8	½ SCK	
5	Hold time for MOSI data lines	8	½ SCK	
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	∞	
8	Idle time between subsequent SPI transactions	1 SCK	∞	

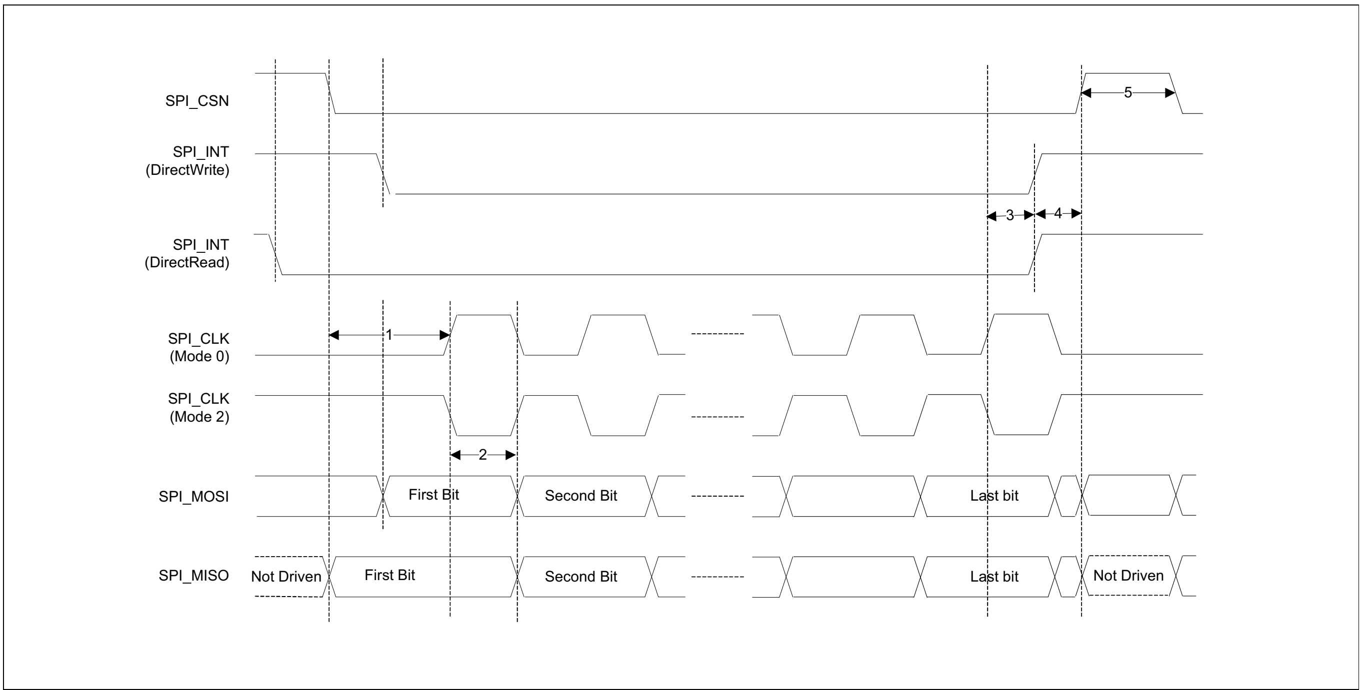


Figure 14 SPI timing – mode 0 and 2

Table 20 and **Figure 15** show the timing requirements when operating in SPI Mode 1 and 3.

Table 20 SPI mode 1 and 3

Reference	Characteristics	Min	Max	Unit
1	Time from master assert SPI_CSN to first clock edge	45	–	ns
2	Hold time for MOSI data lines	12	½ SCK	
3	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	
4	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	–	
5	Idle time between subsequent SPI transactions	1 SCK	–	

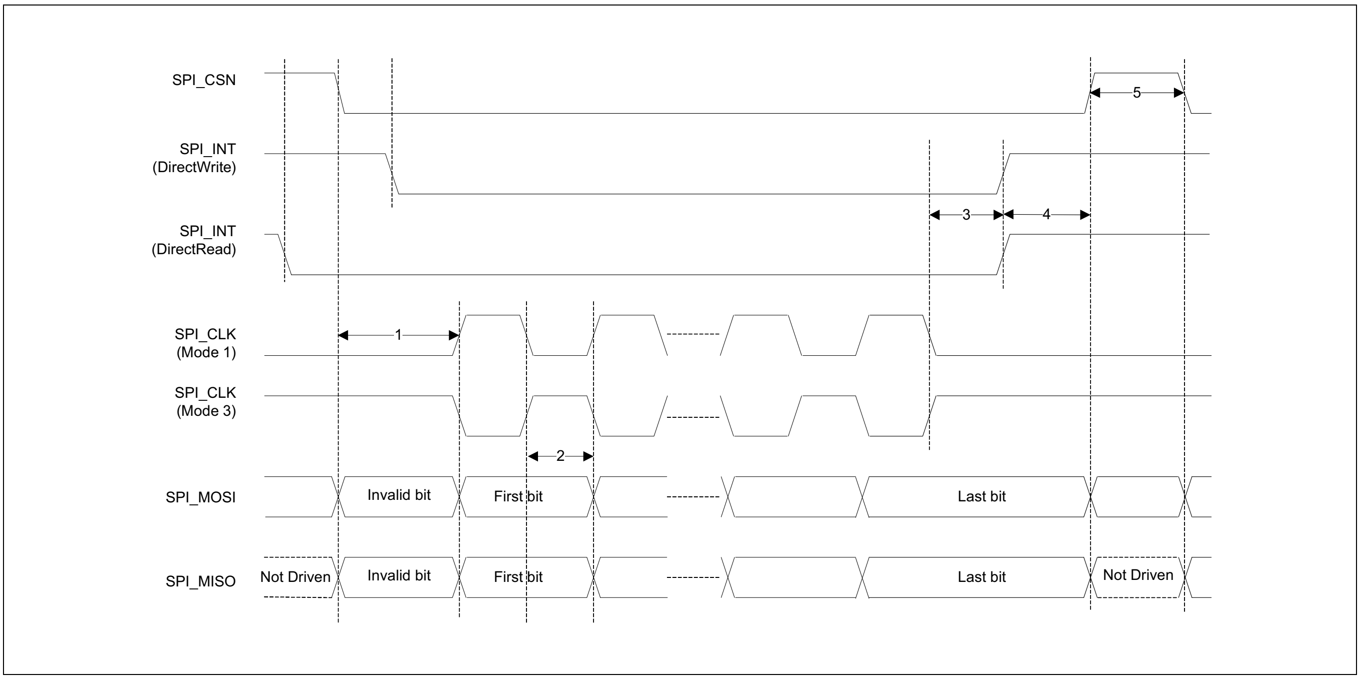


Figure 15 SPI timing – mode 1 and 3

16.3 I²C interface timing

Table 21 I²C Interface Timing Specifications

Reference	Characteristics	Min	Max	Unit
1	Clock frequency	–	100	kHz
			400	
			800	
			1000	
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	
4	Clock low time	650	–	
5	Clock high time	280	–	
6	Data input hold time[16]	0	–	
7	Data input setup time	100	–	
8	STOP condition setup time	280	–	
9	Output valid from clock	–	400	
10	Bus free time[17]	650	–	

Notes

16. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
17. Time that the bus must be free before a new transaction can start.

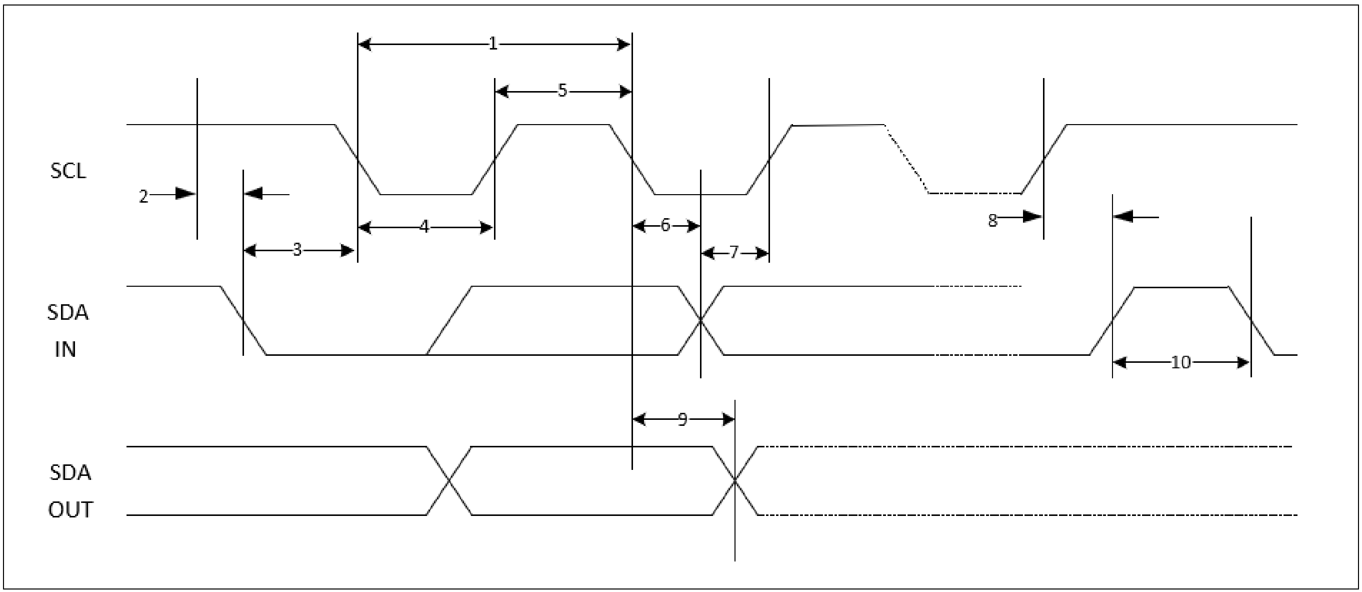


Figure 16 I²C Interface timing diagram

Table 22 Timing for I^2S transmitters and receivers

	Transmitter				Receiver				Notes
	Lower limit		Upper limit		Lower limit		Upper limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	–	–	–	T_r	–	–	–	18
Master mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	19
LOWt_{LC}	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	19
Slave mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	20
LOW t_{LC}	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	20
Rise time t_{RC}	–	–	$0.15T_{tr}$	–	–	–		–	21
Transmitter									
Delay t_{dtr}	–	–	–	0.8T	–	–	–	–	22
Hold time t_{htr}	0	–	–	–	–	–	–	–	21
Receiver									
Setup time t_{sr}	–	–	–	–	–	$0.2T_r$	–	–	23
Hold time t_{hr}	–	–	–	–	–	0	–	–	22

Notes

18. The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.
19. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} are specified with respect to T.
20. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_r$, any clock that meets the requirements can be used.
21. Because the delay (t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means t_{htr} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{htr} is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{tr}$.
22. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
23. The data setup and hold time must not be less than the specified receiver setup and hold time.

Note The time periods specified in **Figure 17** and **Figure 18** are defined by the transmitter speed. The receiver specifications must match transmitter performance.

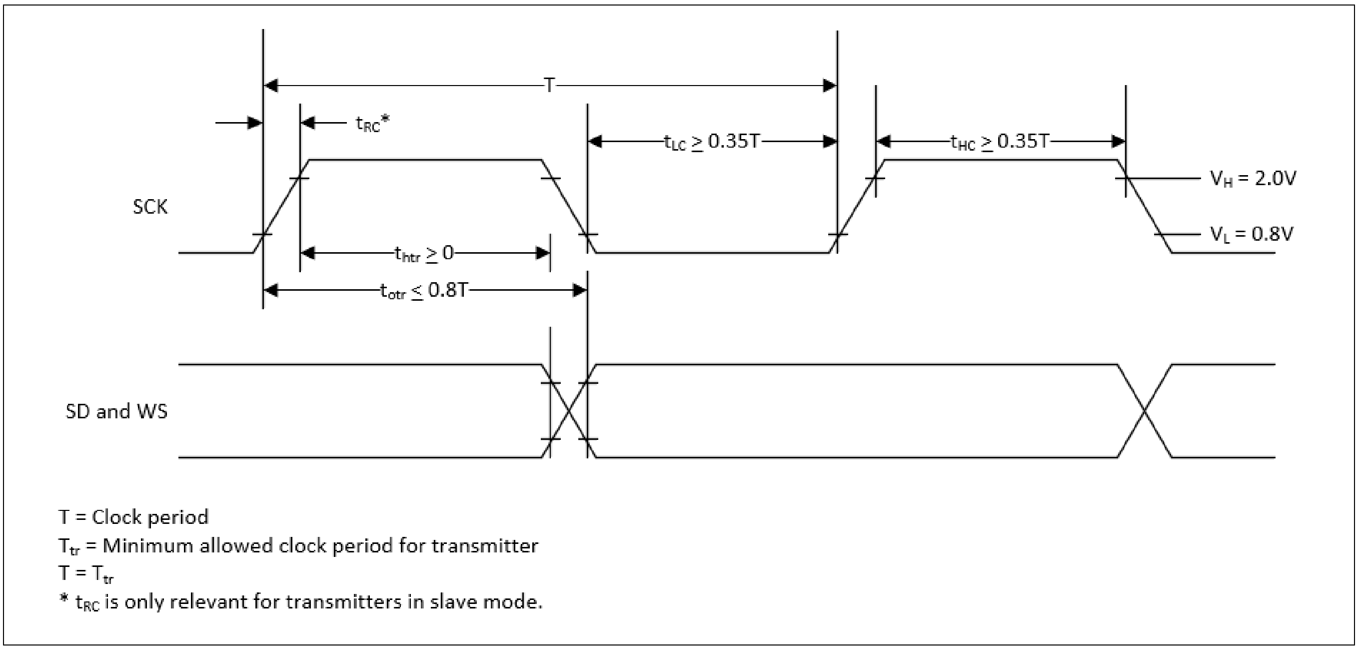


Figure 17 I^2S transmitter timing

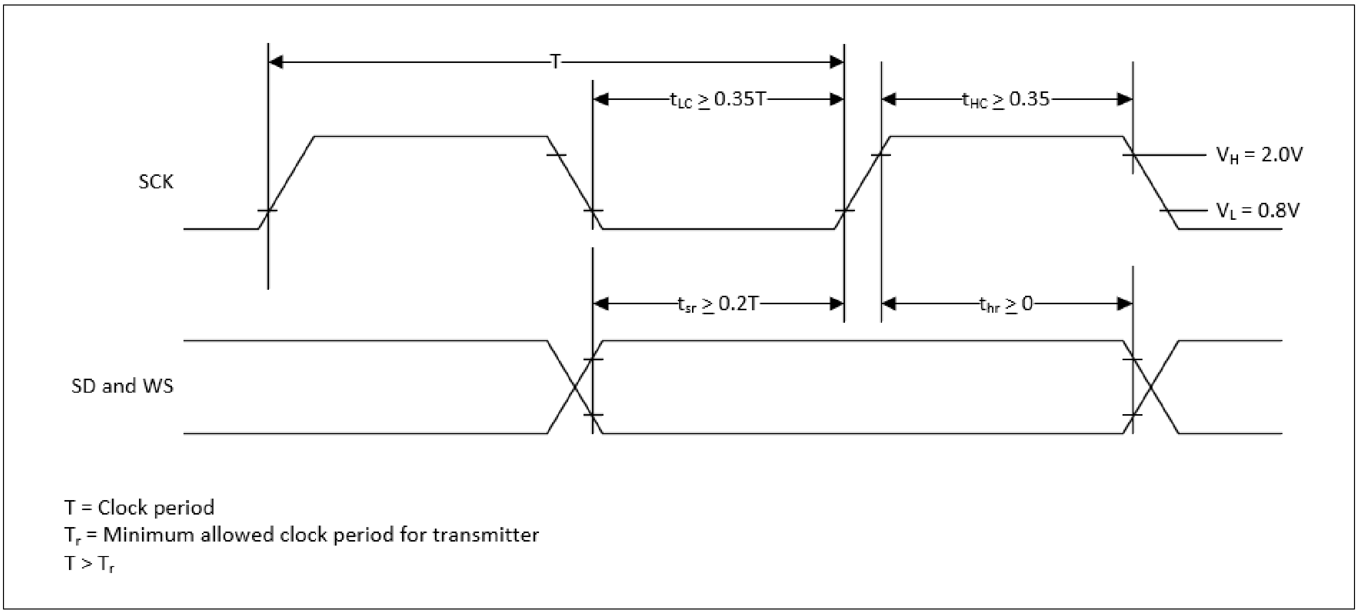


Figure 18 I^2S receiver timing

17 Environmental specifications

17.1 Environmental compliance

This CYBLE-3x307x-02 Bluetooth® LE module is produced in compliance with the Restriction of Hazardous Substances (RoHS) and Halogen-Free (HF) directives. The Infineon module and components used to produce this module are RoHS and HF compliant.

17.2 RF certification

The CYBLE-3x307x-02 module will be certified under the following RF certification standards at production release.

- FCC: TBD
- CE
- IC: TBD
- MIC: TBD

17.3 Safety certification

The CYBLE-3x307x-02 module complies with the following safety regulations:

- Underwriters Laboratories, Inc. (UL): Filing E331901
- CSA
- TUV

17.4 Environmental conditions

Table 23 describes the operating and storage conditions for the Bluetooth® LE module.

Table 23 Environmental conditions for CYBLE-3x307x-02

Description	Minimum specification	Maximum specification
Operating temperature	–30 °C	85 °C
Operating humidity (relative, non-condensation)	5%	85%
Thermal ramp rate	–	3 °C/minute
Storage temperature	–40 °C	85 °C
Storage temperature and humidity	–	85 °C at 85%
ESD: Module integrated into end system Components[24]	–	15 kV Air 2.0 kV Contact

Note

24.This does not apply to the RF pins (ANT).

17.5 ESD and EMI protection

Exposed components require special attention to ESD and electromagnetic interference (EMI).

A grounded conductive layer inside the device enclosure is suggested for EMI and ESD performance. Any openings in the enclosure near the module should be surrounded by a grounded conductive layer to provide ESD protection and a low-impedance path to ground.

Device handling: Proper ESD protocol must be followed in manufacturing to ensure component reliability.

18 Regulatory information

18.1 FCC

FCC NOTICE:

The device CYBLE-3x307x-02 complies with Part 15 of the FCC Rules. The device meets the requirements for modular transmitter approval as detailed in FCC public Notice DA00-1407.transmitter Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

CAUTION:

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by Infineon may void the user's authority to operate the equipment.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help

This module is only FCC authorized for the specific rule FCC 15.247 listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification, final host product requires Part 15 Subpart B compliance testing with the modular transmitter installed.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that FCC labeling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Infineon FCC identifier for this product as well as the FCC Notice above. The FCC identifier is FCC ID: TBD.

In any case the end product must be labeled exterior with “Contains FCC ID: TBD”.

ANTENNA WARNING:

This device is tested with a standard SMA connector and with the antenna listed in **Table 7 on page 20**. When integrated in the OEMs product, these fixed antennas require installation preventing end-users from replacing them with non-approved antennas. Any antenna not in the following table must be tested to comply with FCC Section 15.203 for unique antenna connectors and Section 15.247 for emissions.

RF EXPOSURE:

To comply with FCC RF Exposure requirements, the Original Equipment Manufacturer (OEM) must ensure to install the approved antenna in the previous.

The preceding statement must be included as a CAUTION statement in manuals, for products operating with the approved antenna in **Table 7**, to alert users on FCC RF Exposure compliance. Any notification to the end user of installation or removal instructions about the integrated radio module is not allowed.

The radiated output power of CYBLE-3x307x-02 with the trace antenna is far below the FCC radio frequency exposure limits. Nevertheless, use CYBLE-3x307x-02 in such a manner that minimizes the potential for human contact during normal operation.

End users may not be provided with the module installation instructions. OEM integrators and end users must be provided with transmitter operating conditions for satisfying RF exposure compliance.

18.2 ISED

Innovation, Science and Economic Development Canada (ISED) Certification

CYBLE-3x307x-02 is licensed to meet the regulatory requirements of Innovation, Science and Economic Development Canada (ISED),

License: IC: TBD

Manufacturers of mobile, fixed, or portable devices incorporating this module are advised to clarify any regulatory questions and ensure compliance for SAR and/or RF exposure limits. Users can obtain Canadian information on RF exposure and compliance from **www.ic.gc.ca**.

This device has been designed to operate with the antennas listed in **Table 7 on page 20**, having a maximum gain of –0.5 dBi. Antennas not included in this list or having a gain greater than –0.5 dBi are strictly prohibited for use with this device. The required antenna impedance is 50 ohms. The antenna used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

ISED NOTICE:

The device CYBLE-3x307x-02 including the built-in trace antenna complies with Canada RSS-GEN Rules. The device meets the requirements for modular transmitter approval as detailed in RSS-GEN. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

L'appareil CYBLE-3x307x-02, y compris l'antenne intégrée, est conforme aux Règles RSS-GEN de Canada. L'appareil répond aux exigences d'approbation de l'émetteur modulaire tel que décrit dans RSS-GEN. L'opération est soumise aux deux conditions suivantes: (1) Cet appareil ne doit pas causer d'interférences nuisibles, et (2) Cet appareil doit accepter toute interférence reçue, y compris les interférences pouvant entraîner un fonctionnement indésirable.

ISED INTERFERENCE STATEMENT FOR CANADA

This device complies with Innovation, Science and Economic Development (ISED) Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Cet appareil est conforme à la norme sur l'innovation, la science et le développement économique (ISED) norme RSS exempte de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

ISED RADIATION EXPOSURE STATEMENT FOR CANADA

This equipment complies with ISED radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with a minimum distance of 15 mm between the radiator and your body.

Cet équipement est conforme aux limites d'exposition aux radiations ISED prévues pour un environnement incontrôlé. Cet équipement doit être installé et utilisé avec un minimum de 15 mm de distance entre la source de rayonnement et votre corps.

LABELING REQUIREMENTS:

The Original Equipment Manufacturer (OEM) must ensure that ISED labeling requirements are met. This includes a clearly visible label on the outside of the OEM enclosure specifying the appropriate Infineon IC identifier for this product as well as the ISED Notices above. The IC identifier is TBD. In any case, the end product must be labeled in its exterior with “Contains IC: TBD“

18.3 European declaration of conformity

Hereby, Infineon declares that the Bluetooth® module CYBLE-3x307x-02 complies with the essential requirements and other relevant provisions of Directive 2014. As a result of the conformity assessment procedure described in Annex III of the Directive 2014, the end-customer equipment should be labeled as follows:

All versions of the CYBLE-3x307x-02 in the specified reference design can be used in the following countries: Austria, Belgium, Cyprus, Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Latvia, Lithuania, Luxembourg, Malta, Poland, Portugal, Slovakia, Slovenia, Spain, Sweden, The Netherlands, the United Kingdom, Switzerland, and Norway.

18.4 MIC Japan

CYBLE-3x307x-02 is certified as a module with certification number 203-JN1038. End products that integrate CYBLE-3x307x-02 do not need additional MIC Japan certification for the end product.

End product can display the certification label of the embedded module.

TBD

Figure 19 MIC label

19 Packaging

Table 24 Solder Reflow peak temperature

Module part number	Package	Maximum peak temperature	Maximum time at peak temperature	No. of cycles
CYBLE-343072-02	43-pad SMT	260 °C	30 seconds	2
CYBLE-333073-02	45-pad SMT	260 °C	30 seconds	2
CYBLE-333074-02	43-pad SMT	260 °C	30 seconds	2

Table 25 Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Module part number	Package	MSL
CYBLE-343072-02	43-pad SMT	MSL 3
CYBLE-333073-02	45-pad SMT	MSL 3
CYBLE-333074-02	43-pad SMT	MSL 3

The CYBLE-3x307x-02 is offered in tape and reel packaging. **Figure 20** details the tape dimensions used for the CYBLE-3x307x-02.

Item	W	A_0	B_0	K_0	K_1	P	F	E	D_0	D_1	P_0	P_2	T
Measurement	$24.0^{+0.30}_{-0.30}$	$22.7^{+0.10}_{-0.10}$	$13.6^{+0.10}_{-0.10}$	$2.3^{+0.10}_{-0.10}$	/ $^{+0.10}_{-0.10}$	$28.0^{+0.10}_{-0.10}$	$11.5^{+0.10}_{-0.10}$	$1.75^{+0.10}_{-0.10}$	$1.50^{+0.10}_{-0.00}$	$1.50^{+0.10}_{-0.10}$	$4.00^{+0.10}_{-0.10}$	$2.00^{+0.10}_{-0.10}$	$0.3^{+0.05}_{-0.05}$

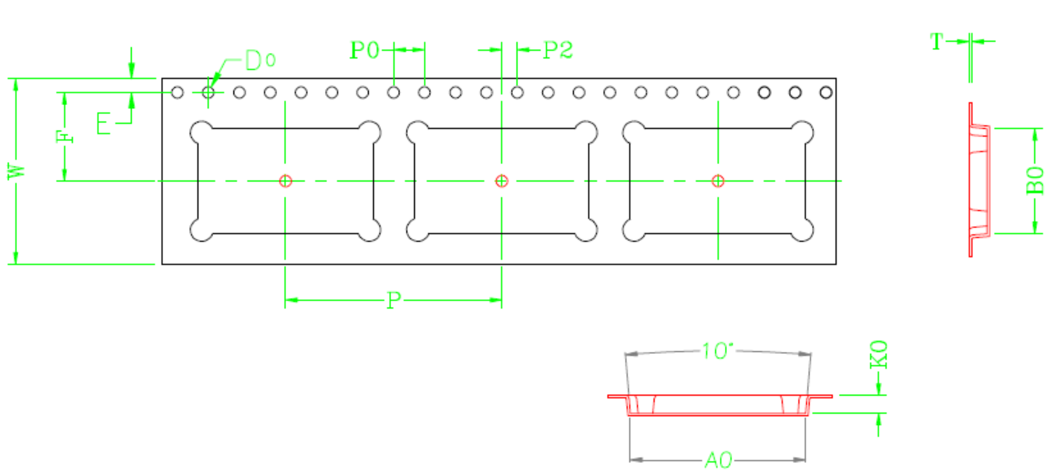


Figure 20 CYBLE-3x307x-02 tape dimensions

Figure 21 details the orientation of the CYBLE-3x307x-02 in the tape as well as the direction for unreeling.

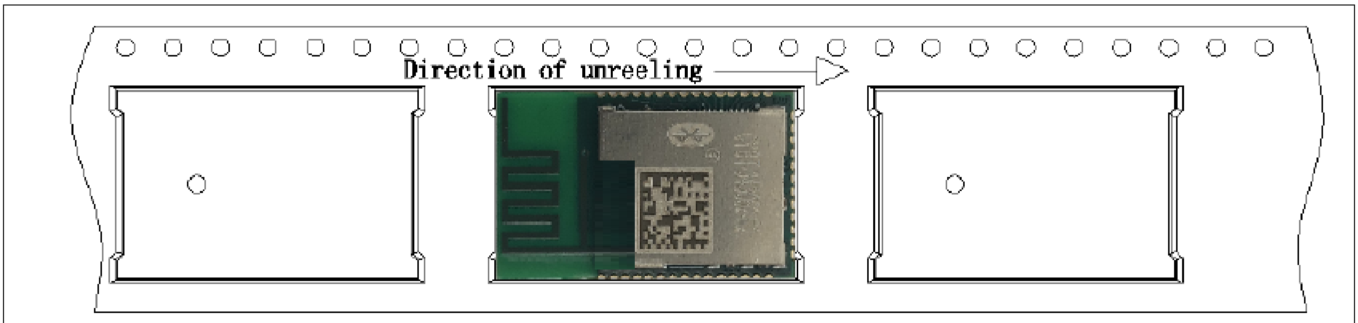
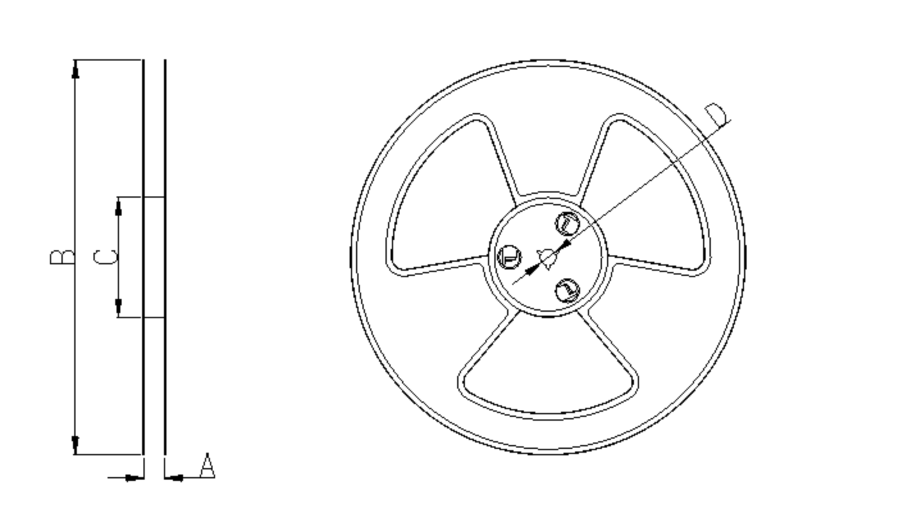


Figure 21 Component orientation in tape and unreeling direction

Figure 22 details reel dimensions used for the CYBLE-3x307x-02.



Index	NOTE	Dimension	Tolerance	
A	Inside Width	24.5	+0.5mm	−0.5mm
B	Reel Diameter	330.00	+1.5mm	−1.5mm
C	Outer Axis Diameter	100.00	+1.5mm	−1.5mm
D	Inner Axis Diameter	13.00	+0.5mm	−0.5mm

Figure 22 Reel dimensions

The CYBLE-3x307x-02 is designed to be used with pick-and-place equipment in an SMT manufacturing environment. The center-of-mass for the CYBLE-3x307x-02 is detailed in **Figure 23**.

TBD

Figure 23 CYBLE-3x307x-02 center of mass

20 Ordering information

Table 26 lists the CYBLE-3x307x-02 part number and features. Table 27 lists the reel shipment quantities for the CYBLE-3x307x-02.

Table 26 Ordering information

Part number	CPU speed (MHz)	Flash size (KB)	RAM size (KB)	UART	I^2C (BSC)	PWM	Antenna	Package	Packaging
CYBLE-343072-02	96	512	384	Yes	Yes	6	Trace	43-SMT	Tape and reel
CYBLE-333073-02	96	512	384	Yes	Yes	6	Pad	45-SMT	Tape and reel
CYBLE-333074-02	96	512	384	Yes	Yes	6	u.FL	43-SMT	Tape and reel

Table 27 Tape and reel package quantity and minimum order amount

Description	Minimum reel quantity	Maximum reel quantity	Comments
Reel quantity	500	500	Ships in 500 unit reel quantities.
Minimum order quantity (MOQ)	500	–	–
Order increment (OI)	500	–	–

The CYBLE-3x307x-02 is offered in tape and reel packaging. The CYBLE-3x307x-02 ships in a reel size of 500.

For additional information and a complete list of Infineon Wireless products, contact your local Infineon sales representative. To locate the nearest Infineon office, visit our website.

U.S. headquarters address	198 Champion Court, San Jose, CA 95134
U.S. headquarter contact info	(408) 943-2600
Website address	**https://www.cypress.com**

21 Acronyms

Table 28 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
ADV	advertising
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
BLE	Bluetooth® Low Energy
Bluetooth® SIG	Bluetooth® Special Interest Group
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CE	European Conformity
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CSA	Canadian Standards Association
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
ESD	electrostatic discharge
FCC	Federal Communications Commission
FET	field-effect transistor
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HCI	host controller interface
HVI	high-voltage interrupt, see also LVI, LVD
I/O	input/output, see also GPIO, DIO, SIO, USBIO
I2C, or IIC	Inter-Integrated Circuit, a communications protocol
IC	integrated circuit
IC	Industry Canada
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
IIR	infinite impulse response, see also FIR

Table 28 Acronyms used in this document *(continued)*

Acronym	Description
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
KC	Korea Certification
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LNA	low noise amplifier
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MIC	Ministry of Internal Affairs and Communications (Japan)
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
Opamp	operational amplifier
PA	power amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset

Table 28 Acronyms used in this document *(continued)*

Acronym	Description
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
QDID	qualification design ID
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
S/H	sample and hold
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I2C serial clock
SDA	I2C serial data
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SMT	surface-mount technology; a method for producing electronic circuitry in which the components are placed directly onto the surface of PCBs
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
STN	super twisted nematic
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TN	twisted nematic
TRM	technical reference manual
TTL	transistor-transistor logic
TUV	Germany: Technischer Überwachungs-Verein (Technical Inspection Association)
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol

Table 28 Acronyms used in this document *(continued)*

Acronym	Description
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

22 Document conventions

22.1 Units of measure

Table 29 Units of measure

Symbol	Unit of Measure
°C	degrees Celsius
dB	decibel
dBm	decibel-milliwatts
fF	femtofarads
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
Khr	kilohour
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Document version	Date of release	Description of changes
**	2021-08-12	Initial release

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Edition 2021-08-12

Published by

Infineon Technologies AG

81726 Munich, Germany

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Document reference

002-33419 Rev. **