DisplayPort1.4a to DP++ Protocol Converter

Features

- DisplayPort® (DP) ver.1.4a compliant receiver
  - Link rate 1.62 / 2.7 / 5.4 / 8.1Gbps
  - 1, 2, or 4 lanes configuration
  - SST, MST up to 6 streams
  - AUX CH 1Mbps
  - HPD_OUT
  - Programmable receiver equalization
  - TPS4 EQ Phase LT support
  - Scrambling of main link data
  - De-spreading of link frequency
  - Video Stream Handling
    - RGB/ YCC 444/422/420 pixel format up to 16 bpc
  - DPCD and CEC
    - DPCD data structure revision 1.4
    - CEC tunneling over AUX
  - Audio stream handling
    - Non-HBR Compressed Formats
      - 2/8 ch layouts
      - Up to 192kHz sample rates
      - Dolby Digital, Digital+, Atmos
    - HBR Audio Formats
      - 8 ch layout
      - Up to 1536kHz sample rates
      - Dolby TrueHD, Atmos, DTS Master
    - LPCM Formats2/8/16/32 Ch
      - Up to 192kHz sample rates
      - 3D LPCM, speaker allocation & mapping
    - One Bit DSD Formats
      - 2/8 ch
      - Single & Double Rate
      - 12288kHz sample rates
    - DST DSD Formats
      - Single/Double rate
      - Up to 22579.2kHz
      - Audio InfoFrame/ ACM/ ISRC/ Audio Metadata DI packets
- DP1.4a / HDMI2.0b (DP++) transmitter
  - DP mode
    - Lane count, Link rate conversion
    - Link rate 1.62 / 2.7 / 5.4 / 8.1Gbps
    - 1, 2, or 4 lanes configuration
    - SST, MST pass through
    - AUX CH 1Mbps
    - HPD_IN
  - HDMI mode
    - AC-coupled HDMI2.0 output
    - 600 MHz maximum TMDS character clock
    - TMDS character-clock divide_by_4 mode
    - HPD_IN (5V Tolerant)
    - DDC CH (5V Tolerant)
    - Conversion to DVI output
  - Scrambler for DP/HDMI output
  - Programmable signal amplitude
  - Programmable pre-emphasis control
  - Pixel format RGB / YCC 444/422/420
  - Deep color up to 16 bits per color
  - 3D video timings
  - CEC 2.0+ with snooping, tunneling
  - SCDC read request handling
  - Metadata handling
- HDMI 2.1 Features
  - Through 6GHz TMDS Mode
  - Supports 4k120Hz,4:2:0, 8bpc with Adaptive Sync to VRR conversion
  - Dynamic HDR Metadata through Extended Metadata Packet
  - Supports VRR, FVA, QMS, QFT, ALLM

Features (continued)

- Video processing
  - Color space conversion from RGB to YCC
  - Colorimetry support: BT2020, BT709, BT601, and Adobe RGB
  - Color bit depth expansion (10 to 12 bits)
  - 16 bits per color pass through
  - DP to HDMI Stereoscopic 3D Transport
    - Frame sequential to stacked top-bottom conversion
    - Pass through of other 3D formats
  - Programmable coefficient 3x3 matrix
    - Programmable input offset
    - Programmable output offset
    - Programmable output clipping levels
  - Video Horizontal blanking expansion
  - Pixel stream de-skewing
  - Adaptive Sync Video
  - Dithering
  - Chroma down sampling
    - 5-tap H & V FIR filters with programmable coefficients
    - 12 bits per color input width
    - 12 bits per color output width
    - YCbCr444 to YCbCr420 conversion
    - YCbCr444 to YCbCr422 conversion
    - YCbCr422 to YCbCr420 conversion
    - Pass through for YCbCr444/422/420
- Max video resolution and color depth on DP output
  - 5K3K60Hz, RGB/YCbCr444, 8 bpc
  - 8K4K60Hz, YCbCr420 up to 8 bpc
  - 4K2K120Hz, RGB/YCbCr444, 8 bpc
- Max video resolution and color depth on HDMI TX output
  - 4K2K60Hz, RGB/YCbCr444, 8 bpc
  - 4K2K60Hz, YCbCr420, up to 16 bpc
  - 4K2K30Hz, RGB/YCbCr444, up to 16 bpc
- HDCP support
  - HDCP1.3 to HDCP1.4 Repeater function
  - DCP compliant: HDCP2.x to HDCP1.4
  - HDCP2.x to HDCP2.x Repeater function
  - Read-protected embedded HDCP keys
- Enhanced security
  - Encrypted on-chip key storage
  - RSA-2048bit signed application firmware
  - Secure boot
  - Secure In-System-Programming
  - Test, debug ports deactivation
- Metadata handling
  - HDMI TX DVI/HDMI mode setting (DPCD register)
  - YCbCr444-420 conversion (DPCD register)
  - IEC60958 BYTE3 channel status overwrite
  - CTA861G INFO FRAME generation
  - CTA861.3 HDR and Mastering InfoFrame
  - Chainable VSC_EXT SDP packing format
- ARM processor and peripheral controllers
  - ARM Cortex M3 core
  - SPI controller
  - I2C master, slave controller
  - On-Chip, RAM, ROM, OTP
- Device configuration options
  - Application FW stored in SPI flash
  - AUX CH, I2C host interface
- Internal video pattern generator
  - Configurable through vendor specific DPCD registers
- EMI reduction support
  - Spread spectrum for DP input, output
  - Scrambler for DP and HDMI outputs
- Low power operation
  - 650mW nominal operation
  - 9.2mW Standby operation
- ESD specification
  - ESD: ±2kV HBM, 250V CDM
- Package
  - TFBGA-169, 7.0mm x 7.0mm x 1.2mm
  - Halogen free Halogen free RoHS and Green Compliant
- Power supply voltages
  - 1.8V I/O, 0.95V core

Description

The MCDP5290 is an advanced DisplayPort1.4a to DP++ dual mode converter targeted primarily for Mobile Notebook accessory and display applications. This device functions as a DP to DP re-timer with lane count, link rate conversion option and DP to HDMI protocol converter with an HDCP1.x/ HDCP2.x repeater function.

The receiver in MCDP5290 supports all DP standard data rates up to HBR3 (8.1Gbps/lane). The dual mode (DP++) transmitter support DP standard data formats up to 8.1Gbps/lane or TMDS data format up to 6.0Gbps/lane. The side-band channel uses 1.0 Mbps Manchester-coded AUX signaling for DP and DDC signaling up to 100 kbps for the HDMI interface.

In the protocol converter mode, MCDP5290 translates a DP SST stream into AC coupled HDMI2.0b output. The highest video timing supported in this mode is 4k2k60Hz RGB/YCC 444 or 4k2k120Hz in YCC 420 pixel format. It supports both RGB 444 and YCC444/422/420 video pixel encoding formats with a color depth up to 16 bpc (bits per component or 48 bits per pixel). The MCDP5290 also has a pixel processing unit capable of video color space conversion from RGB444 to YCC444 with bit depth expansion and pixel encoding format conversion from YCC444 to YCC422/420. It also supports advanced dithering function to truncate the pixel bit depth to the precision of the connected sink device. Pixel format conversion along with horizontal blanking expansion improves interoperability and smooth rendering of video from mobile PC and tablets on legacy TVs. Besides, MCDP52x0 also supports HDMI CEC tunneling over DP AUX channel for remote control pass-through, one touch control of the connected devices in a CE system.

The MCDP5290 processes High Dynamic Range (HDR) video content specified in BT601, BT709, BT2020 or in the Adobe RGB colorimetry format with the appropriate metadata conversion from DP to HDMI standard. It also offers secure reception and transmission of high bandwidth digital audio and video content with HDCP1.x or HDCP2.x content protection. MCDP5290 functions as an HDCP1.x and HDCP2.x repeater between the DP source and DP or HDMI sink.

The MCDP5290 can pass through DP SST or MST uncompressed streams with the flexibility of lane count and link rate conversion. The highest video timing per stream and the number of streams transported is limited by the DP1.4a link bandwidth.

The MCDP5290 uses an external crystal of 25MHz as a reference clock for its operation. It has a 300MHz ARM Cortex M3 CPU with on-chip memories for storing data and code execution. The peripheral subsystem includes SPI, UART (debug only), and I2C master and slave interfaces. An internal Power-On Reset (POR) circuit senses the voltage on the reset input and provides the chip reset during system power-up. The MCDP5290 uses an external 16Mbit SPI flash memory for storing the RSA-2048 signed application firmware with fail-safe recovery. At boot up, the CPU goes through a secure boot process authenticating the application code image stored in the SPI flash. It supports both standard mode and quad mode operation. A firmware update of the SPI flash is done securely through the DP AUX_CH or I2C host interface (Secure In-System-Programming)

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Applications Information

The target applications of MCDP5290 are the notebook, tablet accessories i.e., adapters (dongles), docking stations and other AV accessories.

Application Overview

MCDP5290 is a dual mode converter to support DP++ output. In a protocol converter mode, , it converts DPRX1.4b to the AC coupled HDMI TX 2.0b and during DP to DP conversion, it converts the lane count and link rate to AC coupled DisplayPort1.4 interface with HDCP1.x and 2.x repeater

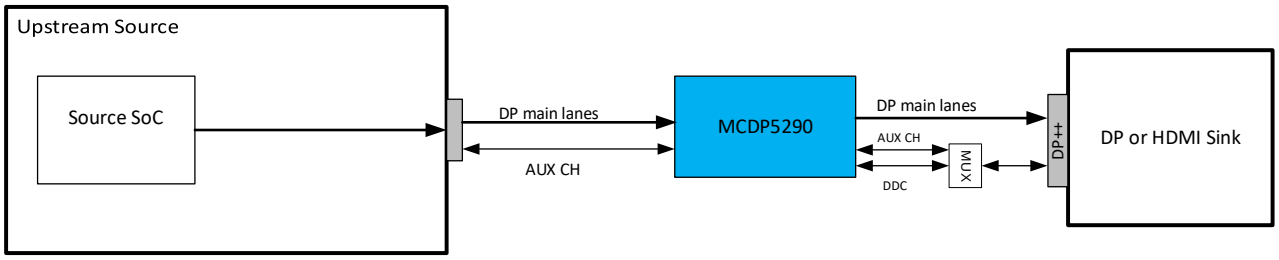
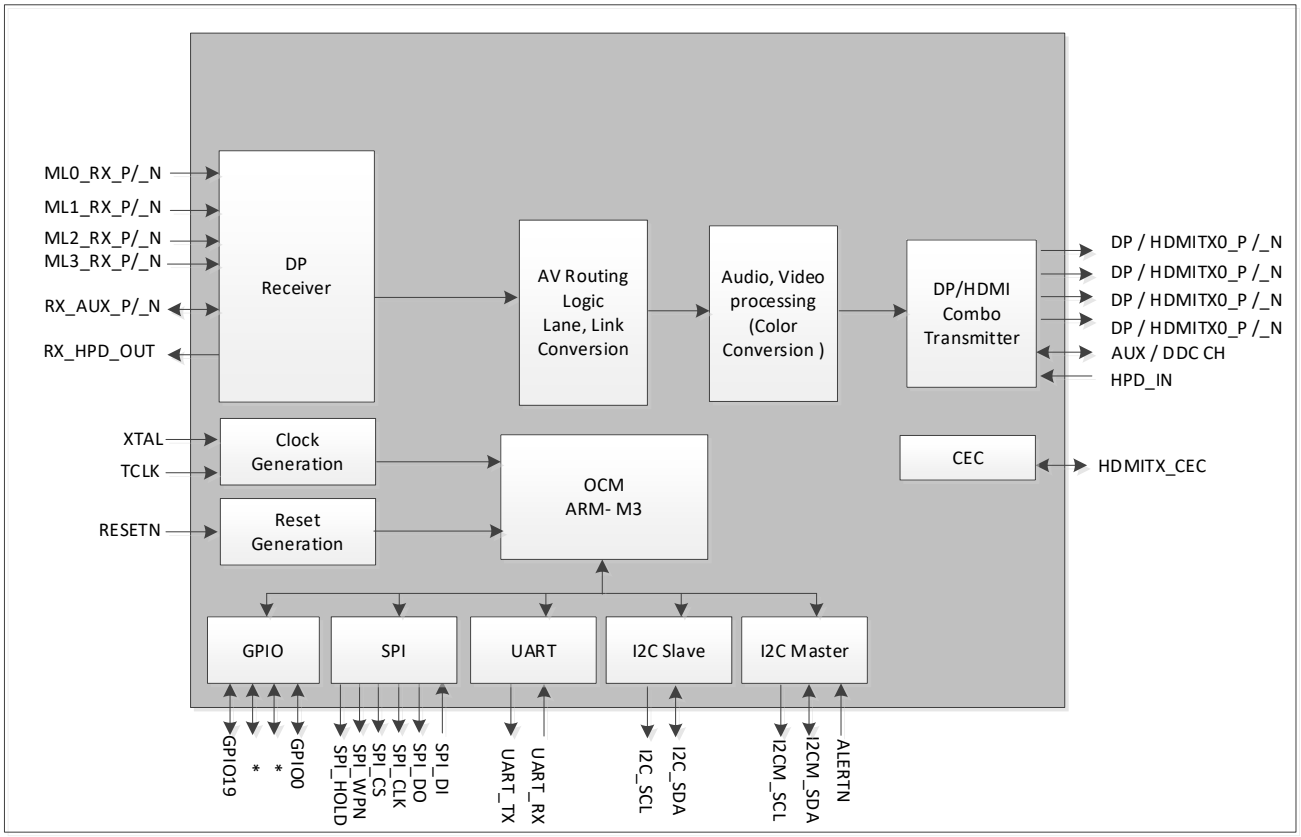


Figure 1. MCDP5290 Adapter Use Case

Functional Block Diagram



Pin Mapping

Table 1. Pin List

Pin #	Name	Pin #	Name	Pin #	Name
A1	GND	D1	GND	G1	I2CM_SDA_PCONF0
A2	UFP_L3N_SSRX2P	D2	AVDDP9_UFP	G2	UFP_HPD_OUT
A3	UFP_L3P_SSRX2N	D3	AVDD18_UFP	G3	NC
A4	GND	D4	AVDD18_UFP	G4	DVDDP9
A5	UFP_L2N_SSTX2P	D5	AVDD18_UFP	G5	GND
A6	UFP_L2P_SSTX2N	D6	GND	G6	GND
A7	RX_REXT	D7	REFCLK_OUT	G7	GND
A8	UFP_L1N_SSTX1N	D8	AVDD18_UFP	G8	GND
A9	UFP_L1P_SSTX1P	D9	AVDD18_UFP	G9	GND
A10	GND	D10	AVDD18_UFP	G10	DVDDP9
A11	UFP_L0N_SSRX1N	D11	DVDD18	G11	TEST
A12	UFP_L0P_SSRX1P	D12	SPI_DI	G12	DFP_CONFIG1
A13	GND	D13	SPI_DO	G13	GPIO7
B1	UFP_AUXP_SBU2	E1	ALERTN_AHPD	H1	I2C_SCL_GPIO1
B2	GND	E2	GND	H2	I2C_SDA_GPIO0
B3	GND	E3	GND	H3	DVDD18
B4	GND	E4	GND	H4	DVDDP9
B5	GND	E5	GND	H5	GND
B6	GND	E6	GND	H6	GND
B7	RESETN	E7	GND	H7	GND
B8	GND	E8	GND	H8	GND
B9	GND	E9	GND	H9	GND
B10	GND	E10	DVDDP9	H10	GND
B11	GND	E11	DVDD18	H11	NC
B12	GND	E12	SPI_WPN	H12	GPIO13
B13	SPI_HOLD	E13	NC	H13	GPIO12
C1	UFP_AUXN_SBU1	F1	I2CM_SCL_PCONF1	J1	DFP_DDC_SDA
C2	GND	F2	GND	J2	GND
C3	AVDDP9_UFP	F3	GND	J3	DVDD18
C4	AVDDP9_UFP	F4	GND	J4	GND
C5	AVDDP9_UFP	F5	GND	J5	GND
C6	XTAL_IN	F6	GND	J6	GND
C7	XTAL_OUT	F7	GND	J7	GND
C8	AVDDP9_UFP	F8	GND	J8	GND
C9	AVDDP9_UFP	F9	GND	J9	GND
C10	AVDDP9_UFP	F10	DVDDP9	J10	DVDDP9
C11	AVDDP9_UFP	F11	GPIO6	J11	NC
C12	SPI_CSN	F12	UTX_GPIO9	J12	GPIO15
C13	SPI_CLK	F13	URX_GPIO8	J13	GPIO14

Continues on page 8

Table 1. Pin List (Continue)

Pin #	Name	Pin #	Name
K1	DFP_DDC_SCL	M1	DFP_L3_HDMICLK_N
K2	CEC_GPIO10	M2	GND
K3	DFP_HPD_IN	M3	GND
K4	AVDD18_DFP	M4	GND
K5	AVDD18_DFP	M5	GND
K6	GND	M6	GND
K7	GND	M7	GND
K8	AVDD18_DFP	M8	GND
K9	AVDD18_DFP	M9	GND
K10	DVDDP9	M10	GND
K11	DVDD18	M11	GND
K12	GPIO17	M12	GND
K13	GPIO16	M13	GND
L1	GND	N1	DFP_L3_HDMICLK_P
L2	DFP_AUX_N	N2	DFP_L2_HDMICH0_N
L3	DFP_AUX_P	N3	DFP_L2_HDMICH0_P
L4	AVDDP9_DFP	N4	DFP_L1_HDMICH1_N
L5	AVDDP9_DFP	N5	DFP_L1_HDMICH1_P
L6	AVDDP9_DFP	N6	DFP_L0_HDMICH2_N
L7	AVDDP9_DFP	N7	DFP_L0_HDMICH2_P
L8	AVDDP9_DFP	N8	DFP_CM
L9	AVDDP9_DFP	N9	DFP_ SSTXP
L10	DVDDP9	N10	DFP_ SSTXN
L11	DVDD18	N11	GND
L12	GPIO19	N12	DFP_ SSRXP
L13	GPIO18	N13	DFP_ SSRXN

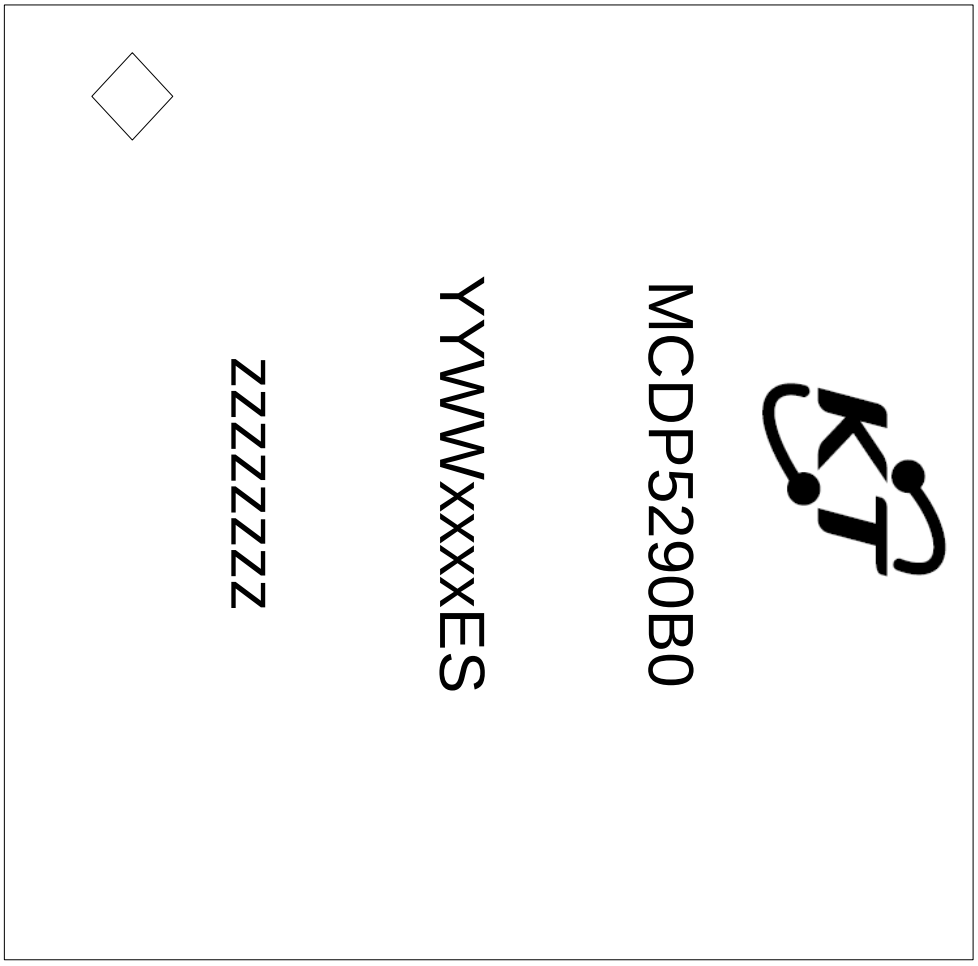
TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	GND	UFP_L3N_SSRX2P	UFP_L3P_SSRX2N	GND	UFP_L2N_SSTX2P	UFP_L2P_SSTX2N	RX_REXT	UFP_L1N_SSTX1N	UFP_L1P_SSTX1P	GND	UFP_L0N_SSRX1N	UFP_L0P_SSRX1P	GND
B	UFP_AUXP_SBU2	GND	GND	GND	GND	GND	RESETN	GND	GND	GND	GND	GND	SPI_HOLD
C	UFP_AUXN_SBU1	GND	AVDDP9_UFP	AVDDP9_UFP	AVDDP9_UFP	XTAL_IN	XTAL_OUT	AVDDP9_UFP	AVDDP9_UFP	AVDDP9_UFP	AVDDP9_UFP	SPI_CSN	SPI_CLK
D	GND	AVDDP9_UFP	AVDD18_UFP	AVDD18_UFP	AVDD18_UFP	GND	REFCLK_OUT	AVDD18_UFP	AVDD18_UFP	AVDD18_UFP	DVDD18	SPI_DI	SPI_DO
E	ALERTN_AHPD	GND	GND	GND	GND	GND	GND	GND	GND	DVDDP9	DVDD18	SPI_WPN	NO CONNECT
F	I2CM_SCL_PCONF1	GND	GND	GND	GND	GND	GND	GND	GND	DVDDP9	DBUG0_GPIO6	UTX_GPIO9	URX_GPIO8
G	I2CM_SDA_PCONF0	UFP_HPD_OUT	NO CONNECT	DVDDP9	GND	GND	GND	GND	GND	DVDDP9	TEST	DFP_CONFIG1	DBUG1_GPIO7
H	I2C_SCL_GPIO1	I2C_SDA_GPIO0	DVDD18	DVDDP9	GND	GND	GND	GND	GND	GND	NO CONNECT	GPIO13	GPIO12
J	DFP_DDC_SDA	GND	DVDD18	GND	GND	GND	GND	GND	GND	DVDDP9	NO CONNECT	GPIO15	GPIO14
K	DFP_DDC_SCL	CEC_GPIO10	DFP_HPD_IN	AVDD18_DFP	AVDD18_DFP	GND	GND	AVDD18_DFP	AVDD18_DFP	DVDDP9	DVDD18	GPIO17	GPIO16
L	GND	DFP_AUX_N	DFP_AUX_P	AVDDP9_DFP	AVDDP9_DFP	AVDDP9_DFP	AVDDP9_DFP	AVDDP9_DFP	AVDDP9_DFP	DVDDP9	DVDD18	GPIO19	GPIO18
M	DFP_L3_HDMICLK_N	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
N	DFP_L3_HDMICLK_P	DFP_L2_HDMICH0_N	DFP_L2_HDMICH0_P	DFP_L1_HDMICH1_N	DFP_L1_HDMICH1_P	DFP_L0_HDMICH2_N	DFP_L0_HDMICH2_P	DFP_CM	DFP_SSTXP	DFP_SSTXN	GND	DFP_SSRXP	DFP_SSRXN

10GHz SERDES	GND	ANALOG	1.8V ANALOG VDD	1.8V DIGITAL I/O	0.95V ANALOG VDD	1.8V DIGITAL VDD	5V TOLERANT OPEN-DRAIN I/O	0.95V DIGITAL VDD	NO CONNECT

169-Pin 7.0mm x 7.0mm x 1.2mm
TFBGA Package, 0.5mm pitch

TOP VIEW



TFBGA-169 7.0mm x 7.0mm x 1.2mm

TOP MARK
KT Logo

MCDP5290B0 = Part Number

YYWWxxxx = Assembly and Date Code ES = Engineering Sample (Blank for production parts)

zzzzzzzz = Special tracking code for ES parts only (Blank for production parts)

Ordering Information

Part Number	Functional Description	Marking[1]	Operating Temperature	Package	External Package
MCDP5290B0	DP1.4 to DP++	YYWWxxxxES	0°C to +70°C	TFBGA-169	TRAYS
MCDP5290B0T					Tape and Reel

Absolute Maximum Ratings[3]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
$V_{DD\_1.8V}$	VDD1.8V to GND	-0.3 to 2.5	V
$V_{DD\_0.95V}$	VDD0.95V to GND	-0.3 to 1.4	V
V_{IO_5V}	VIO5V to GND	-0.3 to 6.0	V
$V_{IO\_1.8V}$	VIO1.8V to GND	-0.3 to 2.5	V
T_S	Storage Temperature Range	-40 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Latch-up Ratings[4]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JESD22-A114 ESD HBM (all pins)	±2.0	kV
V_{ESD_CDM}	JEDEC JESD22-C101 ESD CDM (all pins)	±250	V
I_{LU}	JEDEC JESD78	±100	mA

Thermal Capabilities[5]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	41.7	°C/W
Θ_{JC}	Thermal Resistance – Junction to Case	14.9	°C/W
T_A	Ambient Operating Temperature Range	0 to 70	°C
T_J	Junction Operating Temperature Range	0 to 115	°C

1. "YYWWxxxxES" is the date code, assembly code and lot number. ES – Engineering Sample.

3. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

4. ESD and Latch-up Ratings conform to JEDEC industry standards. Some pins may actually have higher performance. Ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.

5. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to a four-layer JEDEC PCB board, no heat spreader, and no air flow.

Electrical Characteristics[6]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of 0°C to +70°C and $V_{DD\_1.8V}$ = 1.8V, $V_{DD\_0.95V}$ = 0.95V. Typical values are specified at T_A = +25°C.

DC Characteristics

Supply Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DD\_1.8}$	1.8V Supply Operating Range	Analog and digital	1.71	1.8	1.89	V
$V_{DD\_0.95}$	0.95V Supply Operating Range	Analog and digital	0.9	0.95	0.99	V
	Input - 4L DP HBR3, Output – 4L DP HBR3 Video resolution 5k x 3k 60Hz	Protocol converter Mode Measurement conditions: Nominal corner, 25°C, Nominal power supply		661	-	mW
	Input - 2L DP HBR3, Output – HDMI2.0 Video resolution 4k x 2k 60Hz			396	-	mW
	Modern Standby (D1) Core VDD's ON, Clocks OFF			22	-	mW
	Modern Standby (D2) Datapath VDD Off, Clocks OFF			12	-	mW
	Modern Standby (D3) Datapath VDD OFF, Clocks OFF, VDD1 SRAMS OFF			9.2	-	mW

Symbol	Description	Conditions	Minimum Recommended Rating	Typical consumption	Units
$I_{DD\_1.8V}$	1.8V Supply Current[7]	Operating Condition typ Nominal corner, 25°C, Nominal power supply VDD (Analog and Digital) 1.8V VDD (Analog and Digital) 0.95V	188[8]	150	mA
$I_{DD\_0.95V}$	0.95V Supply Current[7]		825[7]	660	mA

IO Signals, 5V Tolerant Open Drain Type

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{PAD}	Input Voltage at PAD			5.0	6.0	V
V_{IH}	Input High voltage		2.0			V
V_{IL}	Input Low voltage				0.8	V
V_{OL}	Output Low voltage				0.3	V
I_{OL}	Output Low current	V_{OL} = 0.4 V	4.0	8.0	11	mA
I_{IL}	Input Leakage current	Input PAD voltage = 5.0V		3.4	13	µA
I_{IL_OFF}	Input Leakage in Fail Safe	VDD/VREF unpowered		3.8	13	µA

6. Device is guaranteed to meet performance specifications over the 0°C to +70°C operating temperature range by design, characterization and correlation with statistical process controls.

7. Ripple amplitude for power supplies should be 20mV or lower with max ripple frequency up to 30MHz.

8. Values are for Power Supply design only and not indicative for Max Power Consumption.

DC Characteristics (continued)

1.8V IO Signals, 1.8V Tolerant, TRISTATE

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input High voltage		1.17			V
V_{IL}	Input Low voltage				0.63	V
V_{OL}	Output Low voltage	I_{OL} = 6mA ~ 24mA			0.45	V
V_{OH}	Output High voltage	I_{OH} = 3mA ~ 12mA	1.35			V
I_{IH}	Input Leakage current		-10		10	µA
I_{IL}			-10		10	µA
I_{OZ}	Tri-state output Leakage current		-10		10	µA
R_{PU}	Pull-up Resistor			80		kΩ
R_{PD}	Pull-down Resistor			95		kΩ

AC Characteristics[9]

Maximum Speed of Operation

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{CLK}	Reference Input Clock				25	MHz
O_{CLK}	On-Chip Microcontroller Clock				300	MHz
$SLAVE\_{SCL}$	I2C host interface clock				400	kHz
$MSTRx\_{SCL}$	DDC Master				400	kHz
SPI	SPI Clock				75	MHz

9. AC characteristics parameters are guaranteed by the silicon characterization across operating condition unless otherwise specified. Not all parameters are tested in the production test.

DisplayPort Receiver Characteristics

Receiver Operating Range

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{RX\_DIF\_PP\_RANGE}$	Differential Input Voltage Range		40		1380	mV
$R_{RX\_TERM\_RANGE}$	RX Termination Control Range		80	100	120	Ω

System Parameters

Symbol	Description	Conditions	Min	Typ	Max	Units
f_{HBR3}	High bit rate 3 frequency	Frequency high limit = +300ppm Frequency low limit = -5300ppm		8.1		Gbps
f_{HBR2}	High bit rate 2 frequency			5.4		Gbps
f_{HBR}	High bit rate frequency			2.7		Gbps
F_{RBR}	Low bit rate frequency			1.6		Gbps
SSC_{DPRX_FREQ}	Link clock down-spreading frequency		30		33	kHz
SSC_{DPRX_AMP}	Link clock down spreading		0		0.5	%

TP3 Parameters

Symbol	Description	Conditions	Min	Typ	Max	Units
$T_{RBR\_EYE\_TP3}$	Receiver Eye TP3 RBR	Measured at 10-9 BER	0.25			UI
$T_{HBR\_EYE\_TP3EQ}$	Receiver Eye TP3_EQ HBR		0.509			UI
$T_{HBR2\_EYE\_TP3EQ}$	Receiver Eye TP3_EQ HBR2		0.38			UI
$T_{HBR3\_EYE\_TP3CTLE}$	Receiver Eye TP3_CTLE HBR3	Measured at 10-6BER	0.38			UI
Target bit error rate 10^{-9}						
$T_{RX\_Non-ISI\_RBR}$	Non-ISI at 1.62 Gbps	1.62Gbps signal @ TP3			0.180	UI
$T_{RX\_TJ\_RBR}$	TJ at 1.62 Gbps	1.62Gbps signal @ TP3			0.750	UI
$T_{RX\_Non-ISI\_HBR}$	Non-ISI at 2.7 Gbps	2.7Gbps signal @ TP3_EQ			0.330	UI
$T_{RX\_TJ\_HBR}$	TJ at 2.7 Gbps	2.7Gbps signal @ TP3_EQ			0.491	UI
$T_{RX\_DJ\_HBR2}$	DJ at 5.4 Gbps	5.4Gbps signal @ TP3_EQ			0.49	UI
$T_{RX\_TJ\_HBR2}$	TJ at 5.4 Gbps	5.4Gbps signal @ TP3_EQ			0.62	UI
Target bit error rate 10^{-6}						
$T_{RX\_NON\_ISI\_HBR3}$	Non-ISI at 8.1 Gbps	8.1Gbps signal @ TP3_CTLE			0.38	UI
$T_{RX\_TJ\_HBR3}$	TJ at 8.1 Gbps	8.1Gbps signal @ TP3_CTLE			0.62	UI

DisplayPort Transmitter Characteristics

Transmitter Operating Range

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{TX\_DIF\_PP\_RANGE}$	Differential Output Voltage Range		340		1380	mV
$R_{TX\_TERM\_RANGE}$	TX Termination Control Range		80	100	120	Ω

System Parameters

Symbol	Description	Conditions	Min	Typ	Max	Units
f_{HBR3}	High bit rate 3 frequency	Frequency high limit = +300ppm Frequency low limit = -5300ppm		8.1		Gbps
f_{HBR2}	High bit rate 2 frequency			5.4		Gbps
f_{HBR}	High bit rate frequency			2.7		Gbps
F_{RBR}	Low bit rate frequency			1.6		Gbps
SSC_{DPTX_FREQ}	Link clock down-spreading frequency		30		33	kHz
SSC_{DPTX_AMP}	Link clock down spreading		0		0.5	%
C_{TX}	Coupling capacitor	All Main lanes and AUX CH need AC coupling on the transmitter side		100		nF

DisplayPort Transmitter Characteristics (Continued)

HBR3/HBR2 Transmitter TP2 Parameters

Symbol	Description	Conditions	Min	Typ	Max	Units
$R_{VSL\_1\_0\_HBR3\_2}$	Ratio of Voltage Swing (VSL[1]/VSL[0])	Calculated using measured value of 1st harmonic of FFT at TX_EOL[0]	1.6		4.5	dB
$R_{VSL\_2\_0\_HBR3\_2}$	Ratio of Voltage Swing (VSL[2]/VSL[0])		3.2		7.0	dB
$R_{VSL\_3\_0\_HBR3\_2}$	Ratio of Voltage Swing (VSL[3]/VSL[0])		4.8		10.5	dB
$R_{VSL\_2\_1\_HBR3\_2}$	Ratio of Voltage Swing (VSL[2]/VSL[1])		1.1			dB
$R_{VSL\_3\_2\_HBR3\_2}$	Ratio of Voltage Swing (VSL[3]/VSL[2])		1.1			dB
$\Delta_{EQL\_1\_0\_HBR3\_2}$	Delta of TX Pre-emphasis TX_EQL[1]/TX_EQL[0]	Calculated using measured value of 1st and 5th harmonics of FFT	1.3		4.0	dB
$\Delta_{EQL\_2\_0\_HBR3\_2}$	Delta of TX Pre-emphasis TX_EQL[2]/TX_EQL[0]		2.4		6.0	dB
$\Delta_{EQL\_3\_0\_HBR3\_2}$	Delta of TX Pre-emphasis TX_EQL[3]/TX_EQL[0]		3.5		8.0	dB
$\Delta_{EQL\_2\_1\_HBR3\_2}$	Delta of TX Pre-emphasis TX_EQL[2]/TX_EQL[1]		0.7			dB
$\Delta_{EQL\_3\_2\_HBR3\_2}$	Delta of TX Pre-emphasis TX_EQL[3]/TX_EQL[2]		0.7			dB

HBR/HBR Transmitter TP2 Parameters

Symbol	Description	Conditions	Min	Typ	Max	Units
$R_{VSL\_1\_0\_HBR\_RBR}$	Ratio of Output Voltage Level 1/Level 0	Measured on non-transition bits at Pre-emphasis Level 0 setting.	0.8		6.0	dB
$R_{VSL\_2\_1\_HBR\_RBR}$	Ratio of Output Voltage Level 2/Level 1		0.1		5.1	dB
$R_{VSL\_3\_2\_HBR\_RBR}$	Ratio of Output Voltage Level 3/Level 2		0.8		6.0	dB
$R_{EQ\_DISABLE}$	Maximum Pre-emphasis when disabled				0.25	dB
$\Delta_{EQL\_1\_0\_HBR\_RBR}$	Delta of Pre-emphasis Level 1 vs. Level 0		2			dB
$\Delta_{EQL\_2\_1\_HBR\_RBR}$	Delta of Pre-emphasis Level 2 vs. Level 1		1.6			dB
$\Delta_{EQL\_3\_2\_HBR\_RBR}$	Delta of Pre-emphasis Level 3 vs. Level 2		1.6			dB

DisplayPort Transmitter Characteristics (Continued)

DisplayPort Transmitter TP3 Parameters

Symbol	Description	Conditions	Min	Typ	Max	Units
$T_{TX\_SKEW\_INTER\_PAIR}$	Lane-to-Lane output Skew	Applies to all pairwise combinations of supported lanes			1250	ps
$T_{TX\_SKEW\_INRA\_PAIR}$	Lane Intra pair Skew	Applies to all supported lanes			30	ps
Target bit error rate 10^{-6}						
$T_{TX\_TJ\_TPS4\_HBR3}$	TJ at 8.1Gbps	8.1Gbps signal @ TP3_CTLE (CTS condition)			0.47	UI
$T_{TX\_NonISI\_TPS4\_HBR3}$	Non-ISI at 8.1Gbps	8.1Gbps signal @ TP3_CTLE (CTS condition)			0.23	UI
Target bit error rate 10^{-9}						
$T_{TX\_TJ\_CP2520\_HBR2}$	TJ CP2520 at 5.4Gbps	5.4Gbps signal @ TP3_EQ			0.62	UI
$T_{TX\_DJ\_CP2520\_HBR2}$	DJ CP2520 at 5.4Gbps	5.4Gbps signal @ TP3_EQ			0.49	UI
$T_{TX\_TJ\_D10.2\_HBR2}$	TJ D10.2 at 5.4Gbps	5.4Gbps signal @ TP3_EQ			0.40	UI
$T_{TX\_DJ\_D10.2\_HBR2}$	DJ D10.2 at 5.4Gbps	5.4Gbps signal @ TP3_EQ			0.27	UI
$T_{TX\_RJ\_D10.2\_HBR2}$	RJ D10.2 at 5.4Gbps	5.4Gbps signal @ TP3_EQ			0.23	UI

DisplayPort AUX_CH Characteristics

DisplayPort AUX_CH

Symbol	Description	Conditions	Min	Typ	Max	Units
UI_{AUX_MAN}	Manchester transaction unit interval		0.4		0.6	µs
$N_{PRE\_CHARGE\_PULSE}$	Number of pre-charge pulses		10		16	
$T_{AUX\_BUS\_PARK}$	AUX CH bus park time		10			ns
$V_{AUX\_DIFFp\text{-}p\_TX}$	AUX peak-to-peak voltage at transmitter		0.29	0.40	1.38	V
$V_{AUX\_DIFFp\_p\_RX}$	AUX peak-to-peak voltage at receiver		0.27		1.36	V
R_{AUX_TERM}	AUX CH termination			100		Ω
$V_{AUX\_TURN\_CM}$	AUX_DC common mode voltage		0		3.6	V
$V_{AUX\_TURN\_CM}$	AUX turn-around common mode voltage				0.3	V
C_{AUX}	AC coupling capacitor		75		200	nF

HDMI Transmitter I/O Characteristics

HDMI Transmitter DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{TX_PP}	Differential output: single ended swing amplitude		0.4	0.5	0.6	V
For < 3.4Gbps						
$V_{TX\_DIF\_HIGH}$	Differential output: Single ended high-level output	Sink supply dependent (typical V_{DD} in OFF state = 3.3V)		3.15		V
For > 3.4Gbps						
$V_{TX\_DIF\_HIGH}$	Differential output: Single ended high-level output	Sink supply dependent (typical V_{DD} in OFF state = 3.3V)		3.05		V

HDMI Transmitter AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$f_{TX\_CHR\_CLK}$	TMDS Character Clock	Programmable	25		600	MHz
$V_{TX\_DIF\_PP}$	Differential Output Voltage	In 64 steps (usable range 0.8 – 1.2 V)	0		1.2	V
t_{TX_ER}	TX Edge Rate	1 V $V_{TX\_DIF\_PP}$ and Pre-emphasis at 0dB (Max = 145)	75		TBD	pS
A_{PREMPH}	TX Pre-Emphasis Level	$V_{TX\_DIF\_PP}$ + A_{PREMPH} should be less than 1.2 V	0		6	dB
$R_{TX\_TERM\_RANGE}$	TX Differential Termination Control Range > 3.4Gbps	Programmable Termination (range 85-600)	80	100	600	Ω
$T_{TX\_CLK\_JITTER}$	TX Clock jitter	Tighter than HDMI specification			0.25	TBIT
	TX Data Jitter	Refer to the tables below.				

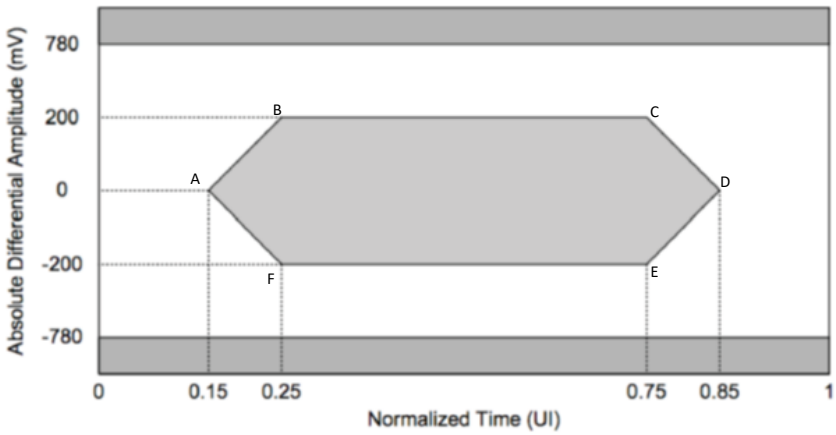


Figure 2. HDMI1.4b EYE Diagram at TP1 at TMDS Character Clock Rate ≤ 340MHz

Table 2. TMDS TX EYE Opening Specification for TMDS Character Clock Rate ≤ 340MHz

Point	H(UI)	V (mV_diff_pp)
A	0.13	0
B	0.20	200
C	0.80	200
D	0.87	0
E	0.80	-200
F	0.20	-200

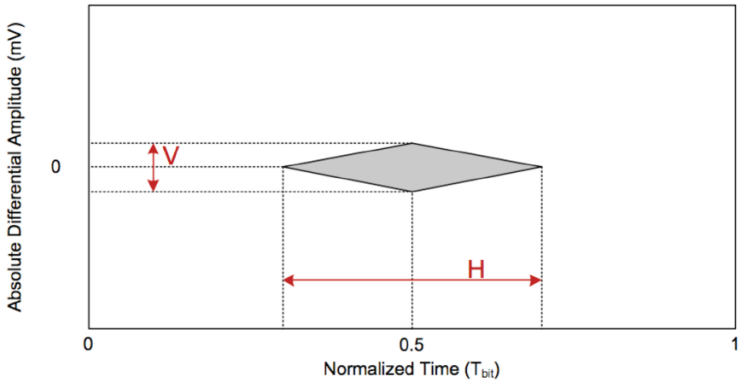


Figure 3. HDMI2.0 EYE Diagram at TP2_EQ at TMDS Character Clock Rate > 340MHz

Table 3. TMDS TX PHY Jitter Specification at TMDS Character Clock Rate > 340 MHz

TMDS Bit Rate (Gbps)	H (Tbit)	V (mV_diff_pp)
3.4 < Rbit < 3.712	0.72	335
3.712 < Rbit <= 5.94	-0.0332 $Rbit^2$ + 0.2312 Rbit + 0.1998	-19.66 $Rbit^2$ + 106.74 Rbit + 209.58
5.94 < Rbit <= 6.0	0.48	150

DDC (I2C) Interface Timing Characteristics

DDC (I2C) Interface Timing

Symbol	Description	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL clock rate	Fast mode	0	-	400	kHz
t_{HD-STA}	Hold time START	After this period, the 1st clock starts	1.2	-	-	µs
t_{LOW}	Low period of clock	SCL	1.3	-	-	µs
t_{HIGH}	High period of clock	SCL	1.2	-	-	µs
$T_{su;STA}$	Set up time for a repeated START		1.2	-	-	µs
$t_{HD;DAT}$	Data hold time	For master	0.7	-	0.9[10]	µs
$t_{SU;DAT}$	Data setup time		380	-	-	ns
T_{BUF}	Bus free time between STOP and START		1.3	-	-	µs
C_B	Capacitance load for each bus line		-	100	400	pF
t_r	Rise time		220	-	300	ns
t_f	Fall time		60	-	300	ns
V_{nh}	Noise margin at high level		0.25 VDD	-	-	V
V_{nl}	Noise margin at low level		0.2 VDD	-	-	V

10. The maximum tHD;DAT only has to be met if the device does not stretch the low period tLOW of the SCL signal. In the diagram below, S = start, P = stop, Sr = Repeated start, and SP= Repeated stop conditions.

I2C Host Interface Timing (Figure 6)

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCL}	SCL Clock Frequency				400	kHz
$t_{hd: DAT}$	Data hold time		0		-	µs
$t_{SU :DAT}$	Data set-up time		50		-	ns
t_R	Rise time of both SDA and SCL signals		-		120	ns
t_F	Fall time of both SDA and SCL signals		20x (V_{DD}/ 5.5)		120	ns
t_{BUF}	Bus free time between a STOP and START condition		0.5		-	µs
C_B	Capacitance load for each bus line		-		550	pF
$t_{VD: DAT}$	Data valid time		-		0.45	µs
$t_{VD: ACK}$	Data valid acknowledge time		-		0.45	µs
t_{I2C_SBR} (400 kHz)	Time for I2C SINGLE BYTE READ		-		110	µs
t_{I2C_SBW} (400 kHz)	Time for I2C SINGLE BYTE WRITE		-		85	µs
t_{I2C_MBR} (400 kHz)	Time for I2C Multi BYTE READ		-		100+35/byte	µs
t_{I2C_MBW} (400 kHz)	Time for I2C Multi BYTE WRITE				85+30/ byte	µs

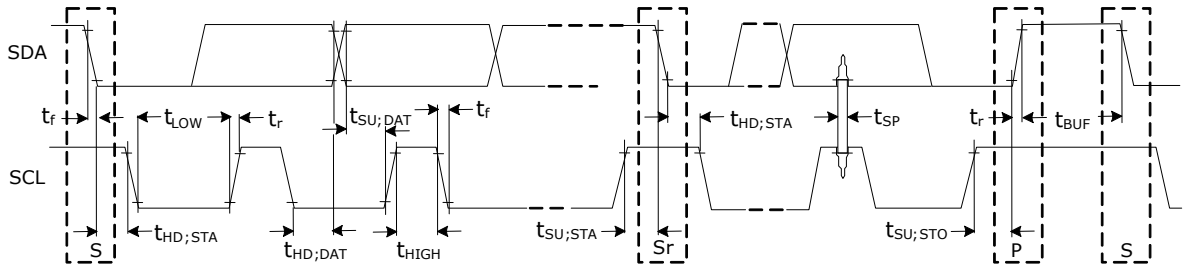


Figure 4. I2C Timing

SPI Interface Timing Characteristics

SPI Interface Timing for Normal Operating Mode[11]

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{CLK}	SPI_CLK output clock frequency for normal SPI mode			50	75	MHz
T_{SCKH}	Serial clock high time		9.2			ns
T_{SCKL}	Serial clock low time		9.2			ns
$T_{R\_SPI\_CLK}$	SPI_CLK rise time @10mA drive 10pF load				2.8	ns
$T_{F\_SPI\_CLK}$	SPI_CLK fall time @10mA drive 10pF load				3.2	ns
T_{CSN_SU}	CSN output setup time requirement		7			ns
T_{CSN_HLD}	CSN output hold time requirement		7			ns
$T_{\_DO\_PD}$	Data Output propagation delay				6	ns
T_{DI_SU}	Data Input setup time		3			ns
T_{DI_HLD}	Data Input hold time		5			ns

11. These specifications specify the typical SPI_CLK output frequency and the minimum requirements of the interface between the SPI NOR Flash device and MCDP52x0.

Power Supply

MCDP5290 supports 1.8V and 0.95V supplies.

Note: There is no relationship between 1.8V ramp-up timing and 0.95V ramp-up timing. Each Power Supply Ramp up time is between 200µs to 4ms.

Chip Power-up Sequence and Reset

The Power-On Reset circuit is shown below

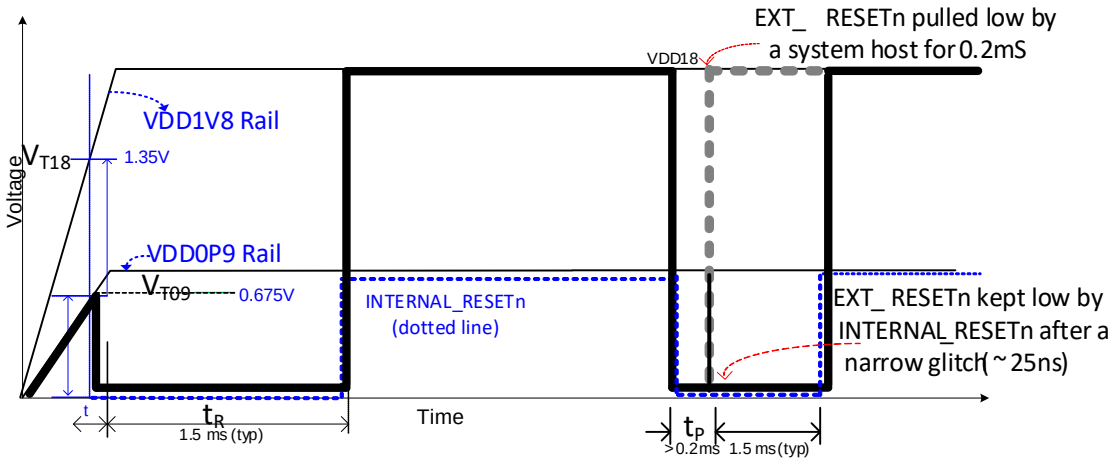


Figure 5. Power-On Reset Requirements

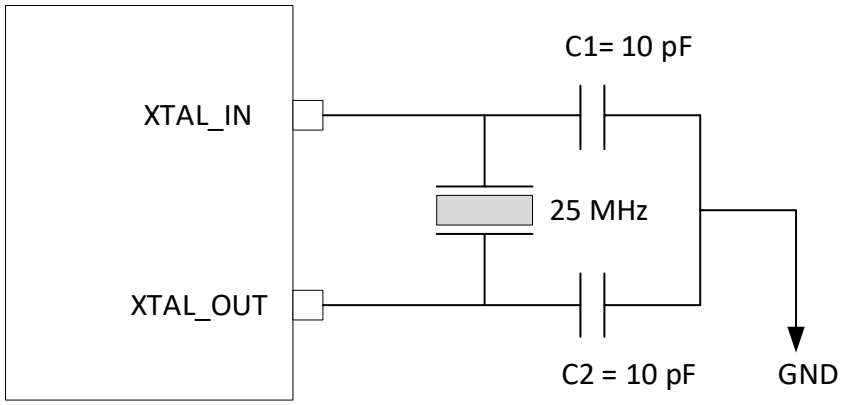
The timing diagram above shows the expected behavior of the POR circuit.

Clock Generation

MCDP5290 requires an external clock signal of 25MHz for its operation. This is the reference clock for all internal clock generation. The reference clock signal can be from an external source (oscillator) to the XTAL_IN input pin or generated by the internal oscillator using a reference 25MHz crystal connected across XTAL_IN and XTAL_OUT pins. The selection between external clock input and the internal oscillator is decided through bootstrap selection pin. Refer to bootstrap configuration selection in following section. The REFCLK_OUT pin provides the internally generated reference clock signal to be used for driving 2nd MCDP5290 or another device in the same system. The REFCLK_OUT is enabled or disabled through bootstrap selection pin.

Internal Oscillator Operation

A crystal resonator is connected between the XTAL_IN and XTAL_OUT pins with the appropriate capacitors (C1 and C2) to match the proper value of loading capacitance specified in crystal specification. A 25MHz crystal oscillation is necessary to meet the reference clock frequency requirement of MCDP5290.



Note: The value of C1 and C2 are determined based on the loading capacitance from the crystal specification and by compensating for the parasitic capacitance of the device and the printed circuit board traces. The external capacitors are terminated to GND. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to VDD.

Figure 6. Internal Oscillator with External Crystal

Crystal Specifications

While the selection of a crystal mainly depends on the specific PCB layout and the crystal manufacturer's specifications, the following are general recommendations.

Table 4. Crystal Specifications

Parameters	Specifications
Frequency	25.000MHz
Operation Mode	Fundamental
Operating Temperature	-10ºC to +70ºC
Frequency Tolerance @ 25ºC	±50ppm max
Equivalent series resistance	≤ 60Ω

Note these details of the oscillator circuit design when using a crystal resonator:

- The PCB traces should be as short as possible.
- The crystal should be a parallel resonate-cut

Functional Description

Connections

Pin List[12]

I/O Legend: I = Input; O = Output; P = Power; G = Ground; I/O = Bi-directional; AI = Analog Input

Table 5. UFP Combo Receiver/Transmitter Pins

Pin	Assignment	I/O	VDD Domain	Description
A2	UFP_L3N_SSRX2P	I	0.95V	UFP combo RX/TX input. Connect to DP main lane 3 negative pin of DP connector or RX2 positive pin of USB-C connector. Use AC-coupling capacitor.
A3	UFP_L3P_SSRX2N	I	0.95V	UFP combo RX/TX input. Connect to DP main lane 3 positive pin of DP connector or RX2 negative pin of USB-C connector. Use AC-coupling capacitor.
A5	UFP_L2N_SSTX2P	IO	0.95V	UFP combo RX/TX input/output. Connect to DP main lane 2 negative pin of DP connector or TX2 positive pin of USB-C connector. Use AC-coupling capacitor.
A6	UFP_L2P_SSTX2N	IO	0.95V	UFP combo RX/TX input/output. Connect to DP main lane 2 positive pin of DP connector or TX2 negative pin of USB-C connector. Use AC-coupling capacitor.
A8	UFP_L1N_SSTX1N	IO	0.95V	UFP combo RX/TX input/output. Connect to DP main lane 1 negative pin of DP connector or TX1 negative pin of USB-C connector. Use AC-coupling capacitor.
A9	UFP_L1P_SSTX1P	IO	0.95V	UFP combo RX/TX input/output. Connect to DP main lane 1 positive pin of DP connector or TX1 positive pin of USB-C connector. Use AC-coupling capacitor.
A11	UFP_L0N_SSRX1N	I	0.95V	UFP combo RX/TX input. Connect to DP main lane 0 negative pin of DP connector or RX1 negative pin of USB-C connector. Use AC-coupling capacitor.
A12	UFP_L0P_SSRX1P	I	0.95V	UFP combo RX/TX input. Connect to DP main lane 0 positive pin of DP connector or RX1 positive pin of USB-C connector. Use AC-coupling capacitor.
B1	UFP_AUXP_SBU2	IO	1.8V	Connect to Side Band Use signal 2 pin of PD controller or connect to auxiliary channel positive pin of DP connector. Use AC-coupling capacitor.
C1	UFP_AUXN_SBU1	IO	1.8V	Connect to Side Band Use signal 1 pin of PD controller or connect to auxiliary channel negative pin of DP connector. Use AC-coupling capacitor.
G2	UFP_HPD_OUT	O	1.8V, Internal PD	UFP HPD signal pin (to DP source), to be externally pulled down (100kΩ).
A7	RX_REXT	I	1.8V	Termination calibration reference resistor; 5.36kΩ ±1% resistor must be connected from this pin to GND

Table 6. DFP USB Receiver/Transmitter Pins

Pin	Assignment	I/O	VDD Domain	Description
N13	DFP_SSRXN	I	0.95V	NC
N12	DFP_SSRXP	I	0.95V	NC
N10	DFP_SSTXN	O	0.95V	NC
N9	DFP_SSTXP	O	0.95V	NC

12. Some pins can have multiple functionalities, which are configured under register control. The alternate functionality for each pin is listed in the description column

Table 7. DFP DP++ Transmitter Pins[13]

Pin	Assignment	I/O	VDD Domain	Description
M1	DFP_L3_HDMICLK_N	IO	DFP_CM	DFP TX port pin. DP transmitter main lane 3 negative output or HDMI transmitter CLOCK negative output.
N1	DFP_L3_HDMICLK_P	IO	DFP_CM	DFP TX port pin. DP transmitter main lane 3 positive output or HDMI transmitter CLOCK positive output.
N2	DFP_L2_HDMICH0_N	IO	DFP_CM	DFP TX port pin. DP transmitter main lane 2 negative output or HDMI transmitter data CH0 negative output.
N3	DFP_L2_HDMICH0_P	IO	DFP_CM	DFP TX port pin. DP transmitter main lane 2 positive output or HDMI transmitter data CH0 positive output.
N4	DFP_L1_HDMICH1_N	IO	DFP_CM	DFP TX port pin. DP transmitter main lane 1 negative output or HDMI transmitter data CH1 negative output.
N5	DFP_L1_HDMICH1_P	IO	DFP_CM	DFP TX port pin. DP transmitter main lane 1 positive output or HDMI transmitter data CH1 positive output.
N6	DFP_L0_HDMICH2_N	IO	DFP_CM	DFP TX port pin. DP transmitter main lane 0 negative output or HDMI transmitter data CH2 negative output.
N7	DFP_L0_HDMICH2_P	IO	DFP_CM	DFP TX port pin. DP transmitter main lane 0 positive output or HDMI transmitter data CH2 positive output.
L2	DFP_AUX_N	IO	1.8V	DFP TX port pin. DP transmitter Auxiliary CH negative output. Use AC-coupling capacitor.
L3	DFP_AUX_P	IO	1.8V	DFP TX port pin. DP transmitter Auxiliary CH positive output. Use AC-coupling capacitor.
K1	DFP_DDC_SCL	O	Open Drain, 5V TOL	HDMI TX DDC I2C master SCL. 5 V tolerant open drain output, External pullup to DDC5V via a 1.5kΩ ~ 2.2kΩ resistor.
J1	DFP_DDC_SDA	IO	Open Drain, 5V TOL	HDMI TX DDC I2C master SDA. 5 V tolerant open drain IO, External pullup to DDC5V via a 1.5kΩ ~ 2.2kΩ resistor.
K2	CEC_GPIO10	IO	Open Drain, 5V TOL	HDMI TX CEC input. 5V tolerant open drain IO. Connect to HDMI connector CEC pin. External pullup to 3.3V via 27kΩ resistor as per HDMI1.4b specification. Use external 27kΩ pull up when CEC is not used.
K3	DFP_HPD_IN	I	Open Drain, 5V TOL	HDMI TX HPD input 5V tolerant open drain IO. Connect to HDMI connector HPD pin. Use external pull down via 47kΩ resistor.
G12	DFP_CONFIG1	I	Open Drain, 5V TOL	1M ohm pulled down to GND

Table 8. System Interface Pins

Pin	Assignment	I/O	VDD Domain	Reset State	Description
B7	RESETN	IO	1.8V	Input	Power-ON chip reset (active low) input signal. Can be driven low by an external reset signal. Use external pullup to 1.8V power rail via 2.2kΩ ±10% resistor.
D7	REFCLK_OUT	O	0.95V	Output	Reference clock output (25MHz). Can be used as clock source for external devices on the system.
C6	XTAL_IN	IO	1.8V	Input / Output	Crystal node. Connect to 25MHz crystal- refer to schematics. When the oscillator clock is used as reference, connect to the clock signal.[14]
C7	XTAL_OUT	IO	1.8V	Input / Output	Crystal node. Connect to 25MHz crystal - refer to schematics. When the oscillator clock is used as reference, this pin is NC. [14]
N8	DFP_CM	IO	1.8V or Open	Input / Output	TX port determination power pin. For DP and DP++ mode this pin must be connected to 1.8 V with proper capacitor filtering to GND. For HDMI mode, only capacitor filtering to GND needed.

13. The HDMI TX output is terminated at the receiver through a 50Ω resistor

14. Load capacitance may vary based on the PCB design and crystal spec.

Pin	Assignment	I/O	VDD Domain	Reset State	Description
H1	I2C_SCL_GPIO1	IO	Open Drain, 5V TOL	Input, internal PU	Host (slave) I2C interface clock line 5V tolerant open drain IO, Use external pullup to 3.3V or 5V supply.
H2	I2C_SDA_GPIO0	IO	Open Drain, 5V TOL	Input, Internal PU	Host (slave) I2C interface data line. 5V tolerant open drain IO, Use external pullup to 3.3V or 5V supply.
C12	SPI_CSN	O	1.8V	Output, Internal PU	Serial peripheral interface chip select. Programmable Slew Rate and Drive Strength.
D12	SPI_DI	IO	1.8V	Input, Internal PD	Serial peripheral interface data input. Use as DQ1 input/output during quad mode operation.
D13	SPI_DO	IO	1.8V	Output, Internal PU	Serial peripheral interface data output. Use as DQ0 input/output during quad mode operation.
C13	SPI_CLK	IO	1.8V	Output, Internal PD	Serial peripheral interface clock.
E12	SPI_WPN	IO	1.8V	Input, Internal PU	Serial peripheral interface write-protect. Use as DQ2 input/output during quad mode operation.
B13	SPI_HOLD	IO	1.8V	Input, Internal PU	Serial peripheral interface hold signal. Use as DQ3 input/output during quad mode operation.
F13	URX_GPIO8	I	1.8V	Input, Internal PU	Universal asynchronous serial RX input. Internal PU. Can be used as GPIO. Programmable Slew Rate and Drive Strength.[15]
F12	UTX_GPIO9	O	1.8V	Output, Internal PU	Universal asynchronous serial TX output. Can be used as GPIO. Programmable Slew Rate and Drive Strength.
G1	I2CM_SDA_PCONF0	IO	Open Drain, 5V TOL	Input Internal PU	I2C Master interface data line. 5V tolerant open drain IO, Use external pullup to 3.3V or 5V supply.
F1	I2CM_SCL_PCONF1	IO	Open Drain, 5V TOL	Input Internal PU	I2C Master interface clock line. 5V tolerant open drain IO, Use external pullup to 3.3V or 5V supply.
E1	ALERTN_AHPD	IO	Open Drain, 5V TOL	Input Internal PU	Interrupt (Alert) input or USB Type-C plug orientation configuration pin. 5V tolerant open drain IO. Connect to TCPC/PD Interrupt out pin. Use external pull down via 5.1kΩ resistor Low: normal operation, High: flipped operation
F11	GPIO6	IO	1.8V	Input Internal PU	General Purpose IO. Programmable Slew Rate and Drive Strength.
G13	GPIO7	IO	1.8V	Input Internal PU	General Purpose IO. Programmable Slew Rate and Drive Strength.
H13	GPIO12	IO	1.8V	Input Internal PD	General Purpose IO. Programmable Slew Rate and Drive Strength.
H12	GPIO13	IO	1.8V	Input Internal PD	General Purpose IO. Programmable Slew Rate and Drive Strength.
J13	GPIO14	IO	1.8V	Input Internal PD	General Purpose IO. Programmable Slew Rate and Drive Strength.

15. UART RX function is disabled in production version

Pin	Assignment	I/O	VDD Domain	Reset State	Description
J12	GPIO15	IO	1.8V	Input Internal PD	General Purpose IO. Programmable Slew Rate and Drive Strength.
K13	GPIO16	IO	1.8V	Input Internal PU	General Purpose IO. Programmable Slew Rate and Drive Strength.
K12	GPIO17	IO	1.8V	Input Internal PU	General Purpose IO. Programmable Slew Rate and Drive Strength.
L13	GPIO18	IO	1.8V	Input Internal PU	General Purpose IO. Programmable Slew Rate and Drive Strength.
L12	GPIO19	IO	1.8V	Input Internal PD	General Purpose IO. Programmable Slew Rate and Drive Strength.
G11	TEST	IO	1.8V	Input	Test purpose. Connect to GND

Table 9. Power and Ground Pins

Pin	Assignment	Voltage Level	Description
C3, C4, C5, C8, C9, C10, C11, D2	AVDDP9_UFP	0.95V	UFP analog power
L4, L5, L6, L7, L8, L9	AVDDP9_DFP	0.95V	DFP analog power
E10, F10, G4, G10, H4, J10, K10, L10	DVDDP9	0.95V	Core 0.9 V power
D3, D4, D5, D8, D9, D10	AVDD18_UFP	1.8V	UFP analog power
K4, K5, K8, K9	AVDD18_DFP	1.8V	DFP analog power
D11, E11, H3, J3, K11, L11	DVDD18	1.8V	1.8V IO power
E13, G3, H11, J11	NC	NA	No connect pins
A1, A4, A10, A13, B2, B3, B4, B5, B6, B8, B9, B10, B11, B12, C2, D1, D6, E2, E3, E4, E5, E6, E7, E8, E9, F2, F3, F4, F5, F6, F7, F8, F9, G5, G6, G7, G8, G9, H5, H6, H7, H8, H9, H10, J2, J4, J5, J6, J7, J8, J9, K6, K7, L1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12, M13, N11	GND	GND	Power return for all supplies

Bootstrap Configuration

DC levels on the bootstrap pins shown below are latched during the de-asserting edge of power-on reset (RESETN goes HIGH).

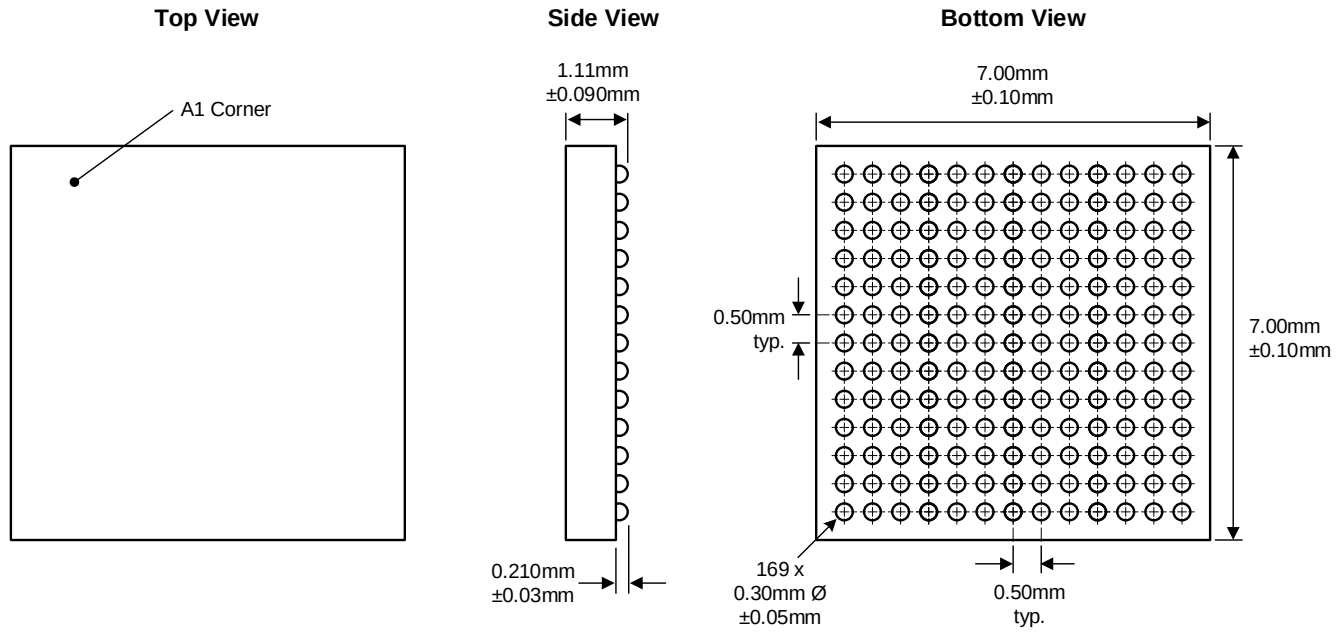
Table 10. Bootstrap Configuration[16]

Bootstrap Signal Name	Assignment	VDD Domain	Internal PU/PD	Function
Bootstrap '0'	GPIO15 (J12)	1.8V	PULL DOWN	Internal. Leave as NC for normal operation.
Bootstrap '1'	GPIO19 (L12)	1.8V	PULL DOWN	Bootstrap assigned by SW. Can be used for customized application configuration
Bootstrap '2'	SPI_CLK (C13)	1.8V	PULL DOWN	Internal. Leave as NC for normal operation.
Bootstrap '3'	GPIO14 (J13)	1.8V	PULL DOWN	Internal. Leave as NC for normal operation.
Bootstrap '4'	SPI_DO (D13)	1.8V	PULL UP	Reference clock select 1 – Crystal Oscillator (Default) 0 – External TCLK
Bootstrap '5'	UTX_GPIO9 (F12)	1.8V	PULL UP	Internal. Leave as NC for normal operation.
Bootstrap '6'	GPIO16 (K13)	1.8V	PULL UP	Bootstrap assigned by SW. Can be used for customized application configuration.
Bootstrap '7'	GPIO17 (K12)	1.8V	PULL UP	Bootstrap assigned by SW. Can be used for customized application configuration.
Bootstrap '8'	GPIO18 (L13)	1.8V	PULL DOWN	Bootstrap assigned by SW. Can be used for customized application configuration.

16. When the pin corresponding to a specific bootstrap is left NC, the pin takes the value of the assigned by the internal PULL UP (Level 1) or PULL DOWN (Level 0). The internal resistor used for 1.8V IO is around 80-95kΩ. To select a non-default value on a bootstrap, use an external PULL-UP or PULL-DOWN resistor tied to the opposite direction that overcomes the internal PULL-UP or PULL-DOWN. Recommended external PULL-UP resistor (14 -16kΩ), PULL-DOWN resistor 2.2kΩ

Packaging Information

TFBGA77-169 (7.00mm x 7.00mm x 1.11mm)



Recommended Footprint