

# Am29833A/Am29853A/Am29855A

## Parity Bus Transceivers

Am29833A/Am29853A/Am29855A

### DISTINCTIVE CHARACTERISTICS

- High-speed bidirectional bus transceivers for processor organized devices
  - T-R delay = 6 ns typical
  - R<sub>p</sub>-Parity delay = 9 ns typical
- Error flag with open-collector output
- Generates odd parity for all-zero protection
- 200-mV minimum input hysteresis (Commercial) on input data ports
- High drive capability:
  - 48 mA Commercial I<sub>OL</sub>
  - 32 mA Military I<sub>OL</sub>
- Higher speed, lower power versions of the Am29833 & Am29853
- Am29855A adds new functionality

### GENERAL DESCRIPTION

The Am29833A, Am29853A, and Am29855A are high-performance parity bus transceivers designed for two-way communications. Each device can be used as an 8-bit transceiver, as well as a 9-bit parity checker/generator. In the transmit mode, data is read at the R port and output at the T port with a parity bit. In the receive mode, data and parity are read at the T port, and the data is output at the R port along with an ERR flag showing the result of the parity test.

In the Am29833A, the error flag is clocked and stored in a register which is read at the open-collector ERR output. The CLR input is used to clear the error flag register. In the Am29853A, a latch replaces this register, and the EN and CLR controls are used to pass, store, sample or clear the error flag output. When both output enables are disabled in the Am29853A and Am29833A, the parity logic defaults to

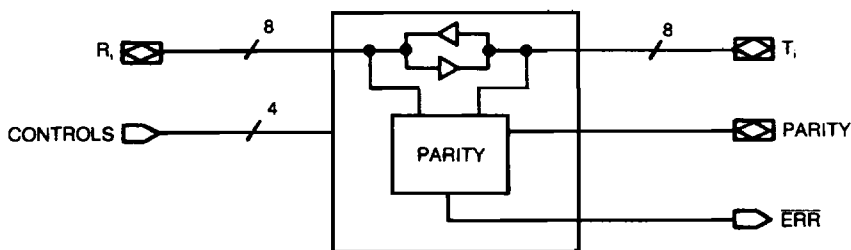
the transmit mode, so that the ERR pin reflects the parity of the R port. The Am29855A, a variation of the Am29853A, is designed so that when both output enables are HIGH, the ERR pin retains its current state.

The output enables,  $\overline{OER}$  and  $\overline{OET}$ , are used to force the port outputs to the high-impedance state so that other devices can drive bus lines directly. In addition, the user can force a parity error by enabling both  $\overline{OER}$  and  $\overline{OET}$  simultaneously. This transmission of inverted parity gives the designer more system diagnostic capability.

Each of these devices is produced with AMD's proprietary IMOX\* bipolar process, and features typical propagation delays of 6 ns, as well as high-capacitive drive capability. Package options include DIPs, PLCCs, LCCs, SOICs, and Flatpacks.

### SIMPLIFIED BLOCK DIAGRAM

#### Parity Transceivers

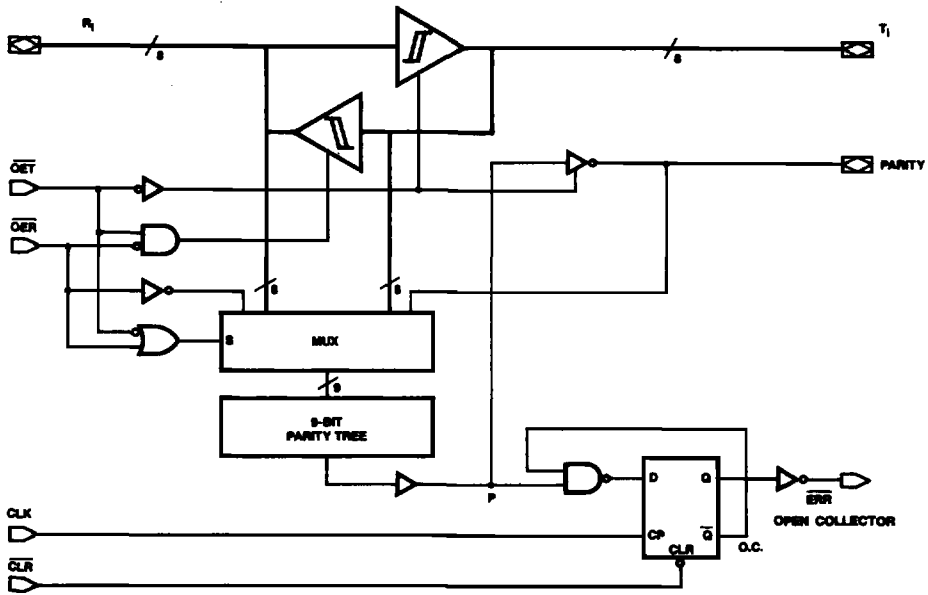


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\*IMOX is a trademark of Advanced Micro Devices, Inc.

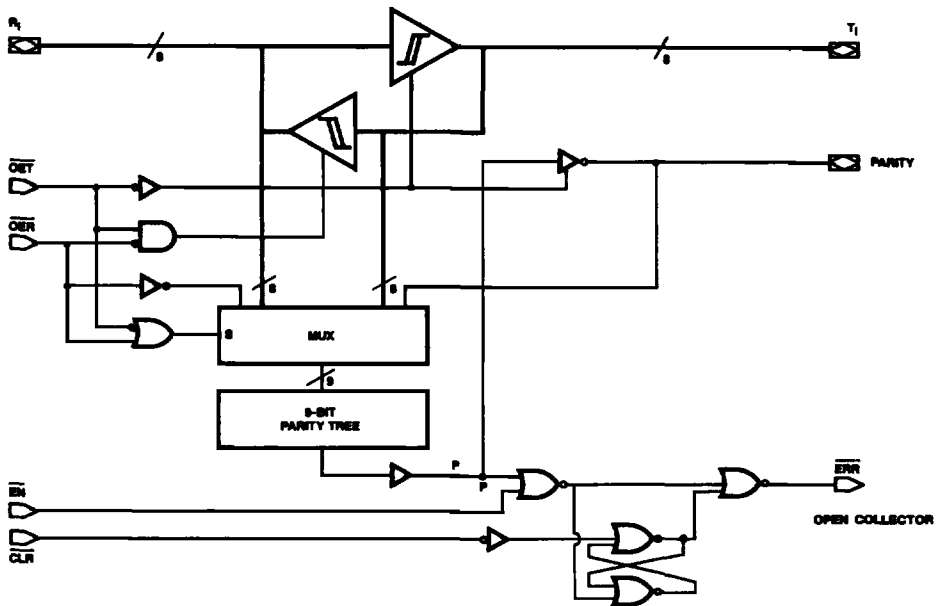
BLOCK DIAGRAMS\*

Am29833A



BD001043

Am29853A

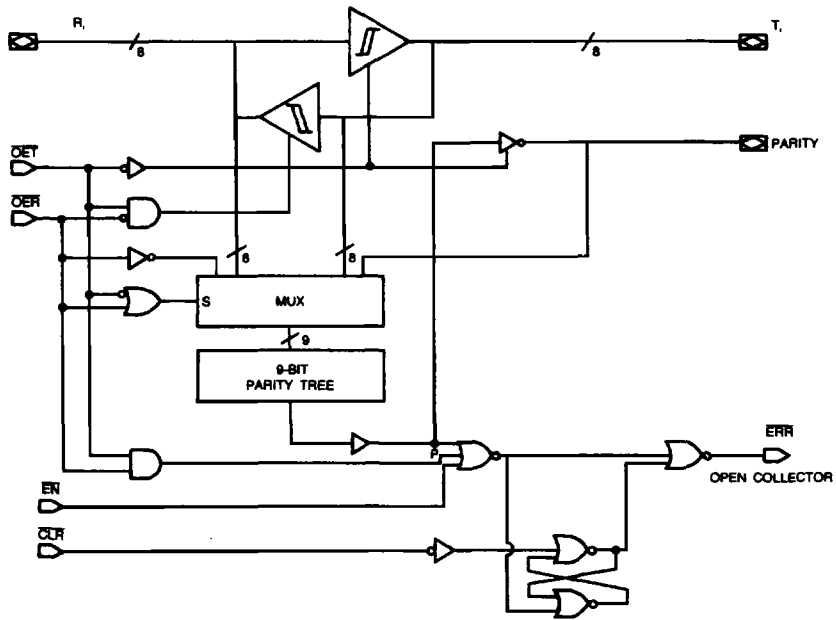


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\*See following page for additional Block Diagrams.

BLOCK DIAGRAMS (Cont'd.)

Am29855A



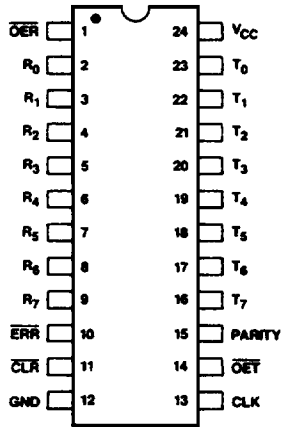
BD005560

# CONNECTION DIAGRAMS Top View

Am29833A/Am29853A/Am29855A

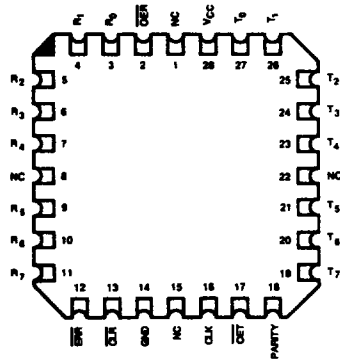
## Am29833

**DIPs\***



CD001120

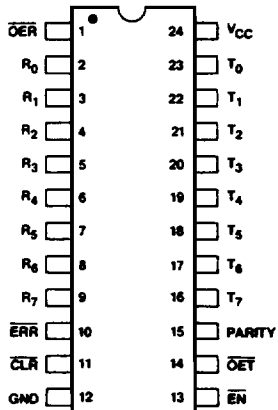
**LCC\*\***



CD001398

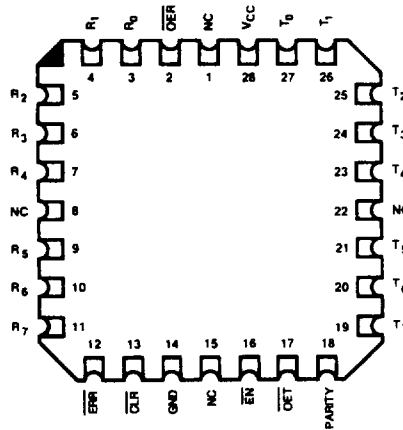
## Am29853/Am29855

**DIPs\***



CD001130

**LCC\*\***



CD001399

\*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.

\*\*Also available in 28-Pin PLCC; pinout identical to LCC.

## FUNCTION TABLES

### Am29833A (Register Option)

Inputs								Outputs				Function
$\overline{OET}$	$\overline{OER}$	$\overline{CLR}$	CLK	$R_i$	Sum of H's of $R_i$	$T_i$	Sum of H's ( $T_i + \text{Parity}$ )	$R_i$	$T_i$	Parity	ERR	
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	H	↑	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	H	↑	NA	NA	L	EVEN	H	NA	NA	L	
H	L	H	↑	NA	NA	L	EVEN	L	NA	NA	L	
X	X	L	X	X	X	X	X	X	X	X	H	Clear error flag register.
H	H	H	X	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled.
H	H	L	X	X	X	X	X	Z	Z	Z	H	
H	H	H	↑	L	ODD	X	X	Z	Z	Z	H	Parity logic defaults to transmit mode. Forced-error checking.
H	H	H	↑	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

H = HIGH  
 L = LOW  
 ↑ = LOW-to-HIGH Transition of Clock  
 X = Don't Care

Z = High Impedance  
 NA = Not Applicable  
 \* = Store the Error State of the Last Receive Cycle

ODD = Odd Number  
 Even = Even Number  
 i = 0, 1, 2, 3, 4, 5, 6, 7

### TRUTH TABLE

#### Error Flag Output

#### Am29833A

Inputs		Internal to Device	Outputs Pre-state	Output	Function
CLR	CLK	Point "P"	ERR <sub>n-1</sub>	ERR	
H	↑	H	H	H	Sample (1's Capture)
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

Note:  $\overline{OET}$  is HIGH and  $\overline{OER}$  is LOW.

**FUNCTION TABLES (Cont'd.)**

**Am29853A (Latch Option)**

Inputs								Outputs				Function
OET	OER	CLR	EN	R <sub>i</sub>	Sum of H's of R <sub>i</sub>	T <sub>i</sub>	Sum of H's (T <sub>i</sub> + Parity)	R <sub>i</sub>	T <sub>i</sub>	Parity	ERR	
L	H	X	X	H	ODD	NA	NA	NA	H	L	NA	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	NA	
L	H	X	X	L	ODD	NA	NA	NA	L	L	NA	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	NA	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled. Parity logic defaults to transmit mode
H	H	L	H	X	X	X	X	Z	Z	Z	H	
H	H	X	L	L	ODD	X	X	Z	Z	Z	H	
H	H	X	L	H	EVEN	X	X	Z	Z	Z	L	
L	L	X	X	H	ODD	NA	NA	NA	H	H	NA	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	NA	
L	L	X	X	L	ODD	NA	NA	NA	L	H	NA	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	NA	

**Am29855A (Latch Option)**

Inputs								Outputs				Function
OET	OER	CLR	EN	R <sub>i</sub>	Sum of H's of R <sub>i</sub>	T <sub>i</sub>	Sum of L's (T <sub>i</sub> + Parity)	R <sub>i</sub>	T <sub>i</sub>	Parity	ERR	
L	H	X	X	H	ODD	NA	NA	NA	H	L	*	Transmit mode: transmits data from R port to T port, generating parity. Receive path is disabled.
L	H	X	X	H	EVEN	NA	NA	NA	H	H	*	
L	H	X	X	L	ODD	NA	NA	NA	L	L	*	
L	H	X	X	L	EVEN	NA	NA	NA	L	H	*	
H	L	L	L	NA	NA	H	ODD	H	NA	NA	H	Receive mode: transmits data from T port to R port with parity test resulting in error flag. Transmit path is disabled.
H	L	L	L	NA	NA	H	EVEN	H	NA	NA	L	
H	L	L	L	NA	NA	L	ODD	L	NA	NA	H	
H	L	L	L	NA	NA	L	EVEN	L	NA	NA	L	
H	L	H	H	NA	NA	X	X	X	NA	NA	*	Store the state of error flag latch.
X	X	L	H	X	X	X	X	X	NA	NA	H	Clear error flag latch.
H	H	H	H	X	X	X	X	Z	Z	Z	*	Both transmitting and receiving paths are disabled.
H	H	L	H	X	X	X	X	Z	Z	Z	H	
L	L	X	X	H	ODD	NA	NA	NA	H	H	*	Forced-error checking.
L	L	X	X	H	EVEN	NA	NA	NA	H	L	*	
L	L	X	X	L	ODD	NA	NA	NA	L	H	*	
L	L	X	X	L	EVEN	NA	NA	NA	L	L	*	

H = HIGH  
 L = LOW  
 † = LOW-to-HIGH transition of clock  
 X = Don't Care

Z = High impedance  
 NA = Not applicable  
 \* = Store the Error state of the last Receive cycle

Odd = Odd number  
 Even = Even number  
 i = 0, 1, 2, 3, 4, 5, 6, 7

### TRUTH TABLE Error Flag Output

#### Am29853A/Am29855A

Inputs		Internal to Device	Outputs Pre-state	Output	Function
EN	CLR	Point "P"	ERR <sub>n-1</sub>	ERR	
L	L	L	X	L	Pass
L	L	H	X	H	
L	H	L	X	L	Sample (1's Capture)
L	H	X	L	L	
L	H	H	H	H	
H	L	X	X	H	Clear
H	H	X	L	L	Store
H	H	X	H	H	

Note:  $\overline{OET}$  is HIGH and  $\overline{OER}$  is LOW.

### ORDERING INFORMATION Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Package Type
- d. Temperature Range
- e. Optional Processing

AM29833A

P

C

B

e. **OPTIONAL PROCESSING**  
Blank = Standard processing  
B = Burn-in

d. **TEMPERATURE RANGE**  
C = Commercial (0 to +70°C)  
E = Extended Military (-55 to +125°C)

c. **PACKAGE TYPE**  
P = 24-Pin Slim Plastic DIP (PD3024)  
D = 24-Pin Slim Ceramic DIP (CD3024)  
S = 24-Pin Plastic Small Outline Package (SO 024)  
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)  
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. **SPEED OPTION**  
Not Applicable

a. **DEVICE NUMBER/DESCRIPTION**  
Am29833A Parity Transceiver, Register Option  
Am29853A Parity Transceiver, Latch Option  
Am29855A Parity Transceiver, Latch Option (New Functionality)

Valid Combinations	
AM29833A	PC, PCB, DC, DCB, DE, SC, JC, LC
AM29853A	
AM29855A	

#### Valid Combinations

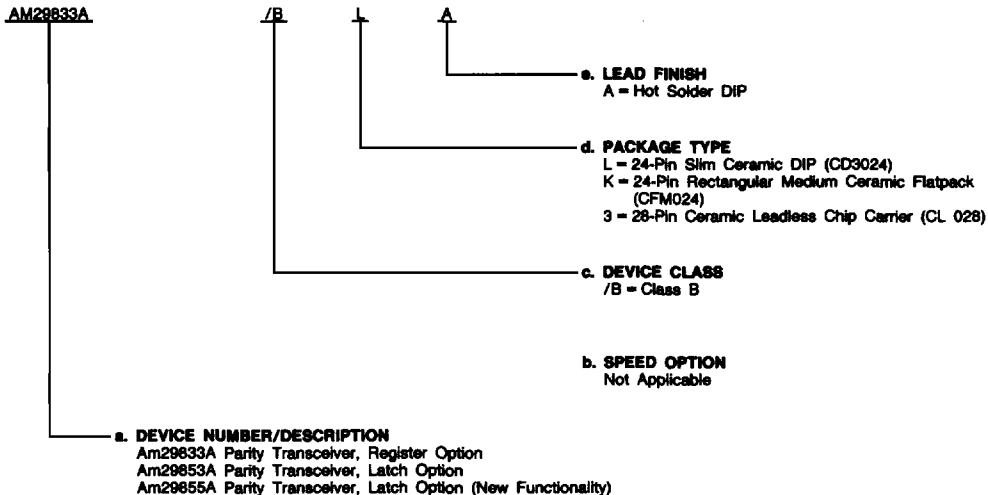
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

# ORDERING INFORMATION (Cont'd.)

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. Device Number
- b. Speed Option (if applicable)
- c. Device Class
- d. Package Type
- e. Lead Finish



Valid Combinations	
AM29833A	/BLA, /BKA, /B3A
AM29853A	
AM29855A	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups  
 1, 2, 3, 7, 8, 9, 10, 11.

Am29833A/Am29853A/Am29855A



## PIN DESCRIPTION

## Am29833A, Am29853A/Am29855A

**OER** Output Enable-Receive (Input, Active LOW)

When LOW in conjunction with  $\overline{\text{OET}}$  HIGH, the devices are in the Receive mode ( $R_i$  are outputs,  $T_i$  and Parity are inputs).

**OET** Output Enable-Transmit (Input, Active LOW)

When LOW in conjunction with  $\overline{\text{OER}}$  HIGH, the devices are in the Transmit mode ( $R_i$  are inputs,  $T_i$  and Parity are outputs).

 **$R_i$**  Receive Port (Input/Output, Three-State)

$R_i$  are the 8-bit data inputs in the Transmit mode, and the outputs in the Receive mode.

 **$T_i$**  Transmit Port (Input/Output, Three-State)

$T_i$  are the 8-bit data outputs in the Transmit mode, and the inputs in the Receive mode.

**Parity** Parity Flag (Input/Output, Three-State)

In the Transmit mode, the Parity signal is an active output used to generate odd parity. In the Receive mode, the  $T_i$  and Parity inputs are combined and checked for odd parity. When both output enables are HIGH, the Parity Flag is in the high impedance state. When both output enables are LOW, the Parity bit forces a parity error.

## Am29833A Only

**ERR** Error Flag (Output, Open Collector)

In the Receive mode, the parity of the  $T_i$  bits is calculated and compared to the Parity input.  $\overline{\text{ERR}}$  goes LOW when the comparison indicates a parity error.  $\overline{\text{ERR}}$  stays LOW until the register is cleared.

 **$\overline{\text{CLR}}$**  Clear (Input, Active LOW)

When  $\overline{\text{CLR}}$  goes LOW, the Error Flag Register is cleared ( $\overline{\text{ERR}}$  goes HIGH).

**CLK** Clock (Input, Positive Edge-Triggered)

This pin is the clock input for the Error Flag register.

## Am29853A/Am29855A Only

**ERR** Error Flag (Output, Open Collector)

In the Receive mode, the parity of the  $T_i$  bits is calculated and compared to the Parity input.  $\overline{\text{ERR}}$  goes LOW when the comparison indicates a parity error.  $\overline{\text{ERR}}$  stays LOW until the latch is cleared. In the Am29855A, the error flag will retain its previous state when  $\overline{\text{OET}}$  and  $\overline{\text{OER}}$  are HIGH.

 **$\overline{\text{CLR}}$**  Clear (Input, Active LOW)

When  $\overline{\text{CLR}}$  goes LOW and  $\overline{\text{EN}}$  is HIGH, the Error Flag latch is cleared ( $\overline{\text{ERR}}$  goes HIGH).

**EN** Latch Enable (Input, Active LOW)

This pin is the latch enable for the Error Flag latch.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature .....	-65 to +150°C
Ambient Temperature with Power Applied .....	-55 to +125°C
Supply Voltage to Ground Potential Continuous .....	-0.5 V to +7.0 V
DC Voltage Applied to Output for High Output State .....	-0.5 V to +5.5 V
DC Input Voltage .....	-1.5 V to +6.0 V
DC Output Current, into Outputs .....	100 mA
DC Input Current .....	-30 mA to +5.0 mA

Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**OPERATING RANGES**

Commercial (C) Devices	
Temperature (T <sub>A</sub> ) .....	0 to +70°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V
Military (M) Devices	
Temperature (T <sub>C</sub> ) .....	-55 to +125°C
Supply Voltage (V <sub>CC</sub> ) .....	+4.5 V to +5.5 V


Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
V <sub>OH</sub>	Output HIGH Voltage (Except ERR)	V <sub>CC</sub> = 4.5 V V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -15 mA I <sub>OH</sub> = -24 mA	2.4 2.0		V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = 4.5 V V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	ERR		0.5	V
			All Other Outputs	I <sub>OL</sub> = 48 mA I <sub>OL</sub> = 32 mA MIL	0.5	
				I <sub>OL</sub> = 48 mA COM'L	0.5	
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 1)		2.0		V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 1)	COM'L		0.8	V
			MIL		0.7	
V <sub>I</sub>	Input Clamp Voltage	V <sub>CC</sub> = 4.5 V, I <sub>IN</sub> = -18 mA			-1.2	V
V <sub>HYST</sub>	Hysteresis for Inputs R <sub>i</sub> , T <sub>i</sub>		COM'L	200		mV
			MIL	150		
I <sub>ZL</sub>	I/O Port LOW Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V			-550	μA
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0.4 V			-0.5	mA
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V			50	μA
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = 5.5 V			100	μA
I <sub>ZH</sub>	I/O Port HIGH Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 2.7 V			100	μA
I <sub>ZI</sub>	I/O Port HIGH Current	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V			150	μA
I <sub>SC</sub>	Output Short-Circuit Current	V <sub>CC</sub> = 5.5 V, V <sub>OUT</sub> = 0.0 V (Note 2)		-75	-250	mA
I <sub>OFF</sub>	Bus Leakage Current	V <sub>CC</sub> = 0 V, V <sub>OUT</sub> = 2.9 V			100	μA
I <sub>CC</sub>	Power Supply Current	V <sub>CC</sub> = 5.5 V Outputs Unloaded	Outputs LOW		180	mA
			Outputs HIGH		155	
			Outputs Hi-Z		170	

- Notes:** 1. Input thresholds are tested during DC parameter testing, and may be tested in combination with other DC parameters.  
2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions*	COM'L		MIL		Units	
			Min.	Max.	Min.	Max.		
t <sub>PLH</sub>	Propagation Delay R <sub>i</sub> to T <sub>i</sub> , T <sub>i</sub> to R <sub>i</sub>	C <sub>L</sub> = 50 pF R <sub>1</sub> = 500 Ω R <sub>2</sub> = 500 Ω		10		14	ns	
t <sub>PHL</sub>				10		14	ns	
t <sub>PLH</sub>	Propagation Delay R <sub>i</sub> to Parity			15		20	ns	
t <sub>PHL</sub>				15		20	ns	
t <sub>ZH</sub>	Output Enable Time $\overline{OER}$ , $\overline{OET}$ to R <sub>i</sub> , T <sub>i</sub> and Parity			12		16	ns	
t <sub>ZL</sub>				12		16	ns	
t <sub>HZ</sub>	Output Disable Time $\overline{OER}$ , $\overline{OET}$ to R <sub>i</sub> , T <sub>i</sub> and Parity			12		16	ns	
t <sub>LZ</sub>					12		16	ns
t <sub>S</sub>	T <sub>i</sub> , Parity to CLK Setup Time (Note 1)			12		16	ns	
t <sub>H</sub>	T <sub>i</sub> , Parity to CLK Hold Time (Note 1)			0		0	ns	
t <sub>REC</sub>	Clear ( $\overline{CLR}$  ) to CLK Setup Time (Note 2)			15		20	ns	
t <sub>PWH</sub>	Clock Pulse Width (Note 1)		HIGH	7		9.5	ns	
t <sub>PWL</sub>			LOW	7		9.5	ns	
t <sub>PWL</sub>	Clear Pulse Width		LOW	7		9.5	ns	
t <sub>PHL</sub>	Propagation Delay CLK to $\overline{ERR}$ (Note 1)				12		16	ns
t <sub>PLH</sub>	Propagation Delay $\overline{CLR}$ to $\overline{ERR}$				16		20	ns
t <sub>PLH</sub>	Propagation-Delay T <sub>i</sub> , Parity to $\overline{ERR}$ (PASS Mode Only) Am29853A/Am29855A			22		25	ns	
t <sub>PHL</sub>					18		20	ns
t <sub>PLH</sub>	Propagation Delay $\overline{OER}$ to Parity			15		20	ns	
t <sub>PHL</sub>					15		20	ns

\*See test circuit and waveforms

- Notes: 1. For Am29853A/Am29855A, replace CLK with  $\overline{EN}$ .  
2. Not applicable to Am29853A/Am29855A.