DATA SHEET

74LVT16373A

3.3V LVT 16-bit transparent D-type latch (3-State)

Product specification
Supersedes data of 1994 Dec 15
IC23 Data Handbook

1998 Feb 19

Philips
Semiconductors

PHILIPS

3.3V 16-bit transparent D-type latch (3-State) 74LVT16373A

FEATURES

- 16-bit transparent latch
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74LVT16373A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is a 16-bit transparent D-type latch with non-inverting 3-State bus compatible outputs. The device can be used as two 8-bit latches or one 16-bit latch. When enable (E) input is High, the Q outputs follow the data (D) inputs. When enable is taken Low, the Q outputs are latched at the levels of the D inputs one setup time prior to the High-to-Low transition.

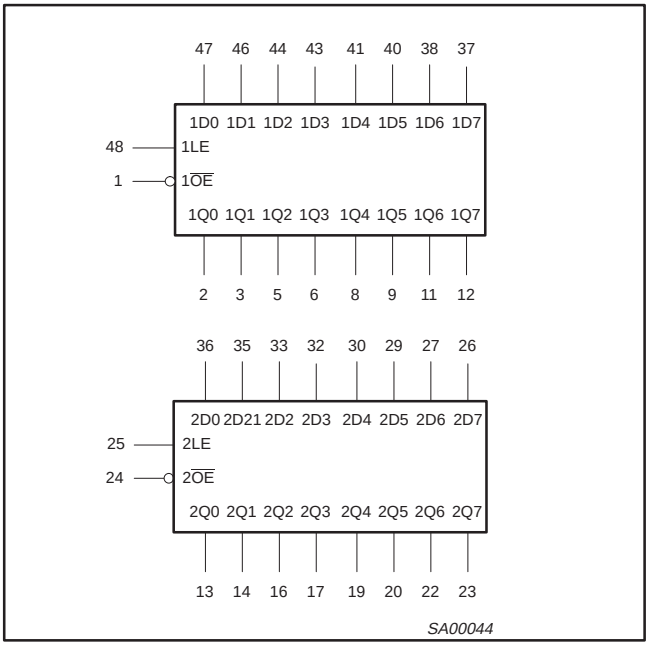
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	C_L = 50pF; V_{CC} = 3.3V	1.9	ns
C_{IN}	Input capacitance	V_I = 0V or 3.0V	3	pF
C_{OUT}	Output capacitance	Outputs disabled; V_O = 0V or 3.0V	9	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} = 3.6V	70	µA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	–40°C to +85°C	74LVT16373A DL	VT16373A DL	SOT370-1
48-Pin Plastic TSSOP Type II	–40°C to +85°C	74LVT16373A DGG	VT16373A DGG	SOT362-1

LOGIC SYMBOL

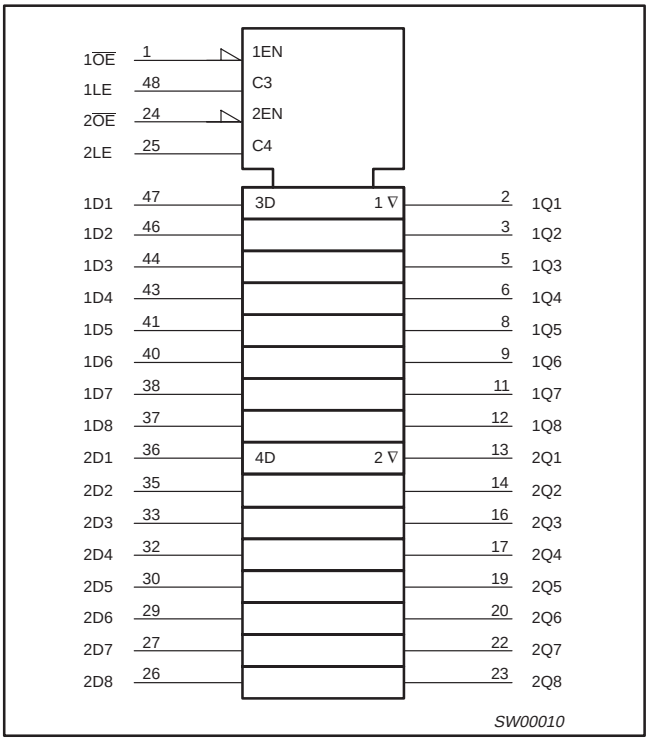


PIN DESCRIPTION

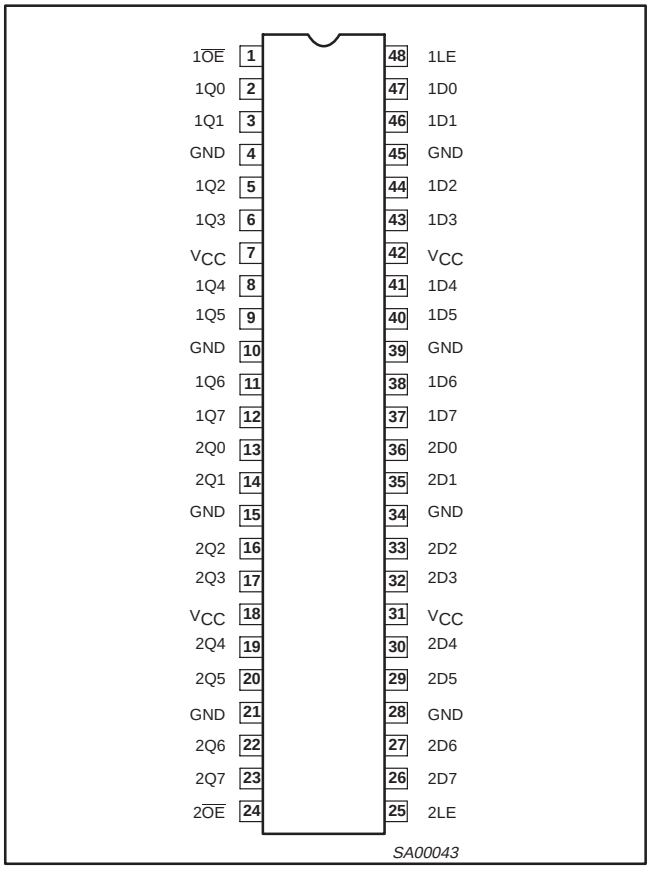
PIN NUMBER	SYMBOL	FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1D0 – 1D7 2D0 – 2D7	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1Q0 – 1Q7 2Q0 – 2Q7	Data outputs
1, 24	$1\overline{OE}$, $2\overline{OE}$	Output enable inputs (active-Low)
48, 25	1E, 2E	Enable inputs (active-High)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive supply voltage

3.3V 16-bit transparent D-type latch (3-State) 74LVT16373A

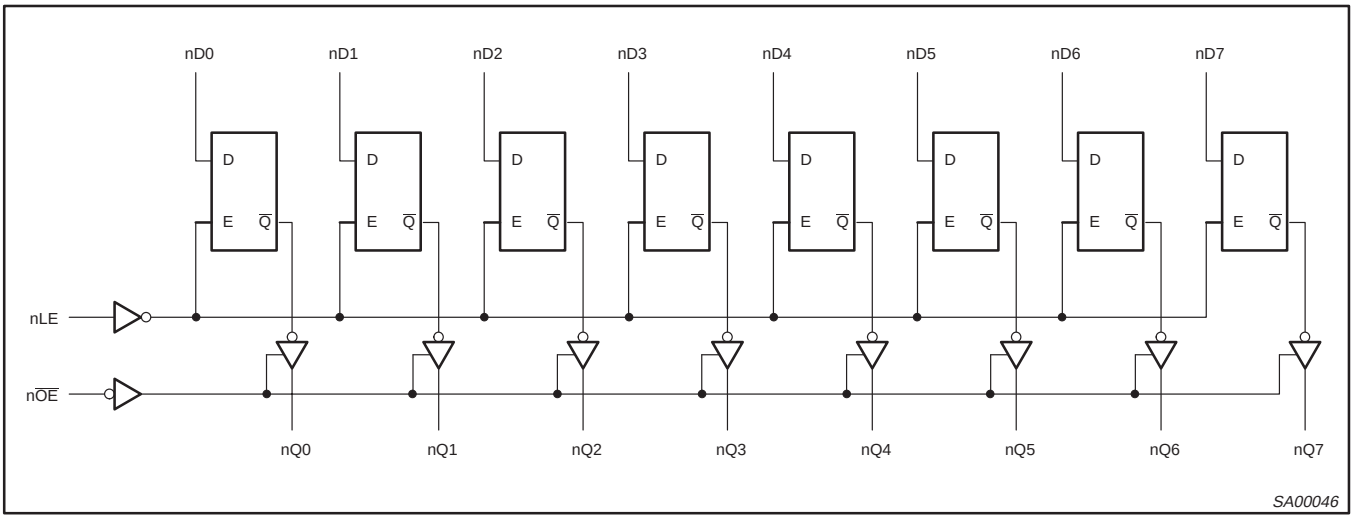
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$n\overline{OE}$	nE	nDx		nQ0 – nQ7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X nDx	NC nDx	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	–50	mA
V_I	DC input voltage[3]		–0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	Output in Off or High state	–0.5 to +7.0	V
I_{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	–64	
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	2.7	3.6	V
V_I	Input voltage	0	5.5	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		32	mA
	Low-level output current; current duty cycle ≤ 50%; f ≥ 1kHz		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage	V_{CC} = 2.7V; I_{IK} = –18mA			–.85	–1.2	V
V_{OH}	High-level output voltage	V_{CC} = 2.7 to 3.6V; I_{OH} = –100µA		V_{CC}-0.2	V_{CC}		V
		V_{CC} = 2.7V; I_{OH} = –8mA		2.4	2.5		
		V_{CC} = 3.0V; I_{OH} = –32mA		2.0	2.3		
V_{OL}	Low–level output voltage	V_{CC} = 2.7V; I_{OL} = 100µA			0.07	0.2	V
		V_{CC} = 2.7V; I_{OL} = 24mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 16mA			0.25	0.4	
		V_{CC} = 3.0V; I_{OL} = 32mA			0.3	0.5	
		V_{CC} = 3.0V; I_{OL} = 64mA			0.4	0.55	
V_{RST}	Power-up output Low voltage[5]	V_{CC} = 3.6V; I_O = 1mA; V_I = GND or V_{CC}			0.1	0.55	V
I_I	Input leakage current	V_{CC} = 3.6V; V_I = V_{CC} or GND	Control pins		0.1	±1	µA
		V_{CC} = 0 or 3.6V; V_I = 5.5V			0.4	10	
		V_{CC} = 3.6V; V_I = V_{CC}	Data pins[4]		0.1	1	
		V_{CC} = 3.6V; V_I = 0			-0.4	-5	
I_{OFF}	Output off current	V_{CC} = 0V; V_I or V_O = 0 to 4.5V			0.1	±100	µA
I_{HOLD}	Bus Hold current D inputs[7]	V_{CC} = 3V; V_I = 0.8V		75	135		µA
		V_{CC} = 3V; V_I = 2.0V		–75	-135		
		V_{CC} = 0V to 3.6V; V_{CC} = 3.6V		±500			
I_{EX}	Current into an output in the High state when V_O > V_{CC}	V_O = 5.5V; V_{CC} = 3.0V			50	125	µA
$I_{PU/PD}$	Power up/down 3-State output current[3]	$V_{CC} \leq$ 1.2V; V_O = 0.5V to V_{CC}; V_I = GND or V_{CC}; $\overline{OE}$ = Don't care			1	±100	µA
I_{OZH}	3-State output High current	V_{CC} = 3.6V; V_O = 3.0V; V_I = V_{IH} or V_{IL}			0.5	5	µA
I_{OZL}	3-State output Low current	V_{CC} = 3.6V; V_O = 0.5V; V_I = V_{IH} or V_{IL}			0.5	–5	
I_{CCH}	Quiescent supply current	V_{CC} = 3.6V; Outputs High, V_I = GND or V_{CC}, I_O = 0			0.07	0.12	mA
I_{CCL}		V_{CC} = 3.6V; Outputs Low, V_I = GND or V_{CC}, I_O = 0			4.0	6	
I_{CCZ}		V_{CC} = 3.6V; Outputs Disabled; V_I = GND or V_{CC}, I_O = 0[6]			0.07	0.12	
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 3V to 3.6V; One input at V_{CC}-0.6V, Other inputs at V_{CC} or GND			0.1	0.2	mA

NOTES:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V_{CC} = 3.3V ±0.3V			V_{CC} = 2.7V	
			MIN	TYP[1]	MAX	MAX	
t_{PLH} t_{PHL}	Propagation delay nDx to nQx	2	0.5 0.5	1.8 1.9	3.9 3.9	4.5 4.5	ns
t_{PLH} t_{PHL}	Propagation delay nE to nQx	1	0.5 0.5	2.1 2.2	4.8 4.8	5.4 5.4	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	4 5	0.1 0.1	2.8 2.6	4.5 4.3	5.1 4.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low Level	4 5	0.1 0.1	3.3 3.0	4.5 4.3	5.1 4.7	ns

NOTE:
1. All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

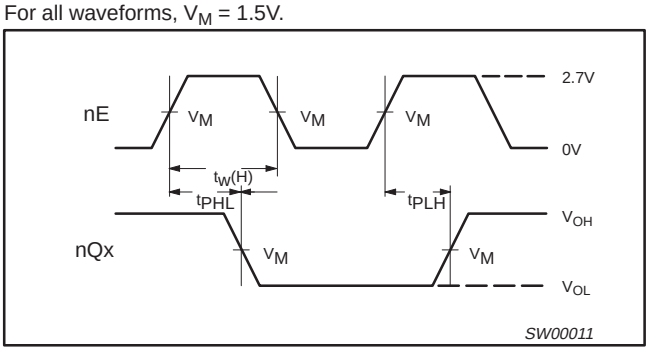
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = –40°C to +85°C.

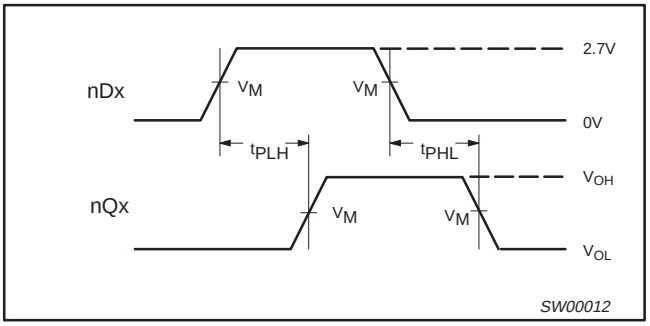
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V_{CC} = 3.3V ±0.3V		V_{CC} = 2.7V	
			MIN	TYP	MIN	
t_S(H) t_S(L)	Setup time nDx to nE	3	1.5 2.0	0.1 0.2	1.0 2.0	ns
t_h(H) t_h(L)	Hold time nDx to nE	3	1.0 1.5	0 0	1.0 2.0	ns
t_W(H)	nE pulse width High	1	1.5	0.5	1.5	ns

AC WAVEFORMS

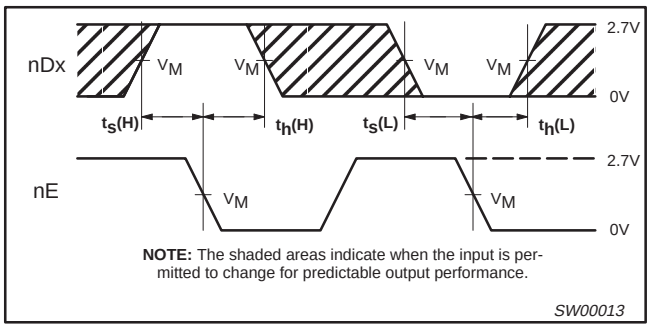
For all waveforms, V_M = 1.5V.



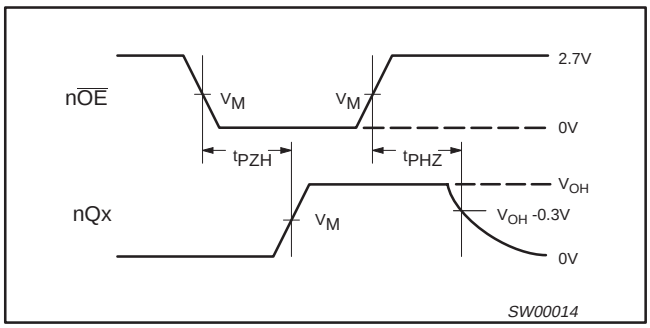
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width



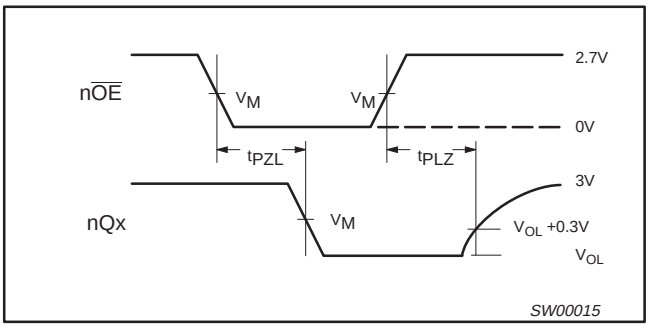
Waveform 2. Propagation Delay for Data to Outputs



Waveform 3. Data Setup and Hold Times

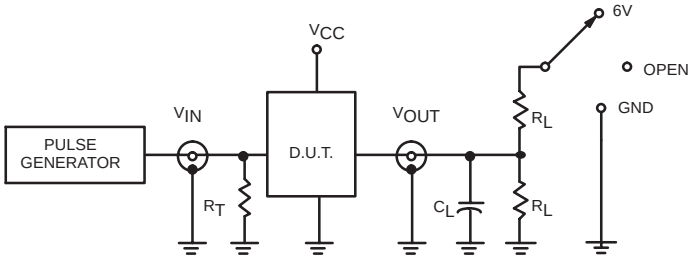


Waveform 4. 3-State Output Enable time to High Level and Output Disable Time from High Level

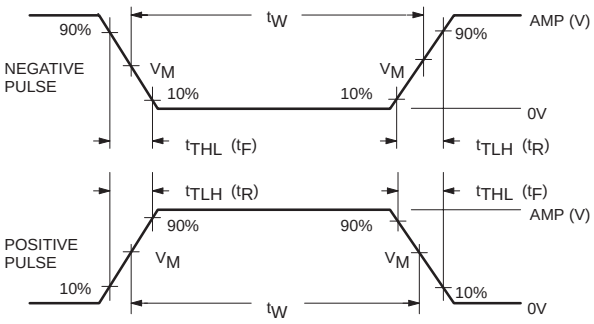


Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS



Test Circuit for 3-State Outputs



V_M = 1.5V
Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

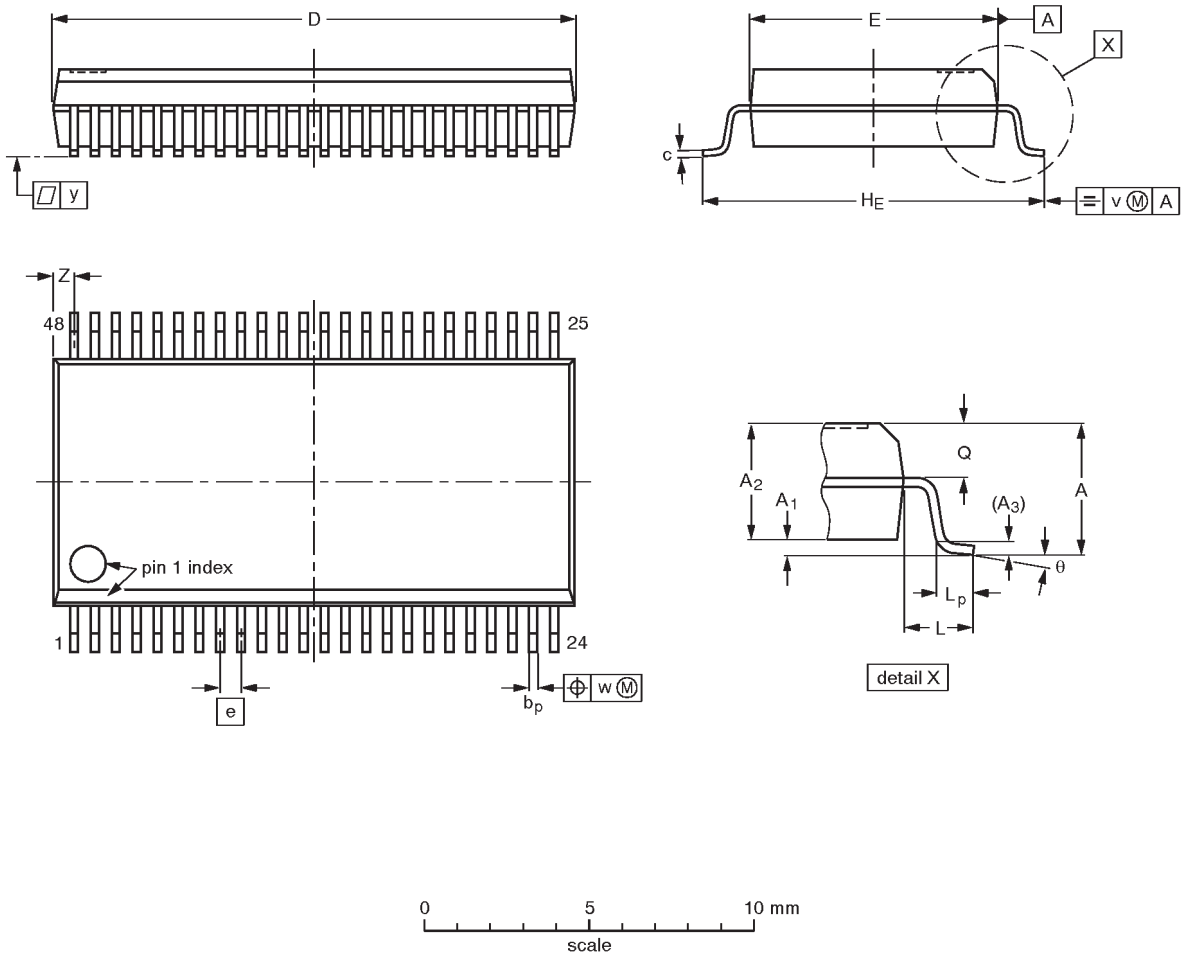
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

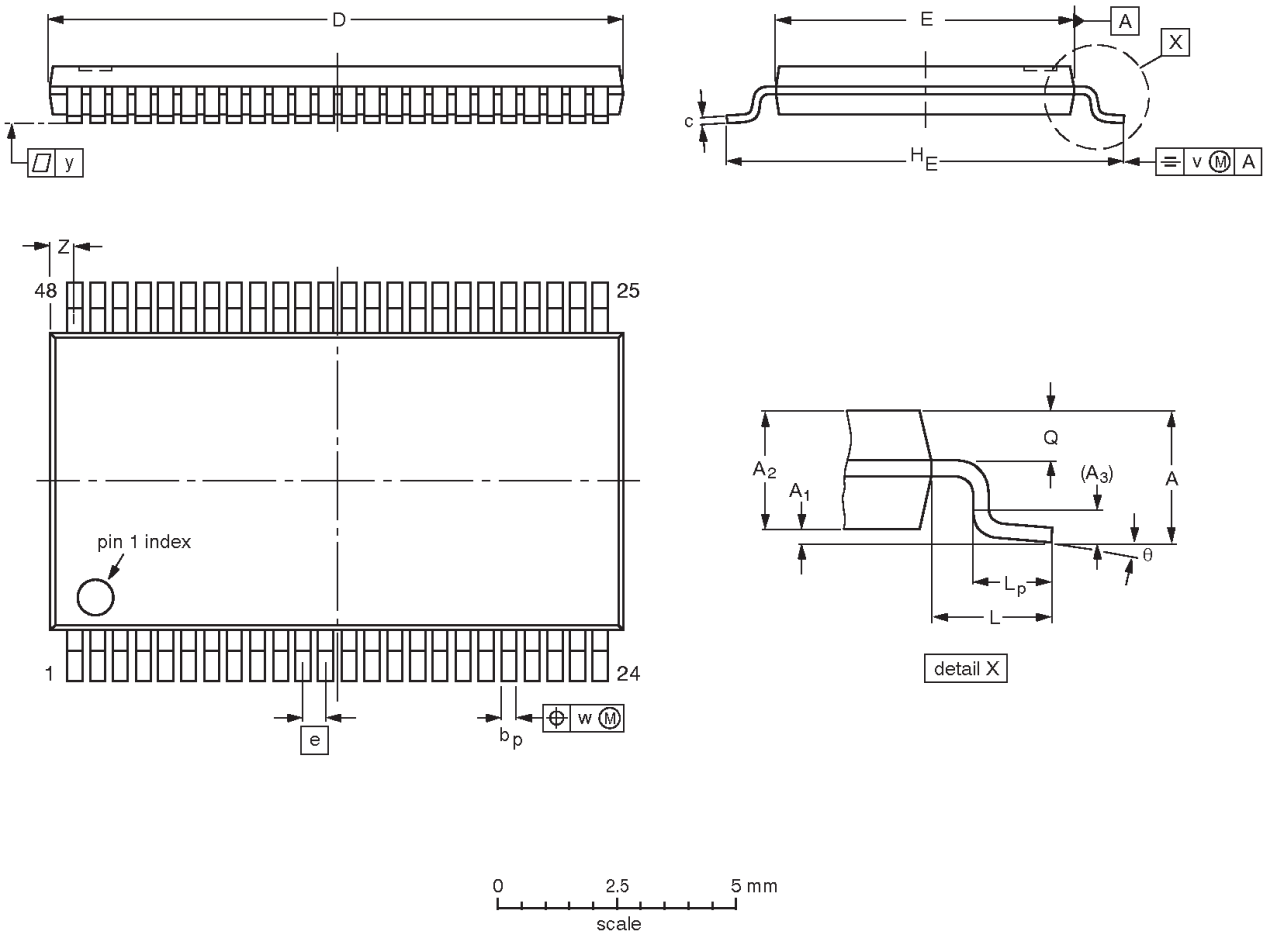
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT370-1		MO-118AA				~~93-11-02~~ 95-02-04

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm **SOT362-1**



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT362-1		MO-153ED					~~93-02-03~~ 95-02-10

3.3V LVT 16-bit transparent D-type latch (3-State)

74LVT16373A

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

Definitions

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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74LVT16373A Preview Product information Selection guide

Datasheet

(Product Specification) v.2, 19-Feb-98, 10 Pages, 96kB

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Download all documentation

3.3V LVT 16-bit transparent D-type latch (3-State)

All information hereunder is subject to the subsequent disclaimers

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- View case studies on general applications or technologies
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- Find more information on NXP's Vision
- Find out more about our ordering process
- Receive e-news on specific interest areas

General description

Hide

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This device is a 16-bit transparent D-type latch with non-inverting 3-State bus compatible outputs. The device can be used as two 8-bit latches or one 16-bit latch. When enable (E) input is High, the Q outputs follow the data (D) inputs. When enable is taken Low, the Q outputs are latched at the levels of the D inputs one setup time prior to the High-to-Low transition.

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Features

Hide

16-bit transparent latch
3-State buffers
Output capability: +64mA/-32mA
TTL input and output switching levels
Input and output interface capability to systems at 5V supply
Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
Live insertion/extraction permitted
Power-up reset
Power-up 3-State
No bus current loading when output is tied to 5V bus
Latch-up protection exceeds 500mA per JEDEC Std 17
ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

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Products/packages

Hide

Type number	Orderable part number	Ordering code (12NC)	Product status	Package	Packing	Marking	ECCN

74LVT16373ADGG	74LVT16373ADGG,112	9352 030 90112	Volume production	SOT362-1 (TSSOP48)	Tube	Standard Marking	
74LVT16373ADGG	74LVT16373ADGG,118	9352 030 90118	Volume production	SOT362-1 (TSSOP48)	Reel Pack, SMD, 13"	Standard Marking	
74LVT16373ADL	74LVT16373ADL,112	9351 831 10112	Volume production	SOT370-1 (SSOP48)	Tube	Standard Marking	
74LVT16373ADL	74LVT16373ADL,118	9351 831 10118	Volume production	SOT370-1 (SSOP48)	Tape reel smd	Standard Marking	

The variants in the table below are discontinued. See the table Discontinued information for more information.

Type number	Orderable part number	Ordering code (12NC)	Product status	Package	Packing	Marking	ECCN
74LVT16373ADGG	74LVT16373ADGG,512	9352 030 90512	Withdrawn Replacement product	SOT362-1 (TSSOP48)	Tube Dry Pack	Standard Marking	

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Quality/reliability/chemical content

Hide

Type number	Orderable part number	Chemical content	RoHS	Leadfree conversion date	RHF	IFR (FIT)	MTBF (hours)	MSL Lead-free
74LVT16373ADGG	74LVT16373ADGG,112	74LVT16373ADGG	EU/CN RoHs COMPLIANT	Always Pb-free	D	1,33	7,52E+08	1
74LVT16373ADGG	74LVT16373ADGG,118	74LVT16373ADGG	EU/CN RoHs COMPLIANT	Always Pb-free	D	1,33	7,52E+08	1
74LVT16373ADL	74LVT16373ADL,112	74LVT16373ADL	EU/CN RoHs COMPLIANT	week 13, 2005	G	1,33	7,52E+08	1
74LVT16373ADL	74LVT16373ADL,118	74LVT16373ADL	EU/CN RoHs COMPLIANT	week 13, 2005	G	1,33	7,52E+08	1

The variants in the table below are discontinued. See the table Discontinued information for more information.

Type number	Orderable part number	Chemical content	RoHS	Leadfree conversion date	RHF	IFR (FIT)	MTBF (hours)	MSL Lead-free
74LVT16373ADGG	74LVT16373ADGG,512	74LVT16373ADGG	EU/CN RoHs COMPLIANT	week 14, 2005	G	1,33	7,52E+08	1

Quality and reliability disclaimer

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Pricing/ordering/availability

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Type number	Ordering code (12NC)	Orderable part number	Indicative price/unit($)	Region	Distributor	In stock	Order quantity	Inventory date	Buy online	Samples
74LVT16373ADGG	9352 030 90112	74LVT16373ADGG,112		JAPAN	CHIP ONE STOP	no		03/19/2010	Buy online	not available
74LVT16373ADGG	9352 030 90118	74LVT16373ADGG,118		JAPAN	CHIP ONE STOP	no		03/19/2010	Buy online	Order samples
74LVT16373ADL	9351 831 10112	74LVT16373ADL,112	1.1400	JAPAN	CHIP ONE STOP	no		03/19/2010	Buy online	not available
74LVT16373ADL	9351 831 10118	74LVT16373ADL,118	1.1400	JAPAN	CHIP ONE STOP	no		03/19/2010	Buy online	Order samples

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Discontinued information

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Type number	Ordering code (12NC)	Last-time buy date	Last-time delivery date	Replacement product	DN Notice	Status	Comments
74LVT16373ADGG	935203090512				DN		

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Block diagrams/pinning

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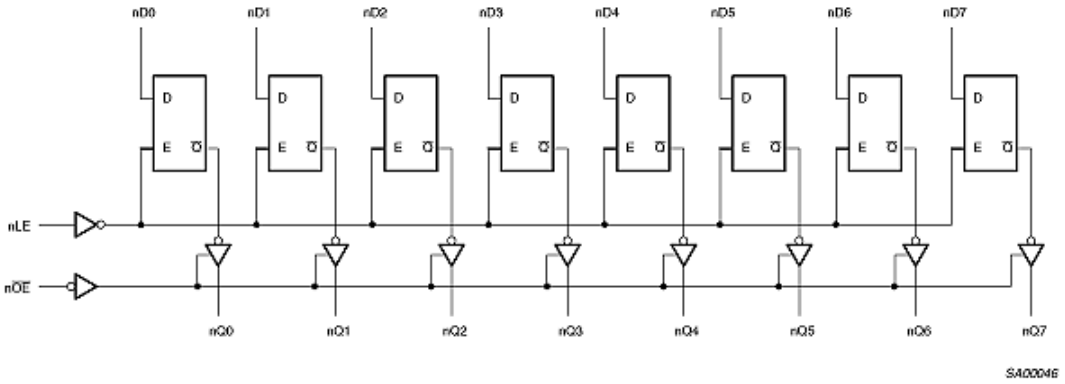

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Design support

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Application Notes

- LVT (Low Voltage Technology) and ALVT (Advanced LVT) (1998-01-01)
- Simulation Support for Philips' Advanced BiCMOS Products (1993-11-01)
- Test Fixtures for High Speed Logic (1998-04-02)
- The Behavior Of Integrated Bus Hold Circuits (1996-03-01)
- Transmission Lines and Terminations with Philips Advanced Logic Families (1998-02-01)

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Parametrics/similar products

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Type number	Package	Description	Propagation Delay (ns)	Voltage	No. of Pins	Logic Switching Levels	Output Drive Capability
74LVT16373ADGG	SOT362-1 (TSSOP48)	3.3V 16-Bit D-Type Transparent Latch (3-State)	1.9@3.3V	2.7-3.6 V	48	TTL	-32/+64 mA
74LVT16373ADL	SOT370-1 (SSOP48)	3.3V 16-Bit D-Type Transparent Latch (3-State)	1.9@3.3V	2.7-3.6 V	48	TTL	-32/+64 mA

Similar products

74LVT16373A links to the similar products page containing an overview of products that are similar in function or related to the type number(s) as listed on this page. The similar products page includes products from the same catalog tree(s), relevant selection guides and products from the same functional category.

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Print this product information

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