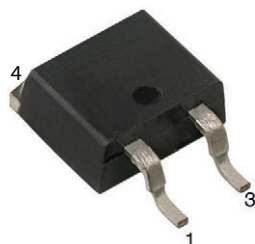
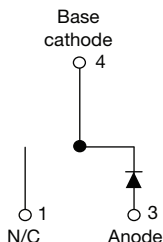


650 V Gen 3 Power SiC Merged PIN Schottky Diode, 20 A


D²PAK 2L (TO-263AB 2L)


FEATURES

- Majority carrier diode using Schottky technology on SiC wide band gap material
- Improved V_F and efficiency by thin wafer technology
- Positive V_F temperature coefficient for easy paralleling
- Virtually no recovery tail and no switching losses
- Temperature invariant switching behavior
- 175 °C maximum operating junction temperature
- Meets MSL level 1, per J-STD-020, LF maximum peak of 245 °C
- MPS structure for high ruggedness to forward current surge events
- Meets JESD 201 class 1A whisker test
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT
HALOGEN
FREE

LINKS TO ADDITIONAL RESOURCES



PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	20 A
V_R	650 V
V_F at I_F at 150 °C	1.5 V
T_J max.	175 °C
I_R at V_R at 175 °C	9 μ A
Q_C ($V_R = 400$ V)	53 nC
Package	D ² PAK 2L (TO-263AB 2L)
Circuit configuration	Single

DESCRIPTION / APPLICATIONS

Wide band gap SiC based 650 V Schottky diode, designed for high performance and ruggedness.

Optimum choice for high speed hard switching and efficient operation over a wide temperature range, it is also recommended for all applications suffering from Silicon ultrafast recovery behavior.

Typical applications include AC/DC PFC and DC/DC ultra high frequency output rectification in FBPS and LLC converters.

MECHANICAL DATA

Case: D²PAK 2L (TO-263AB 2L)

Molding compound meets UL 94 V-0 flammability rating
Base P/N-M3 - halogen-free, RoHS-compliant

Terminals: matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C unless otherwise specified)				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Peak repetitive reverse voltage	V_{RRM}		650	V
Average rectified forward current	$I_{F(AV)}$	$T_C = 111$ °C (DC)	20	A
DC blocking voltage	V_{DC}		650	V
Repetitive peak forward current	I_{FRM}	$T_C = 25$ °C, $f = 50$ Hz, square wave, DC = 25 %	63	A
Non-repetitive peak forward surge current	I_{FSM}	$T_C = 25$ °C, $t_p = 10$ ms, half sine wave	110	
		$T_C = 110$ °C, $t_p = 10$ ms, half sine wave	104	
Power dissipation	$P_{tot}^{(1)}$	$T_C = 25$ °C	93	W
		$T_C = 110$ °C	41	
I^2t value	$\int i^2 dt$	$T_C = 25$ °C	60.5	A ² s
		$T_C = 110$ °C	54	
Operating junction and storage temperatures	$T_J^{(2)}, T_{Stg}$		-55 to +175	°C

Notes

(1) Based on maximum R_{th}

(2) The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{thJA}$

**ELECTRICAL SPECIFICATIONS** ($T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Forward voltage	V_F	$I_F = 20\text{ A}$	-	1.3	1.5	V
		$I_F = 20\text{ A}, T_J = 150\text{ }^{\circ}\text{C}$	-	1.5	1.85	
		$I_F = 20\text{ A}, T_J = 175\text{ }^{\circ}\text{C}$	-	1.60	-	
Reverse leakage current	I_R	$V_R = V_R\text{ rated}$	-	1.3	100	μA
		$V_R = V_R\text{ rated}, T_J = 150\text{ }^{\circ}\text{C}$	-	5.5	250	
		$V_R = V_R\text{ rated}, T_J = 175\text{ }^{\circ}\text{C}$	-	9	-	
Total capacitance	C	$V_R = 1\text{ V}, f = 1\text{ MHz}$	-	845	-	pF
		$V_R = 400\text{ V}, f = 1\text{ MHz}$	-	82	-	
Total capacitive charge	Q_C	$V_R = 400\text{ V}, f = 1\text{ MHz}$	-	53	-	nC

THERMAL - MECHANICAL SPECIFICATIONS ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Thermal resistance, junction to case	R_{thJC}		-	1.2	1.6	$^{\circ}\text{C/W}$
Marking device			3C20ET07S			

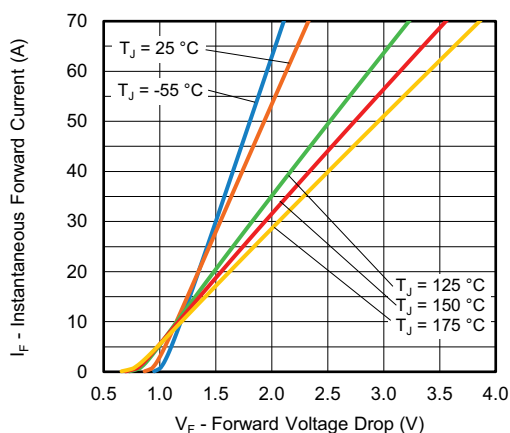


Fig. 1 - Typical Forward Voltage Drop Characteristics

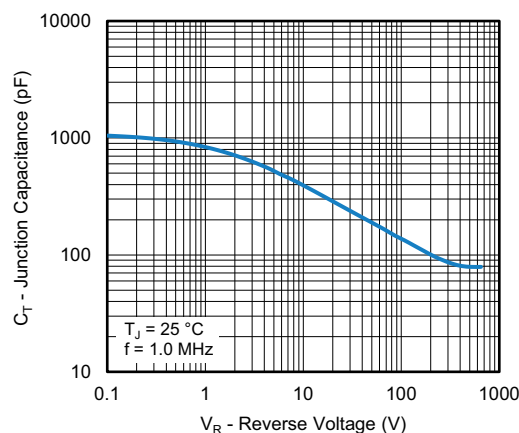


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage

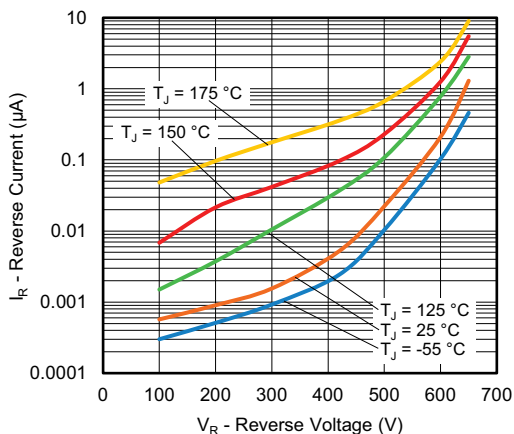


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage

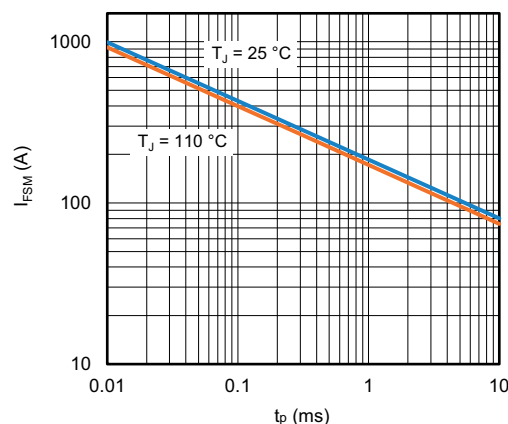


Fig. 4 - Non-Repetitive Peak Forward Surge Current vs. Pulse Duration (Square Wave)

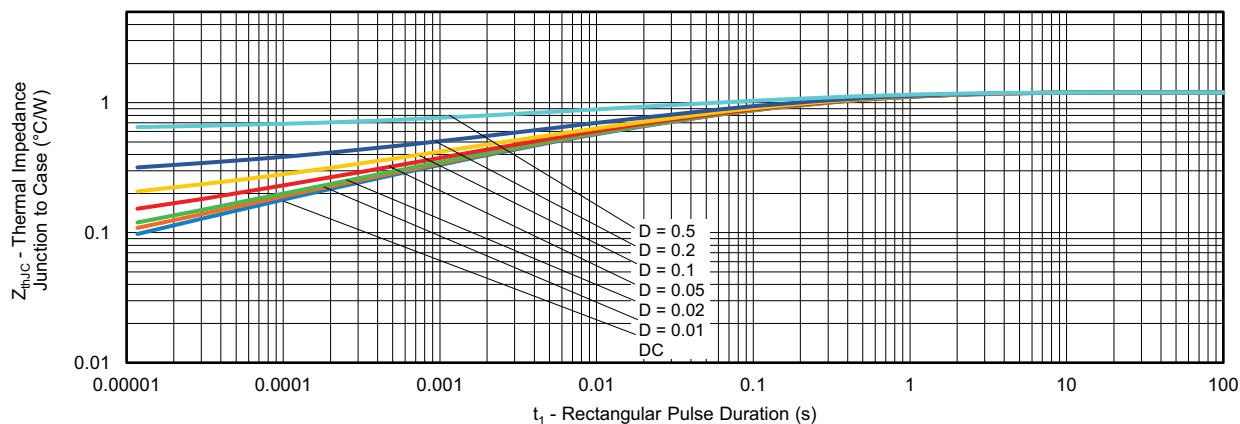
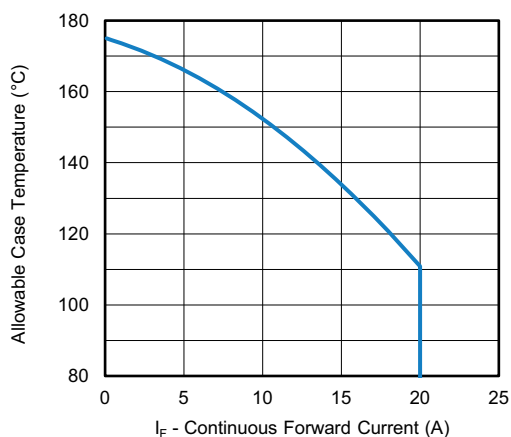

Fig. 5 - Typical Thermal Impedance Z_{thJC} Characteristics


Fig. 6 - Maximum Allowable Case Temperature vs. Average Forward Current

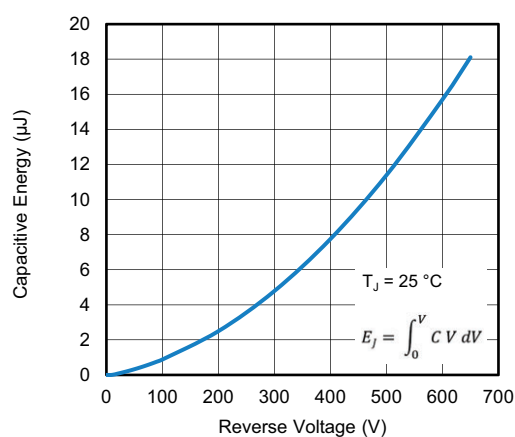


Fig. 8 - Typical Capacitive Energy vs. Reverse Voltage

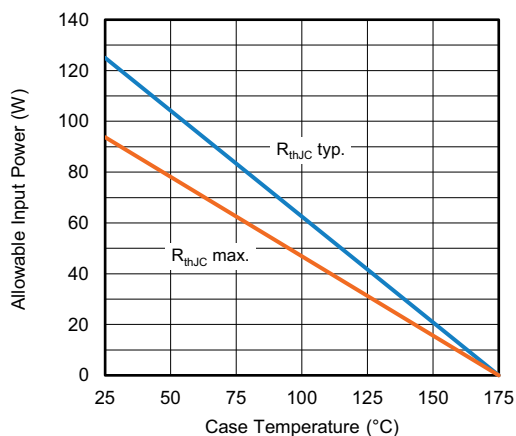


Fig. 7 - Forward Power Loss Characteristics

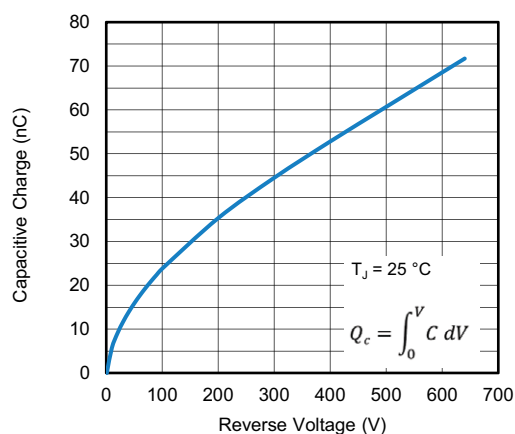


Fig. 9 - Typical Capacitive Charge vs. Reverse Voltage

**ORDERING INFORMATION TABLE**

Device code	VS-	3C	20	E	T	07	S	2	L	-M3
	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
1	- Vishay Semiconductors product									
2	- 3C = SiC diode, generation 3									
3	- Current rating (20 = 20 A)									
4	- E = single diode									
5	- T = D ² PAK package									
6	- Voltage rating: (07 = 650 V)									
7	- S = surface mountable									
8	- 2 = true 2 pin D ² PAK									
9	- L = tape and reel (left oriented)									
10	- Environmental digit: -M3 = halogen-free, RoHS-compliant, and termination lead (Pb)-free									

ORDERING INFORMATION

PREFERRED P/N	BASE QUANTITY	PACKAGING DESCRIPTION
VS-3C20ET07S2L-M3	800 per reel	13" diameter reel

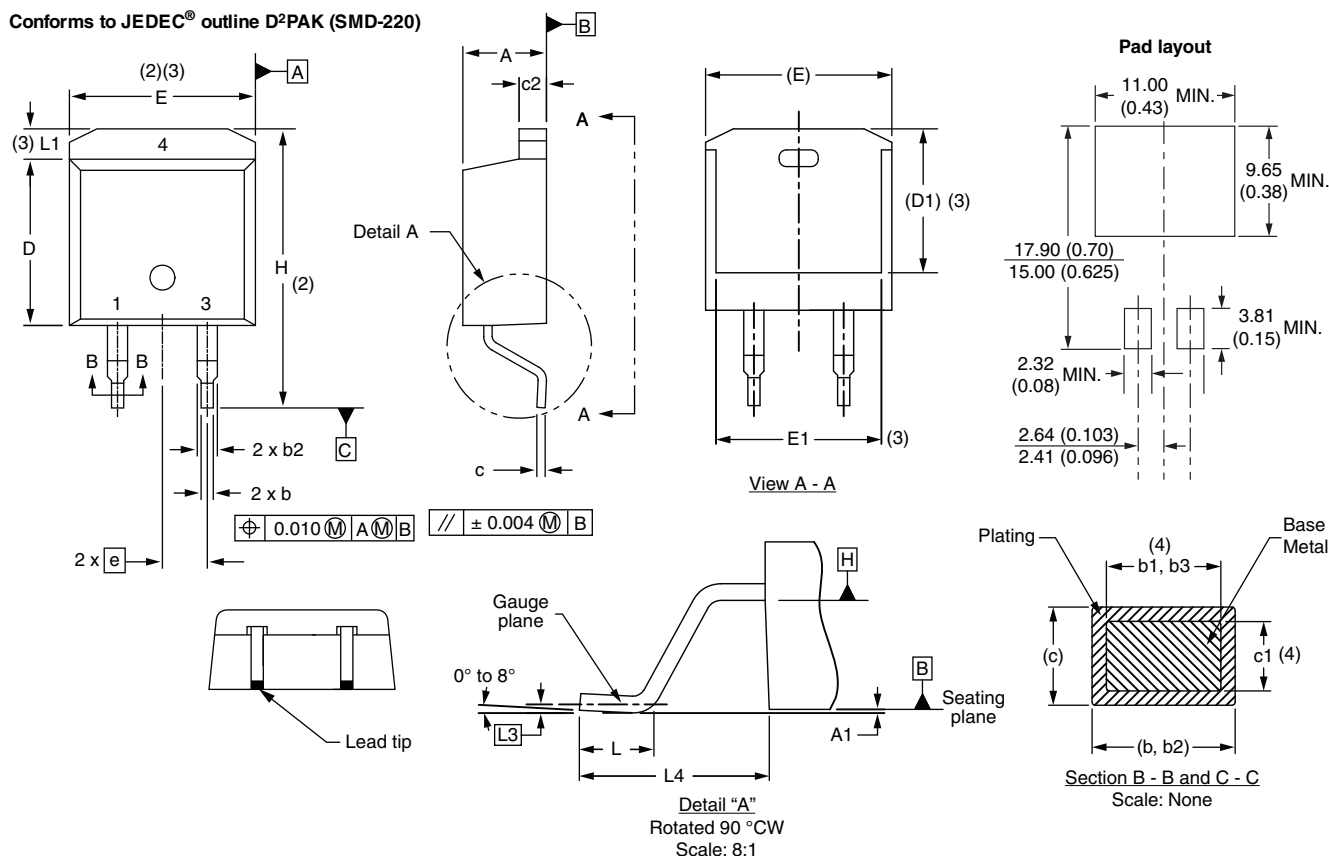
LINKS TO RELATED DOCUMENTS

Dimensions	www.vishay.com/doc?96683
Part marking information	www.vishay.com/doc?96693
Packaging information	www.vishay.com/doc?95032

D²PAK 2L (TO-263AB 2L)

DIMENSIONS in millimeters and inches

Conforms to JEDEC® outline D²PAK (SMD-220)



SYMBOL	MILLIMETERS		INCHES		NOTES	SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190		D1	6.86	8.00	0.270	0.315	3
A1	0.00	0.254	0.000	0.010		E	9.65	10.67	0.380	0.420	2, 3
b	0.51	0.99	0.020	0.039		E1	7.90	8.80	0.311	0.346	3
b1	0.51	0.89	0.020	0.035	4	e	2.54 BSC		0.100 BSC		
b2	1.14	1.78	0.045	0.070		H	14.61	15.88	0.575	0.625	
b3	1.14	1.73	0.045	0.068	4	L	1.78	2.79	0.070	0.110	
c	0.38	0.74	0.015	0.029		L1	-	1.65	-	0.066	3
c1	0.38	0.58	0.015	0.023	4	L3	0.25 BSC		0.010 BSC		
c2	1.14	1.65	0.045	0.065		L4	4.78	5.28	0.188	0.208	
D	8.51	9.65	0.335	0.380	2						

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5 M-1994
- (2) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body
- (3) Thermal pad contour optional within dimension E, L1, D1 and E1
- (4) Dimension b1 and c1 apply to base metal only
- (5) Datum A and B to be determined at datum plane H
- (6) Controlling dimension: inch
- (7) Outline conforms to JEDEC® outline TO-263AB



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