EZ-PD™ CCG8 USB Type-C port controller

General description

EZ-PD™ CCG8 is a dual-port USB Type-C controller that complies with the latest USB Type-C and Power Delivery (PD) specifications. CCG8 provides a complete USB Type-C and USB PD port control solution for PCs and notebooks. It includes a discrete N-channel field effect transistor (NFET) gate driver with fault protection and slew rate. It also contains a 32-bit, 48-MHz Arm® Cortex®-M0+ processor integrating a complete Type-C transceiver including the Type-C termination resistors Rp, Rd, and dead battery Rd termination. CCG8S (single port) is available in a 48-pin QFN package,whileCCG8D (dual-port) is available in 97-BGA package. Both CCG8S and CCG8D support Extended Power Range (EPR) upto 28 V without the need of any external components.

Applications

- Notebooks and desktops
- Thunderbolt hosts, non-Thunderbolt hosts

Features

- USB PD
  - Supports latest USB PD 3.1 specification (supports up to 28 V EPR)
  - Fast Role Swap (FRS)[1]
  - Extended data messaging
- **Type-C**
  - Integrated current sources for Downstream Facing Port (DFP)[2] role (Rp)
    - Default current at 900 mA
    - 1.5 A
    - 3 A
  - Integrated Rd resistor for Upstream Facing Port (UFP)[3] role
  - Integrated VCONN FETs to power EMCA cables
  - Integrated dead battery termination
- **Mux**
  - Integrated 3:1 SBU Muxes for alternate modes and closed chassis debug
- **Integrated load switch controller**
  - Integrated load switch controller for driving NFETs on VBUS provider path
  - Slew rate controlled turn-on of the VBUS provider path
  - Configurable hardware-controlled VBUS overvoltage, undervoltage, overcurrent, short-circuit, reverse current protection, and thermal shutdown
  - VBUS high-side current sense amplifier capable of measuring current across 5-mΩ series resistance on the provider path
- **LDO**
  - Integrated high-voltage LDO operational up to 28 V for dead battery mode operation
- **Integrated digital blocks**
  - Four TCPWMs that are configurable as timers, counters or PWMs to meet response times required by the USB PD protocol
  - Four run-time serial communication blocks (SCBs) that can be configured as either I^2C, SPI, or UART peripherals

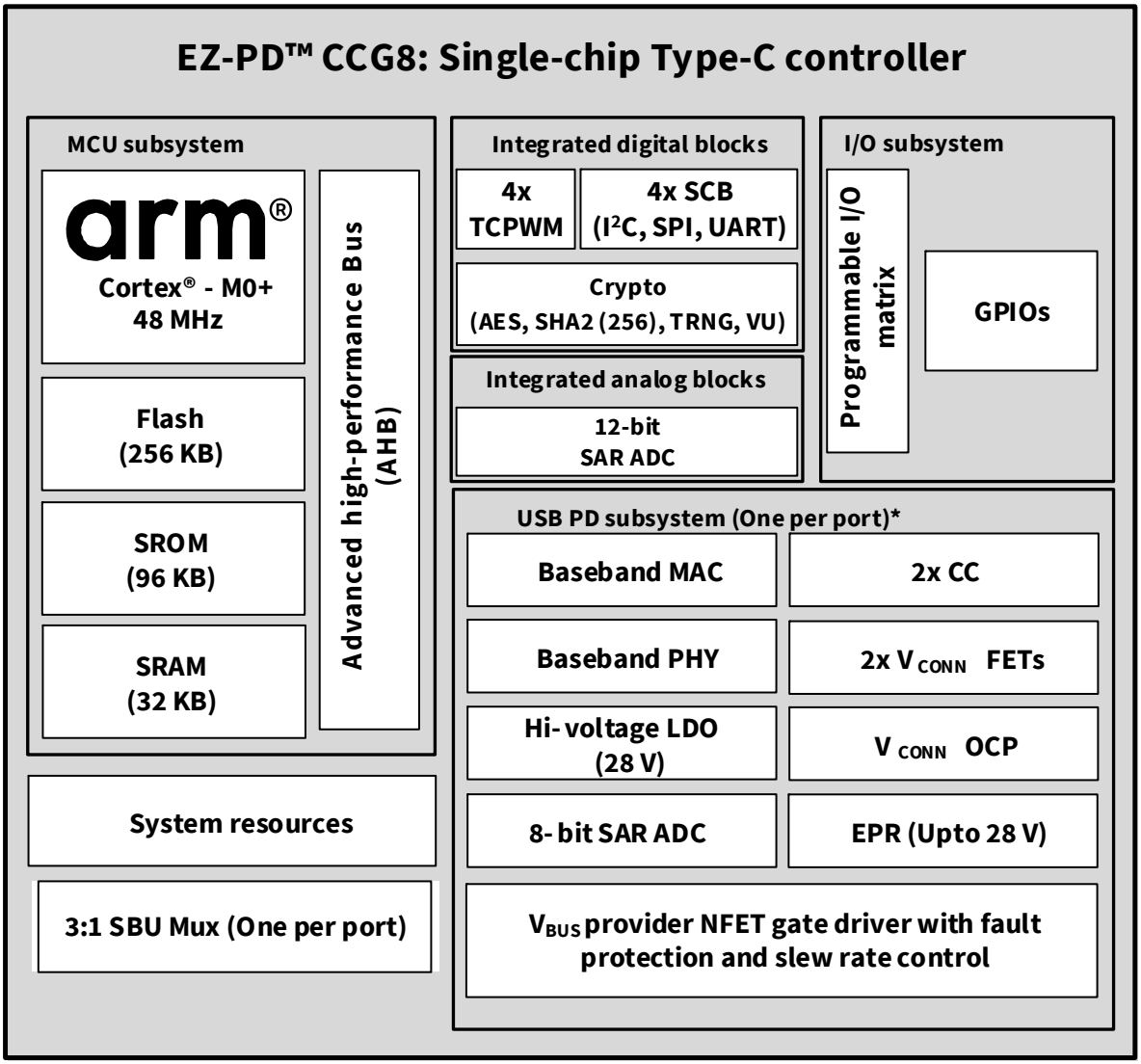
Notes

1. EZ-PD™ CCG8 requires an external load switch supporting FRS on the provider path to meet the FRS timings as per the PD specification.
2. DFP refers to power source.
3. UFP refers to power sink.

Features

- **Authentication**
  - True Random Number Generator (TRNG)
    - Vector Unit (VU)
- **Clocks and oscillators**
  - Integrated oscillator eliminating the need for an external clock
- **Operating range**
  - VSYS (2.8 V–5.5 V)
  - VBUS (4 V–28 V)
- **Packages**
  - CCG8D: 97-ball BGA
  - CCG8S: 48-pin QFN

Logic block diagram



* Only one USB PD subsystem exists for EZ-PD™ CCG8S because it has only one Type-C port available.

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1 Development support

EZ-PD™ CCG8 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit **www.infineon.com/cms/en/product/universal-serial-bus-usb-power-delivery-controller/usb-c-and-power-delivery** to find out more.

1.1 Documentation

A suite of documentation supports EZ-PD™ CCG8 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

ModusToolbox™ user guide: A step-by-step guide for using ModusToolbox™ (MTB) software. The software user guide shows you how ModusToolbox™ build process works in detail, how to use source control with ModusToolbox™, and much more.

Component datasheets: The flexibility of CCG8 allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all the information needed to select and use a particular component, including functional description, API documentation, example codes, and AC/DC specifications.

Application notes: This includes the Getting started application note and the hardware design guidelines.

Technical reference manual: The technical reference manual (TRM) contains all the technical detail you need to use a EZ-PD™ CCG8 device, including a complete description of all EZ-PD™ CCG8 registers. The TRM is available in the Documentation section at **www.infineon.com/cms/en/product/universal-serial-bus-usb-power-delivery-controller/usb-c-and-power-delivery**.

1.2 Infineon Developer Community

In addition to print documentation, the **EZ-PD™ CCG8 forums** connect you with fellow users and experts in CCG8 from around the world, 24 hours a day, 7 days a week.

1.3 Tools

With the industry standard cores, programming, and debugging interfaces, EZ-PD™ CCG8 family is part of a development tool ecosystem.

Visit us at **https://www.infineon.com/products/modustoolbox-software-environment** for the latest information , easy to use Eclipse IDE for ModusToolbox™, supported third party compilers, programmers, debuggers, and development kits.

1.4 Eclipse IDE for ModusToolbox™ and the EZ-PD™ CCG8 SDK

ModusToolbox™ is an Eclipse-based development environment on Windows, macOS, and Linux platforms that includes the Eclipse IDE for ModusToolbox™ and EZ-PD™ CCG8 SDK. The IDE brings together several device resources, middleware, and firmware to build an application. Using ModusToolbox™, you can enable and configure device resources and middleware libraries, write C/C++/assembly source code, and program and debug the device.

EZ-PD™ CCG8 SDK is the software development kit. The SDK makes it easier to develop firmware for supported devices without the need to understand the intricacies of the device resources.

For additional details on using the ModusToolbox™ software, seethe **Modus Toolbox™ software user guide** and the documentation and help integrated into the ModusToolbox™ software. As **Figure 1** shows, with the Eclipse IDE for ModusToolbox™ , you can:

1. Create a new application based on a list of template applications, filtered by kit or device, or browse the collection of code examples online.
2. Configure device resources in the Device configurator to build your hardware system design in the workspace.
3. Add software components or middleware.
4. Develop your application firmware.

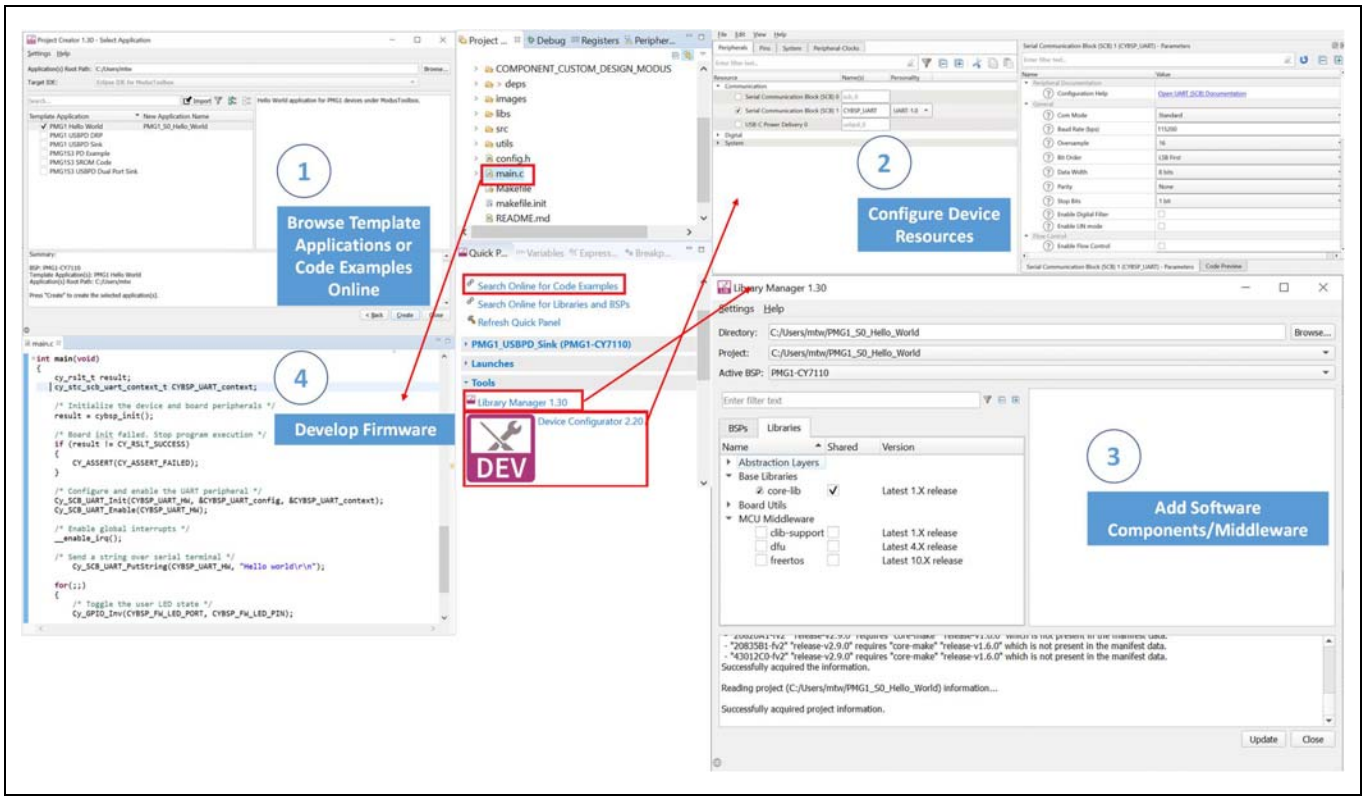


Figure 1 ModusToolbox™ IDE resources and middleware

2 Functional overview

2.1 CPU and memory subsystem

2.1.1 CPU

The Cortex®-M0+ in EZ-PD™ CCG8 is a 32-bit MCU which is optimized for low-power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. The implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a wakeup interrupt controller (WIC). The WIC can wake the processor up from the deep sleep mode, allowing power to be switched off to the main processor when the chip is in the deep sleep mode.

The CPU subsystem also includes a 16-channel DMA/Datawire block and a Serial Wire Debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for CCG8 has four break-point (address) comparators and two watchpoint (data) comparators.

2.1.2 Flash

CCG8 has a 256 KB flash module.

2.1.3 SRAM

32 KB of SRAM which is retained during deep sleep is provided.

2.1.4 ROM

96 KB of supervisory ROM that contains boot and configuration routines is provided. In addition to the flash erase and program routines provided for CCG8, the SROM also contains flash checksum routines.

2.1.5 Cryptographic accelerator

The crypto accelerator block supports below requirements:

- Vector Unit (VU) to support asymmetric key cryptography.
- SHA2 (256-bit)
- Vector unit for asymmetric cryptography capable of performing RSA-4096, 3072, ECC-256
- AES (128-bit) supports forward block cipher
- True Random Number Generator (AIS-31 compliant)
- Performance @ 48 MHz
  - RSA-3072 verify performance: 25 ms
  - SHA-2 256-bit over 64 KB: 10 ms
  - Secure boot transfer control to user program in 50 ms
- Public-key storage
  - Flash: 2 KB RSA-3072 key structure stored in flash. The key structure includes modulus, exponent and three coefficients

2.2 System resources

2.2.1 Power system

The power system is described in detail in **"Power systems overview"** on page 15. It provides assurance that voltage levels are as required for each respective mode and will either delay mode entry (on power-on reset (POR) for instance) until voltage levels are as required for proper function or will generate resets (brown-out detection (BOD)) if operation under unsafe power supply levels is imminent. CCG8 can operate with a single external supply over the range of 2.8 V to 5.5 V (VSYS) or 4 V to 28 V (VBUS) and has three different power modes (active, sleep, deep sleep), transitions between which are managed by the power system.

When operating on a 28-V regulator, depending on the package and VBUS supply value, ensure that you limit the current consumption (by turning off peripherals) and ensure that the die T_{JA} does not exceed 125°C.

2.2.2 Clock system

The clock system for CCG8 is a strict subset of the M0S8 platform. CCG8 has a fully integrated clock and therefore does not require an external crystal. The clock system is responsible for providing clocks to all subsystems that require clocks (SCB, TCPWM, programmable analog subsystem (PASS) and PD) and for switching between different clock sources without glitches. In addition, it must ensure that no metastable conditions occur.

Figure 2 illustrates the CCG8 clock system which consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO). PERXYZ_CLK represents the clocks for different peripherals.

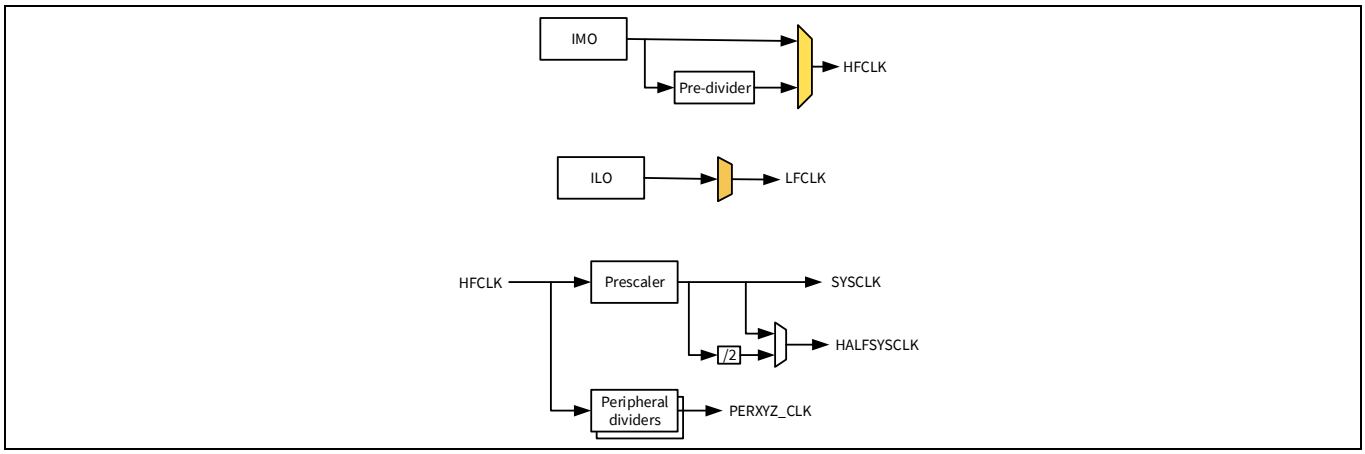


Figure 2 Clocking architecture of EZ-PD™ CCG8

The HFCLK signal can be divided down to generate synchronous clocks for the analog and digital peripherals. There are 21 clock dividers (5 with fractional divide and 16 with integer divide capability). The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The digital clock dividers generate enabled clocks (i.e., 1 in *N* clocking where 'N' is the divisor). The analog clock divider needs to provide a true 50% duty cycle to maintain analog performance at all allowed frequencies.

2.2.2.1 IMO clock source

The IMO is the primary source of internal clocking in CCG8. It is trimmed during production to achieve the desired accuracy of ±2%. Trim values are stored in supervisory rows in the flash memory. Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 48 MHz ±2%. The IMO RMS jitter allows 12-bit SAR accuracy.

2.2.2.2 ILO clock source

The ILO is a very-low-power, relatively inaccurate oscillator, which is primarily used to generate clocks for peripheral operation in USB Suspend (deep sleep) mode. It is a 32-kHz oscillator with untrimmed accuracy of -70 to +150% and it is capable of being trimmed within ±55%.

2.2.3 Watchdog timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during deep sleep and generates a watchdog reset if not serviced before the timeout occurs. The timer can be used to generate interrupts if required in addition to generating resets.

2.2.4 Reset

CCG8 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register which is sticky through reset and allows software to determine the cause of the reset. A pin (XRES) is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration.

2.2.5 Voltage reference

CCG8 reference system generates all internally required references. To allow better signal-to-noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the 12-bit SAR ADC. The internal reference at the pin may be buffered by using one of the on-chip opamps and used as an external reference.

2.3 Analog blocks

2.3.1 12-bit SAR ADC

The 12-bit 1-Msps SAR ADC operates at a maximum clock rate of 18 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion. The ADC clock input is derived by dividing the CPU clock rate by an integer value. This means that at the 48 MHz CPU clock rate, the highest allowable clock rate for the ADC is 16 MHz. The 16 MHz clock rate allows 10-bit conversions to be performed at 1 Msps (a 10-bit conversion takes a minimum of 16 clocks). Using integer dividers also means that 12-bit ADC performance is 890 samples/second at 48 MHz and its peak of 1 Msps is at 18 or 36 MHz. The ADC requires an approximately 50% duty cycle clock and this is provided for all integer divider values.

The block functionality is augmented for the user by adding a reference buffer to it and by providing the choice of three internal voltage references: VDDA, VDDA/2, and Vref (nominally 1.2 V) as well as an external reference through a GPIO pin. The sample-and-hold (S/H) aperture is programmable allowing the gain-bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed allowing less expensive external opamps to be used. The system performance is 68 dB for true 12-bit precision, if appropriate references are used. In particular, it is possible to provide an external bypass (via a fixed pin location) for the internal reference amplifier.

The SAR ADC is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (i.e., aggregate sampling bandwidth is equal to 1 Msps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. In order to accommodate signals with varying source impedance and frequency it is possible to have different sample times programmable on a per-channel basis. Also, signal range specification via a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SARADC includes multiple sample averaging capability in order to save CPU bandwidth. It digitizes the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SARADC is not available in deep sleep mode as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 to 5.5 V.

2.3.2 Temperature sensor

CCG8 has an on-chip temperature sensor which consists of a diode biased by a current source that can be disabled to save power. The diode is calibrated during production to achieve ±5% maximum deviation from accuracy (typical ±1%). Because the measured temperature is the on-chip temperature of the diode, the diode is placed in close proximity to the SAR ADC to allow more accurate measurement.

2.4 USB PD subsystem

This subsystem provides the interface to the Type-C USB port.

2.4.1 USB PD physical layer

The USB PD subsystem contains the USB PD physical layer block and supporting circuits. The physical layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC as per the PD 3.1 standard All communication is half-duplex. The physical layer or PHY practices collision avoidance to minimize communication errors on the channel.

2.4.2 VCONN FET

CCG8 has two integrated VCONN FETs to power either CC1 or CC2 pins. There is a power supply input V5V pin for providing power to EMCA cables through these VCONN FETs. These FETs can provide 1.5-W power per port over the valid VCONN range of 4.85 V to 5.5 V on the CC1/2 pins for EMCA cables. At any given time, only one of the VCONN FETs is ON.

2.4.3 ADC

The ADC is a low-footprint 8-bit SAR ADC available for general purpose A/D conversion applications in the chip. The ADC can be accessed from the GPIOs through an on-chip analog mux. In CCG8, one ADC is instantiated per PD port.

2.4.4 SBU mux

CCG8 contains a set of analog switches to connect SBU1 and SBU2 pins of the Type-C connector to AUX of a DisplayPort or LSx of Thunderbolt and UART debug pins. AUX pins are provided with switchable pull-up and pull-down resistors as required by their respective specs as shown in **Figure 3**. The LSTX/RX, debug ports are muxed digitally and no analog mux is required for these inputs.

The dual-port (CCG8D) has two 3:1 SBU MUXes and the single port (CCG8S) has one 3:1 SBU MUX integrated in it.

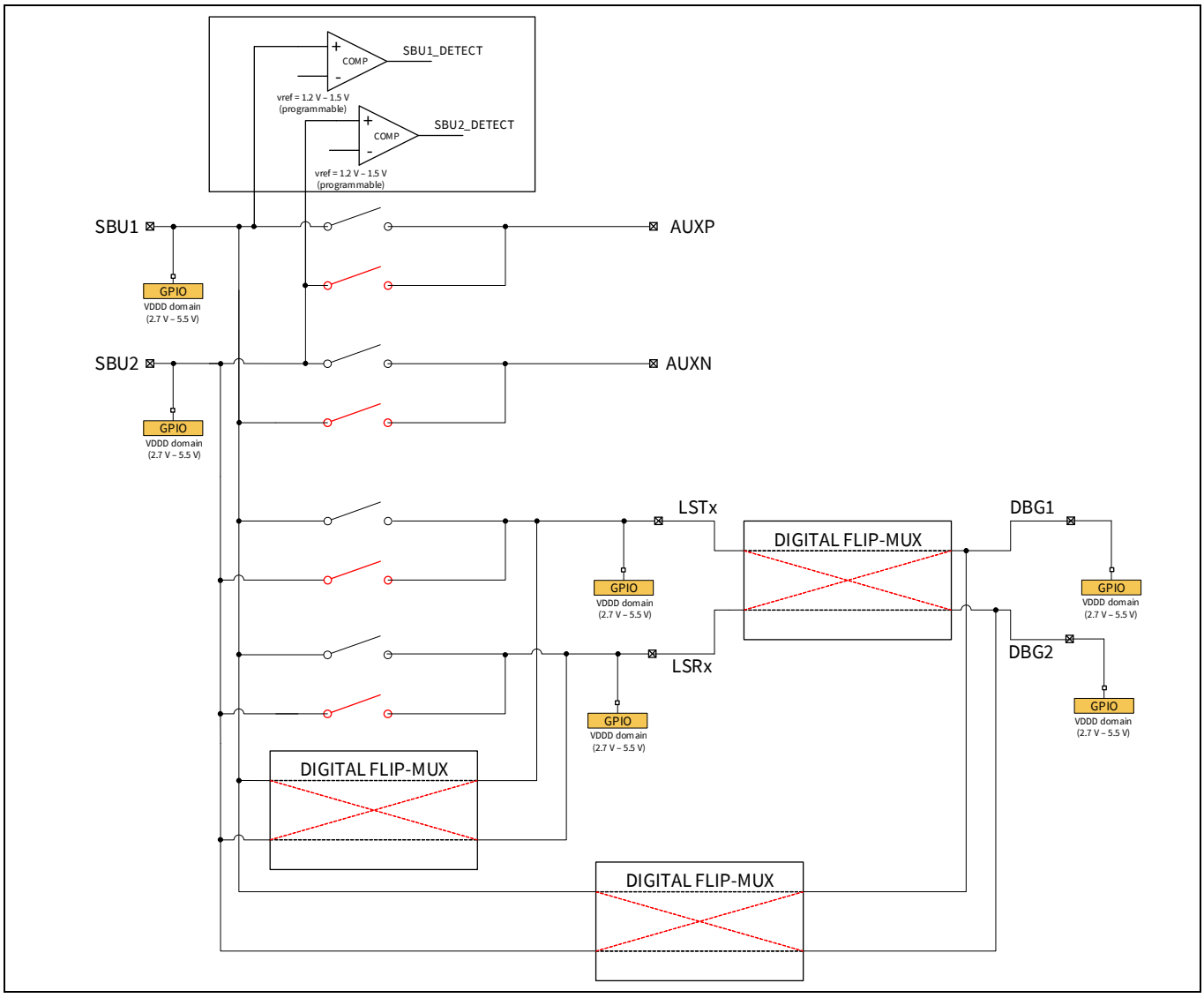


Figure 3 SBU Mux

2.4.5 Load switch controller

CCG8 has an integrated load switch controller with the following functions. The load switch controller can support up to 28 V on the provider path.

2.4.5.1 Overvoltage and undervoltage protection on VBUS

The chip implements an undervoltage/overvoltage (UVOV) detection circuit for the VBUS supply. The thresholds for both UV and OV are programmable.

2.4.5.2 Over current, short-circuit current, and reverse current fault detection comparators for VBUS

The chip supports the detection of over current, short-circuit current and reverse current faults in the VBUS provider path. The external resistor (5 mΩ) placed in the connector VBUS path connects to the chip; the drop across this resistor is monitored to detect these faults. CCG8 restricts reverse current to 400 mA on the VBUS provider path when Type-C VBUS is greater than VIN (provider voltage before the VBUS NFET). CCG8 reacts quickly and turns off the VBUS provider NFET. This feature is not supported on the consumer path and there will be reverse current whenever the consumer side voltage is higher than connector side voltage on the consumer path.

2.4.5.3 VBUS discharge

CCG8 has an integrated high-voltage (28 V) VBUS discharge circuitry. After cable removal detection, the chip will discharge the residual charge and bring the floating VBUS back to vSafe0V.

2.4.5.4 VBUS regulator

The chip has up to three input power supplies – VSYS and VBUS_C (Port0 and Port1). A regulator operating on these power supplies will derive the chip operating supply. The VSYS always takes priority over VBUS. In the absence of VSYS, the regulator powers the chip from VBUS (Port0 or Port1 whichever is present).

2.4.5.5 Gate drivers for VBUS NFETs

CCG8 has two integrated gate drivers to drive external NFETs on the provider path, one per port. These gate drivers support only external NFET; these NFETs must be capable of supporting max VGS of ±VBUS_NGDO_MAX. These gate drivers do not meet the Fast Role Swap (FRS) timings per the PD spec, hence an external load switch is recommended for applications require FRS support.

On the source path, the back-to-back NFETs must be configured only in common drain mode.

The consumer path external FETs will be controlled by a GPIO pin.

Figure 4 and **Figure 5** show how the gate drivers can be configured in different scenarios.

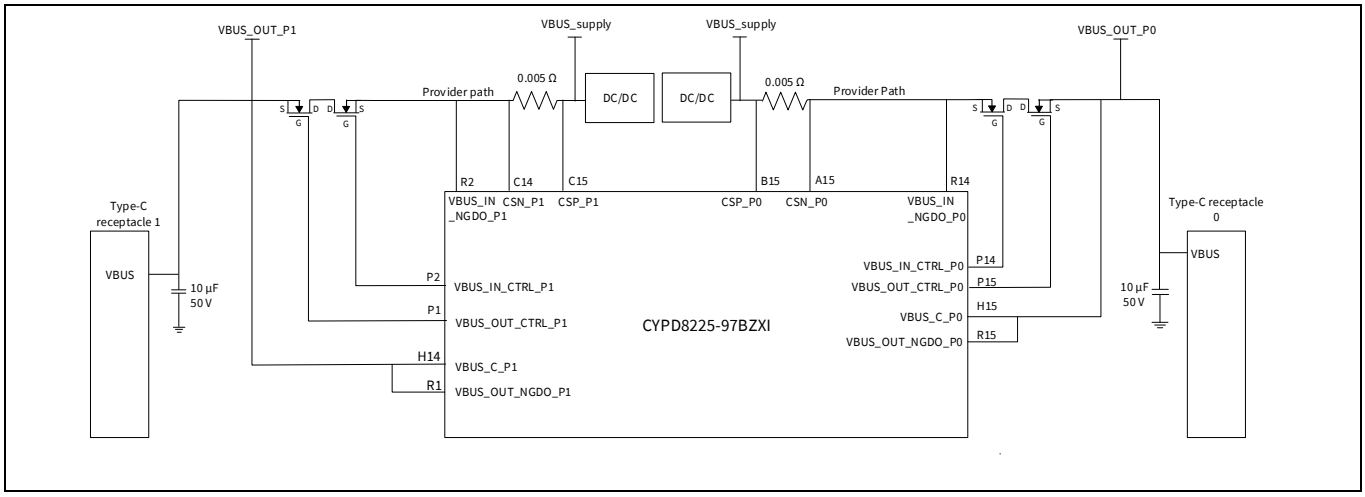


Figure 4 Source configuration on both Type-C ports using 97-BGA

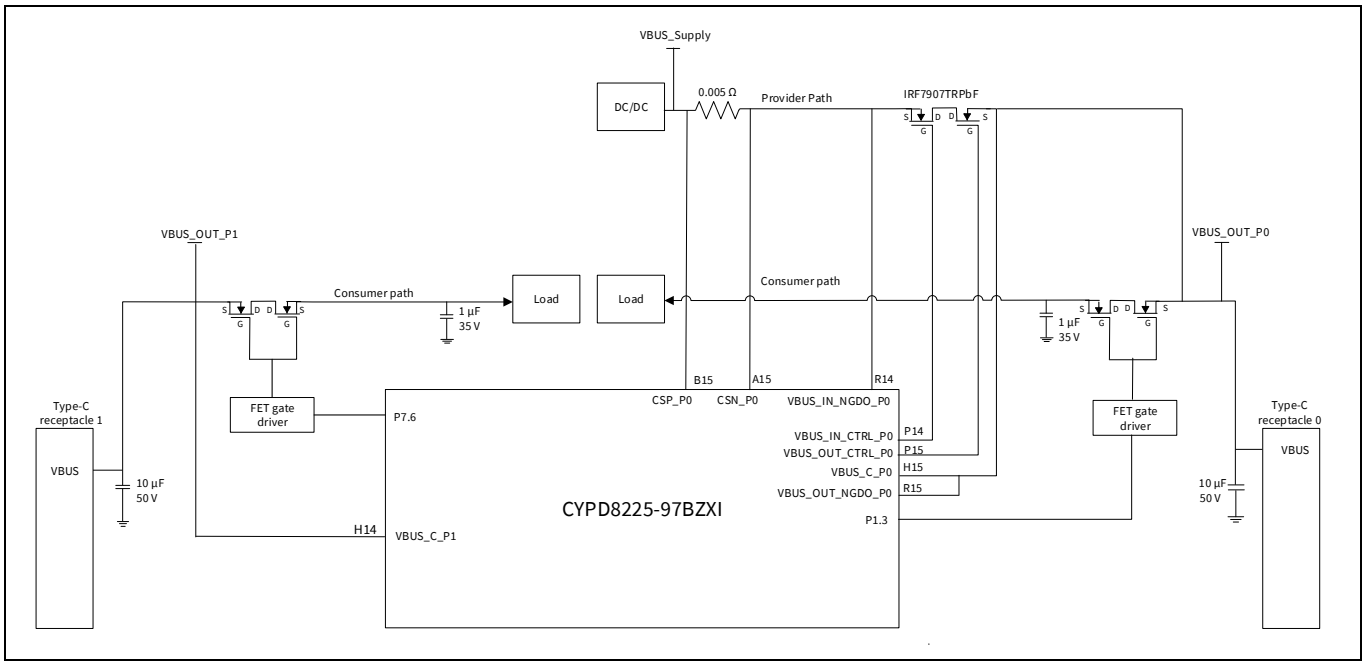


Figure 5 DRP on one Type-C port and sink on the second Type-C port using 97-BGA

In **Figure 5**, Port 0 is configured as a DRP; CCG8 gate driver pins are used to control the provider path and a GPIO pin is used to control the consumer path FETs.

2.5 Fixed-function digital

2.5.1 Timer/counter/PWM block

The timer/counter/PWM block consists of a 16-bit counter with user-programmable period length. There is a capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as dead-band programmable complementary PWM outputs. It also has a “kill” input to force outputs to a pre-determined state; this is used in motor drive systems for instance when an over-current state is indicated and the PWMs driving the FETs need to be shut-off immediately with no time for software intervention.

CCG8 has up to four TCPWMs. They can be used as internal timers by firmware or for providing PWM-based functions on the GPIOs.

2.5.2 SCB

CCG8 has four SCB blocks that can be configured for I2C, SPI, or UART. These blocks implement full multi-master and slave I2C interfaces capable of multi-master arbitration. I2C is compatible with the standard NXP I2C specification v3.0. These blocks operate at speeds of up to 1 Mbps and have flexible buffering options to reduce the interrupt overhead and latency for the CPU.

The SCB blocks support 8-deep FIFOs for receive (RX) and transmit (TX), which, by increasing the time given for the CPU to the read data, greatly reduces the need for clock stretching caused by the CPU not having read the data on time. The FIFO mode is useful in the absence of the DMA. Data throughput is not a critical consideration for I2C. The I2C port I/Os for SCB0 are overvoltage-tolerant (OVT). The I2C port for SCB1-7 are not OVT compliant.

UART mode: This is a full-feature UART operating at up to 1 Mbps. In addition, it supports the 9-bit multi-processor mode which allows address of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported.

SPI mode: The SPI mode supports full Motorola SPI as well as TI SSP (essentially adds a start pulse used to synchronize SPI codecs), and National Microwire (half-duplex form of SPI) variants. The SPI block can also utilize the FIFO.

2.5.3 GPIO interface

CCG8 has up to 50 GPIOs in 97-BGA package and 26 GPIOs in 48-QFN package including the SCB and SWD pins which can also be used as GPIOs.

The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled.
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables.
- Hold mode for latching previous state (used for retaining I/O state in deep sleep mode).
- Selectable slew rates for dV/dt related noise control.

The pins are organized in logical entities called “ports”, which are 8-bit in width. During the power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix (HSIOM) is used to multiplex between various signals that may connect to an I/O pin. The pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity. Data output registers and pin state registers store, respectively, the values to be driven on the pins and the states of the pins. The configuration of the pins can be done by programming of registers through software for each digital I/O port.

Every I/O pin can generate an edge-triggered interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it.

The I/O ports can retain their state during the deep sleep mode or remain ON. If operation is restored using reset, then the pins go the High-Z state. If operation is restored by an interrupt event, the pin drivers retain their state until firmware chooses to change it. The I/Os (on the data bus) do not draw current on power down.

2.5.3.1 GPIO power domain

All the GPIOs reside in a separate I/O power domain called VDDIO (with exception of SBU GPIO). The separate I/O power domain provides flexible system-level interfacing. GPIOs connected to SBU (connector side) are on the VDDD domain and not on the VDDIO domain.

For all 50 GPIOs in 97-BGA, the voltages on AMUXBUSA and AMUXBUSB lines cannot be more than VDDA supply.

3 Power systems overview

Figure 6 illustrates the general requirements for power pins on EZ-PD™ CCG8. The power scheme allows different VDDD and VDDA connections. There are no sequencing requirements. The following diagram is intended to show that VDDD and VDDA are separate nets which are not ohmically connected on the chip. Depending on different package requirements, these may be connected together in the bonding arrangement or required to be connected off chip.

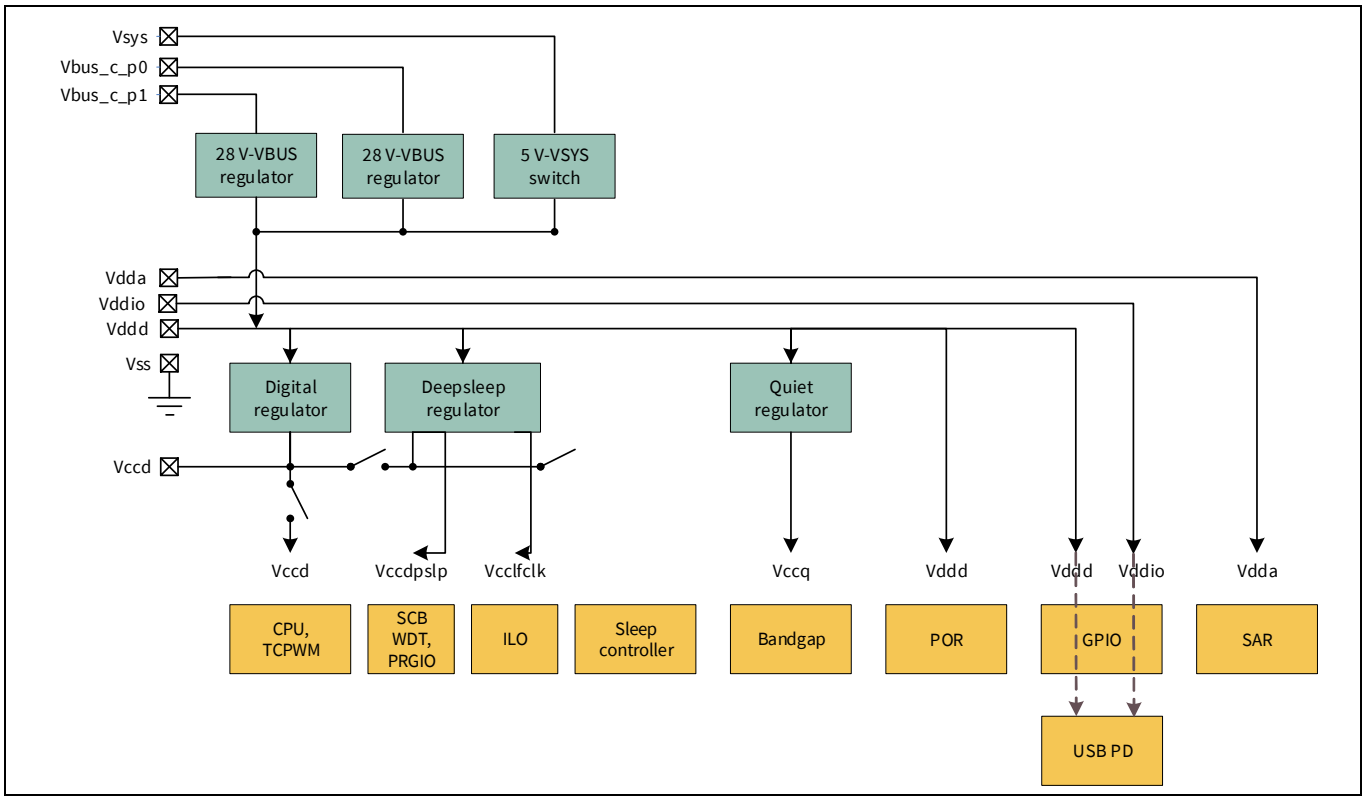


Figure 6 EZ-PD™ CCG8 power system block diagram

4 Pinouts

Table 1 Pinout for CYPD8225-97BZXI

Group name	Pin name	Port	97-BGA pinout	Pin description
VBUS OCP/SCP/ RCP	CSN_P0	Analog	A15	Current sense negative input for VBUS side external Rsense: Port-0
	CSN_P1		C14	Current sense negative input for VBUS side external Rsense: Port-1
	CSP_P1		C15	Current sense positive input for VBUS side external Rsense: Port-1
	CSP_P0		B15	Current sense positive input for VBUS side external Rsense: Port-0
Power	VSYS	Power	B14	2.8-V to 5.5-V supply for the system
	VDDIO		B8, H12	GPIO supply (1.71 V - 5.5 V). At system-level short the VDDD to VDDIO.
	VCCD		D10	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	VDDA		D6, F6	Programmable analog supply (2.7 V - 5.5 V). Shorted to VDDD at board level.
	VDDD		D8	VDDD supply output 1. VSYS powered: (Min: VSYS-100 mV) 2.7 V to 5.5 V 2. VBUS powered: 2.7 V to 3.6 V
	VBUS_C_P1		H14	Type-C VBUS connector input for Port-1 (4 V to 28 V)
	VBUS_C_P0		H15	Type-C VBUS connector input for Port-0 (4 V to 28 V)
	V5V_P1		L1, L2	4.85 V to 5.5 V supply for VCONN FET of Type-C: Port-1
	V5V_P0		L14, L15	4.85 V to 5.5 V supply for VCONN FET of Type-C: Port-0
USB Type-C	CC1_P1	Analog	N1, N2	USB PD Port-1 connector detect/configuration channel 1
	CC1_P0		N14, N15	USB PD Port-0 connector detect/configuration channel 1
	CC2_P1		J1, J2	USB PD Port-1 connector detect/configuration channel 2
	CC2_P0		J14, J15	USB PD Port-0 connector detect/configuration channel 2
Reset	XRES		E14	Reset input
Ground	VSS	Ground	F8, F10, F12, H8, H10, K8, K10	Ground
Muxes/ switches	DBG2_P1/P0.3[4]	GPIO	K6	Closed chassis debug2 pin for Port-1/GPIO
	AUX_P_P1[4]	Analog	M4	Type-C auxiliary signal for DisplayPort - system side: Port-1
	AUX_N_P1[4]		M6	
	DBG1_P0/P0.5[4]	GPIO	M8	Closed chassis debug1 pin for Port-0/GPIO

Note
4. I/O logic is connected to VDDD instead of VDDIO.

Table 1 Pinout for CYPD8225-97BZXI *(continued)*

Group name	Pin name	Port	97-BGA pinout	Pin description
Muxes/ switches	AUX_P_P0[4]	Analog	P11	Type-C auxiliary signal for DisplayPort - system side: Port-0
	SBU2_P0[4]		P13	Type-C auxiliary signal for DisplayPort - connector side: Port-0
	SBU2_P1[4]		P5	Type-C auxiliary signal for DisplayPort - connector side: Port-1
	DBG1_P1/P0.2[4]	GPIO	P7	Closed chasis debug1 pin for Port-1/GPIO
	DBG2_P0/P0.4[4]		P8	Closed chasis debug2 pin for Port-0/GPIO
	AUX_N_P0[4]	Analog	P9	Type-C auxiliary signal for DisplayPort - system side: Port-0
	LSRX_P0/P0.7[4]	GPIO	R11	LSRX for Port-0/GPIO
	SBU1_P0[4]	Analog	R13	Type-C auxiliary signal for DisplayPort - connector side: Port-0
	SBU1_P1[4]	Analog	R5	Type-C auxiliary signal for DisplayPort - connector side: Port-1
	LSTX_P1/P0.1[4]	GPIO	R7	LSTX for Port-1/GPIO
	LSRX_P1/P0.0[4]		R8	LSRX for Port-1/GPIO
	LSTX_P0/P0.6[4]		R9	LSTX for Port-0/GPIO
VBUS control	VBUS_OUT_CTRL_P1	Analog	P1	Full rail control I/O for enabling/disabling NFET (output side) of USB Type-C path-1
	VBUS_IN_CTRL_P0		P14	Full rail control I/O for enabling/disabling NFET (input-side) of USB Type-C path-0
	VBUS_OUT_CTRL_P0		P15	Full rail control I/O for enabling/disabling NFET (output side) of USB Type-C path-0
	VBUS_IN_CTRL_P1		P2	Full rail control I/O for enabling/disabling NFET (input-side) of USB Type-C path-1
	VBUS_IN_NGDO_P0		R14	VBUS input for the NGDO - path-0 (4 V to 30 V)
	VBUS_IN_NGDO_P1		R2	VBUS input for the NGDO - path-1 (4 V to 30 V)
	VBUS_OUT_NGDO_P0		R15	VBUS output for the NGDO - path-0 (4 V to 30 V)
	VBUS_OUT_NGDO_P1		R1	VBUS output for the NGDO - path-1 (4 V to 30 V)
GPIO	P3.0	GPIO	A1	TCPWM/GPIO
	P7.2		A14	GPIO
	P2.0		A2	
	RETIMER_RESET_N_P0/P2.2		A3	Retimer Reset_N for Port-0/GPIO
	P2.5		A5	GPIO
	P2.4		A7	TCPWM/GPIO
	P2.7		A8	GPIO
	P7.5		A9	
	P3.3		B1	TCPWM/GPIO
	RETIMER_RESET_N_P1/P7.4		B11	Retimer Reset_N for Port-1/GPIO
	RETIMER_PWR_EN_P1/P7.3		B13	Retimer power enable for Port-1/GPIO
	P2.1		B2	TCPWM/GPIO
	P3.1		B3	GPIO

Note
4. I/O logic is connected to VDDD instead of VDDIO.

Table 1 Pinout for CYPD8225-97BZXI *(continued)*

Group name	Pin name	Port	97-BGA pinout	Pin description
	RETIMER_PWR_EN_P0/P2.3		B5	Retimer power enable for Port-0/GPIO
	P2.6		B7	GPIO
	VBUS_C_CRTL_P1/P7.6		B9	Consumer path external FET control for Port-1/GPIO
	P3.7		C1	GPIO
GPIO	I2C_SDA_SCB0 /P4.1	GPIO	D12	SCB0 data for configuring retimer or DP/USB multi-function MUX/GPIO
	I2C_SCL_SCB0 /P4.0		E15	SCB0 clock for configuring retimer or DP/USB multi-function MUX/GPIO
	P3.4		D4	GPIO
	I2C_SDA_SCB2 /P5.1		E1	SCB2 data for communicating with SoC or TBT controller/GPIO
	I2C_SCL_SCB2 /P5.0		G2	SCB2 clock for communicating with SoC or TBT controller/GPIO
	I2C_SDA_SCB4 /P3.6		E2	SCB4 data for communicating with embedded controller/GPIO
	I2C_SCL_SCB4 /P3.5		F4	SCB4 clock for communicating with embedded controller/GPIO
	I2C_SDA_SCB1 /P1.5		M12	SCB1 data/GPIO
	I2C_SCL_SCB1 /P1.6		K12	SCB1 clock/GPIO
	VBUS_C_CTRL_P0/P1.3		K4	Consumer path external FET control for Port-0/GPIO
	P1.0		H2	GPIO
	I2C_INT_EC/ P5.5		H4	Embedded controller interrupt/GPIO
	P5.2		H6	GPIO
	HPD_P0/P1.4		M10	Hot plug detect I/O for Port-0/GPIO
	P3.2		C2	GPIO
	I2C_INT_ TBT_P1/P5.4		G1	Thunderbolt interrupt for Port-1/GPIO
	HPD_P1/P7.1		G14	Hot plug detect I/O for Port-1/GPIO
	P7.0		G15	GPIO
	I2C_INT_ TBT_P0/P5.3		H1	Thunderbolt interrupt for Port-0/GPIO
	SWD_CLK/I2C_CFG_EC/P1.1		P3	Serial Wire Debug clock/EC I2C config/GPIO
	SWD_IO/P1.2		R3	Serial Wire Debug data/GPIO

Note
4. I/O logic is connected to VDDD instead of VDDIO.

Table 2 Pinout for CYPD8125-48LDXI

Group name	Pin name	Port	48-QFN pinout	Pin description
VBUS OCP/SCP/RCP	CSN	Analog	37	Current sense negative input for VBUS side external Rsense
	CSP		38	Current sense positive input for VBUS side external Rsense
Power	VSYS	Power	36	2.8-V to 5.5-V supply for the system
	VDDIO		23,42	GPIO supply (1.71 V to 5.5 V). At system-level, short the VDDD to VDDIO.
	VCCD		41	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	VDDA		5	Programmable analog supply (2.7 V to 5.5 V). Shorted to VDDD at board level.
	VDDD		43	VDDD supply output 1. VSYS powered: (Min: VSYS-100 mV) 2.7 V to 5.5 V 2. VBUS powered: 2.7 V to 3.6 V
	VBUS_C		31	Type-C VBUS connector input (4 V to 28 V)
	V5V		29	4.85 V to 5.5 V supply for VCONN FET of Type-C
	CC1	Analog	28	USB PD connector detect/Configuration Channel 1
	CC2		30	USB PD connector detect/Configuration Channel 2
Reset	XRES		33	Reset input
Ground	VSS	Ground	6,32,44	Ground
Muxes/Switches	DBG2/P0.3[5]	GPIO	22	Closed Chassis Debug2 Pin/GPIO
	AUX_P[5]	Analog	15	Type-C auxiliary signal for DisplayPort - system side
	AUX_N[5]		16	
	SBU2[5]		18	Type-C auxiliary signal for DisplayPort - connector side
	DBG1/P0.2[5]	GPIO	21	Closed Chassis Debug1 Pin/GPIO
	SBU1[5]	Analog	17	Type-C auxiliary signal for DisplayPort - connector side
	LSTX/P0.1[5]	GPIO	20	LSTX/GPIO
	LSRX/P0.0[5]		19	LSRX/GPIO
VBUS Control	VBUS_IN_CTRL	Analog	27	Full rail control I/O for enabling/disabling NFET (input-side) of USB Type-C
	VBUS_OUT_CTRL		26	Full rail control I/O for enabling/disabling NFET (output side) of USB Type-C
	VBUS_IN_NGDO		24	VBUS input for the NGDO (4 V to 30 V)
	VBUS_OUT_NGDO		25	VBUS output for the NGDO (4 V to 30 V)
GPIO	P3.0	GPIO	1	TCPWM/GPIO
	RETIMER_RESET_N/P2.2		47	Retimer Reset_N/GPIO
	P2.4		45	TCPWM/GPIO/Hot Plug Detect I/O
	P3.3		2	Consumer path external FET control/GPIO
	P7.4		40	GPIO
	P7.3		39	
	P2.1		48	TCPWM/GPIO

Note
5. I/O logic is connected to VDDD instead of VDDIO.

Table 2 Pinout for CYPD8125-48LDXI *(continued)*

Group name	Pin name	Port	48-QFN pinout	Pin description
GPIO	RETIMER_PWR_EN/ P2.3	GPIO	46	Retimer power enable/GPIO
	I2C_SDA_SCB0/P4.1		35	SCB0 data for configuring re-timer or DP/USB Multi-function MUX/GPIO
	I2C_SCL_SCB0/P4.0		34	SCB0 clock for configuring re-timer or DP/USB Multi-function MUX/GPIO
	I2C_SDA_SCB2/P5.1		8	SCB2 data for communicating with SoC or TBT controller/GPIO
	I2C_SCL_SCB2/P5.0		7	
	I2C_SDA_SCB4/P3.6		4	SCB4 data for communicating with embedded controller/GPIO
	I2C_SCL_SCB4/P3.5		3	SCB4 clock for communicating with embedded controller/GPIO
	VBUS_C_CTRL/P1.3		14	TCPWM/GPIO
	I2C_INT_EC/P5.5		11	Embedded controller Interrupt/GPIO
	P5.2		9	GPIO
	I2C_INT_TBT/P5.3		10	Thunderbolt interrupt/GPIO
	SWD_CLK/I2C_CFG_ EC/P1.1		12	Serial Wire Debug clock/EC I2C config/GPIO
	SWD_IO/P1.2		13	Serial Wire Debug data/GPIO

Note
5. I/O logic is connected to VDDD instead of VDDIO.

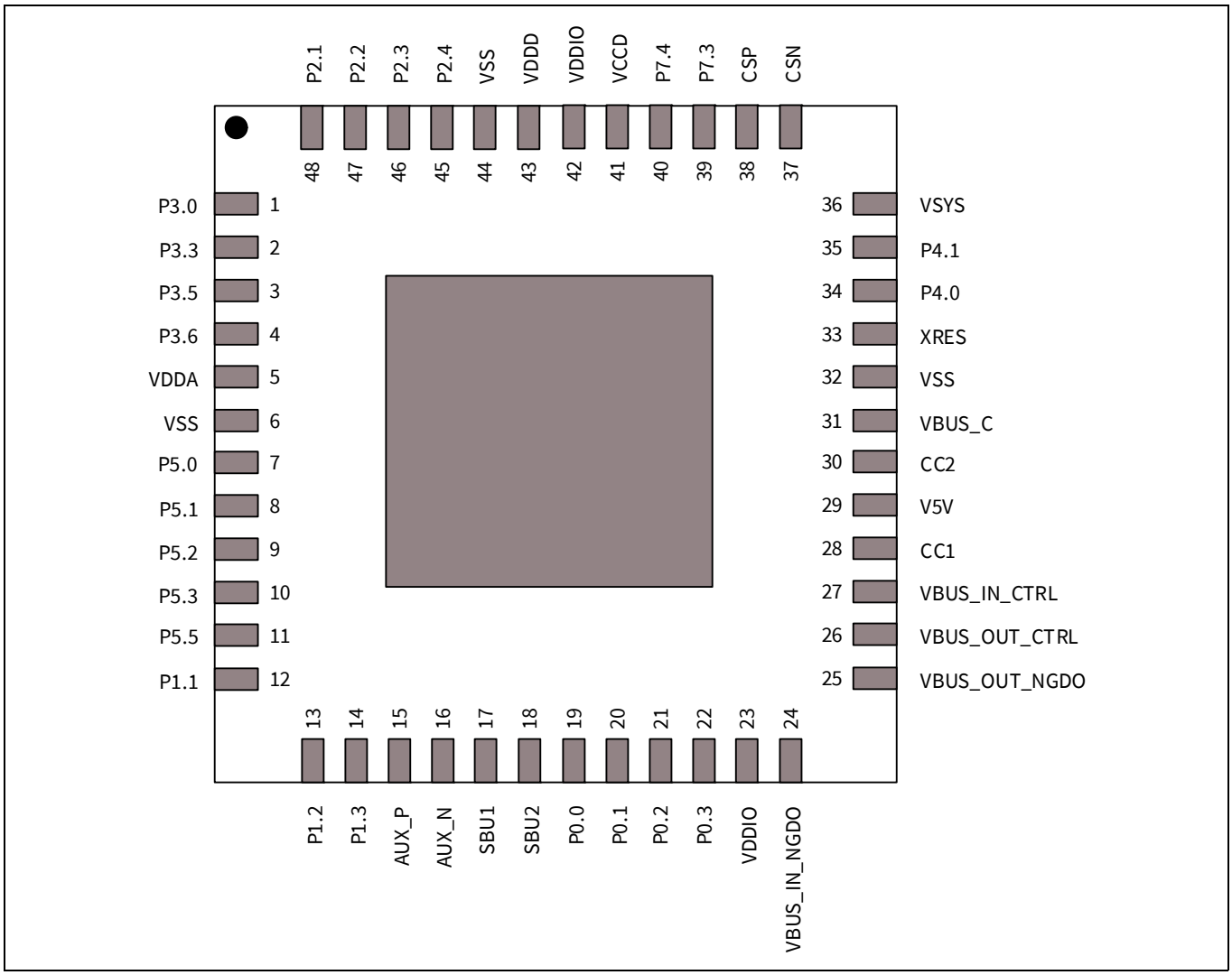


Figure 7 CYPD8125-48LDXI: single-port 48-QFN

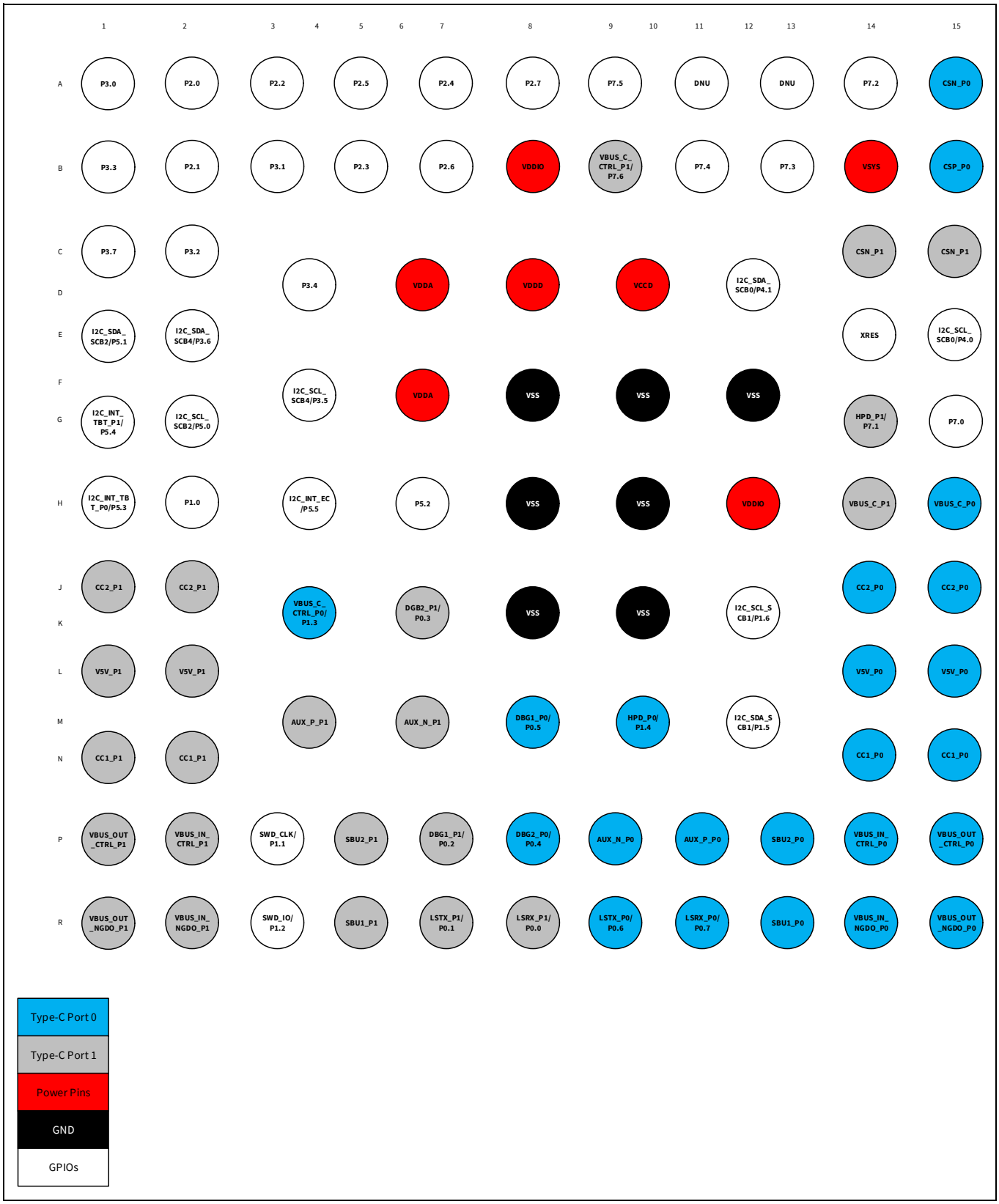


Figure 8 97-ball BGA pin map (top view) for CYPD8225-97BZXI

5 Application diagrams

Figure 9 shows the application diagram using the EZ-PD™ CCG8S device.

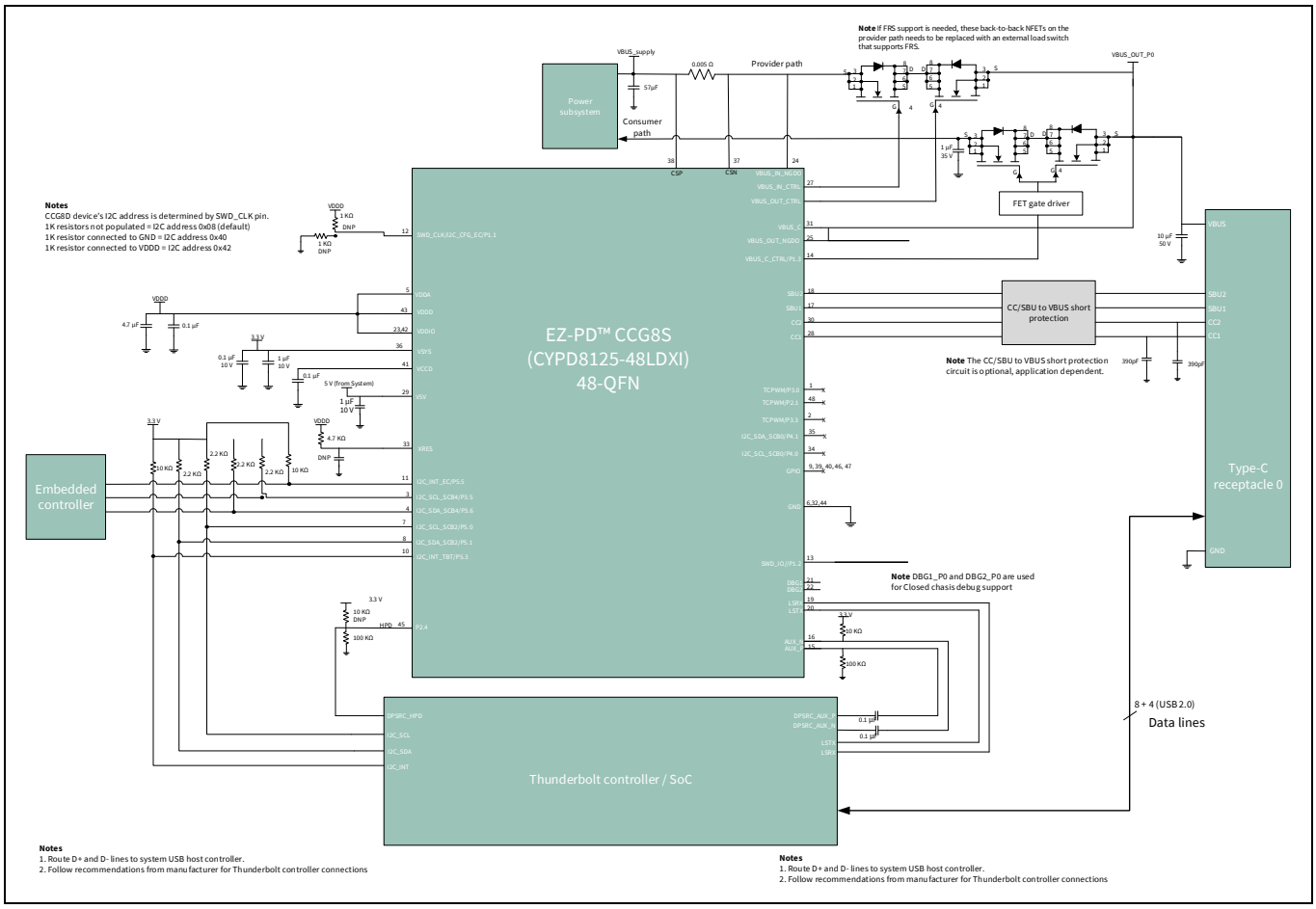


Figure 9 EZ-PD™ CCG8S application diagram

Application diagrams

Figure 10 shows the application diagram using the EZ-PD™ CCG8D device.

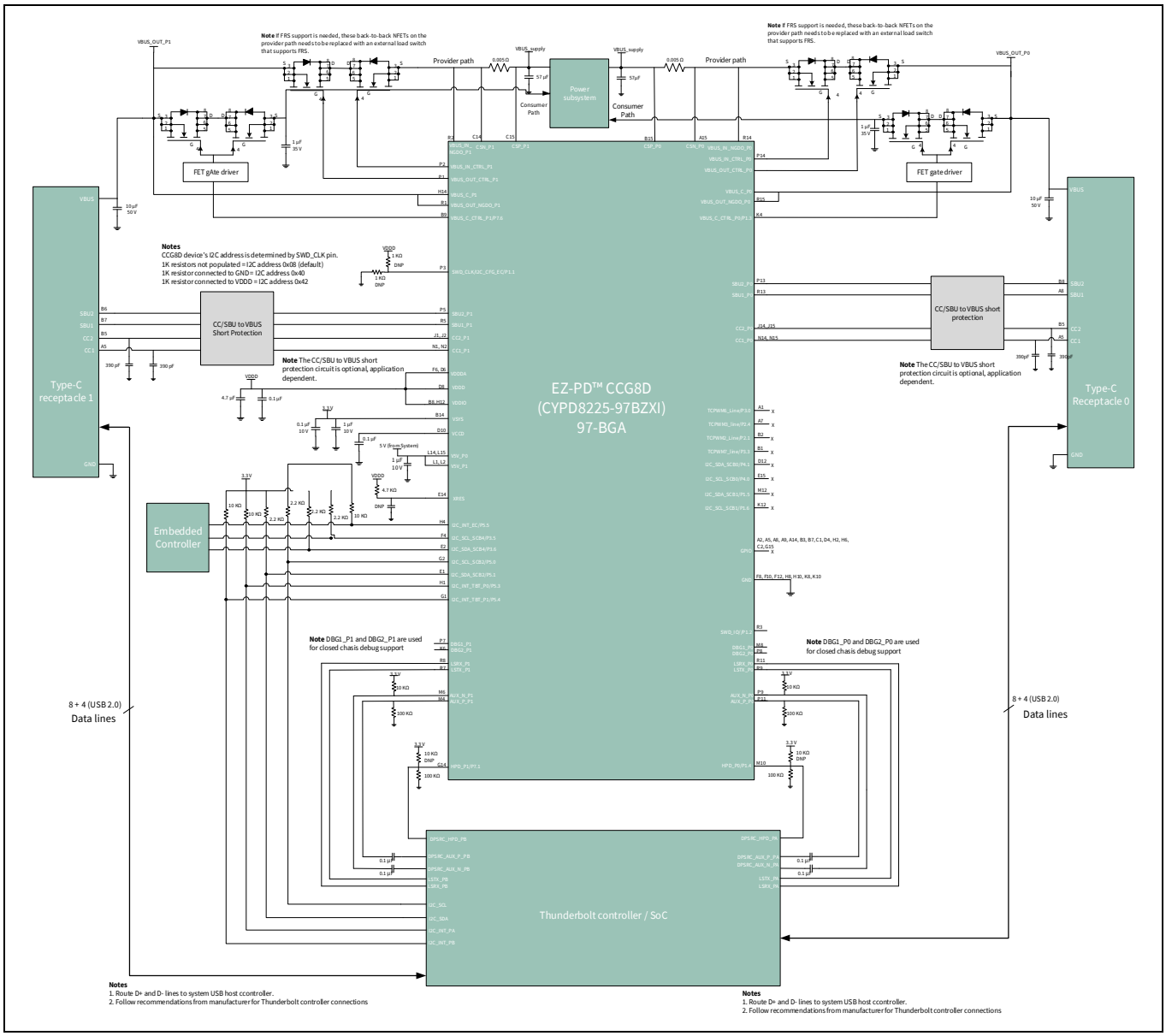


Figure 10 EZ-PD™ CCG8D application diagram

Note: Contact the Infineon local support team for application diagrams for any EPR designs with ≥ 28 V support.

6 Electrical specifications

Table 3 Absolute maximum ratings[6]

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR.ABS#1	V_{DDIO_ABS}	I/O Supply relative to V_{SS} (V_{SSIO} = V_{SSD} = V_{SSA})	–0.5[7]	–	6	V[8]	Absolute minimum-maximum
SID.PWR.ABS#2	V_{CCD_ABS}	Direct digital core voltage input relative to V_{SSD}	–0.5		1.95	V	
SID.PWR.ABS#3	V_{GPIO_ABS}	GPIO voltage	–0.5		6		Absolute minimum-maximum. It cannot be more than "V_{DDIO} +0.5" at any point.
SID.PWR.ABS#4	$V_{GPIO\_OVT\_ABS}$	GPIO OVT voltage	–0.5		6		Absolute minimum-maximum
SID.PWR.ABS#5	I_{GPIO_ABS}	Current per GPIO	–25		25	mA	
SID.PWR.ABS#6	$I_{GPIO\_injection}$	GPIO injection current per pin	–0.5		0.5		
SID.PD.PWR.ABS#1	$V_{CONN\_SOURCE\_ABS}$	Min-max supply voltage relative to V_{SS}	–0.5		6	V	
SID.PD.PWR.ABS#2	V_{SYS_ABS}		–0.5		6		
SID.PD.PWR.ABS#3	V_{BUS_ABS}	Min-max VBUS_C_P0/1 voltage relative to V_{SS}	–0.3		34		Minimum-absolute maximum
SID.PD.PWR.ABS#4	$V_{BUS\_NGDO\_ABS}$	Min-Max VBUS_IN/OUT_P0/1 voltage relative to V_{SS}	–0.3		34		Absolute minimum-maximum
SID.PD.PIN.ABS#1	$V_{CC\_PIN\_ABS}$	Min-max voltage on CC1 and CC2 pins	–0.5		6		Absolute minimum-maximum. It cannot be more than "V_{DDD} +0.5" at any point.
SID.PD.PIN.ABS#2	$V_{SBU\_PIN\_ABS}$	Min-max voltage on SBU1 and SBU2 pins	–0.5		6		
SID.PD.PIN.ABS#3	$V_{USB\_PIN\_ABS}$	Min-max voltage on USBDP and USBDM pins	–0.5		6		
SID.PD.PIN.ABS#4	$V_{AUX\_PIN\_ABS}$	Min-max voltage on AUX_N_P0/1 and AUX_P_P0/1 pins	–0.5		6		
SID.PD.PIN.ABS#5	$V_{CSA\_PIN\_ABS}$	Min-max voltage on CSP_P0/1 and CSN_P0/1 pins	–0.3		34		Absolute minimum-maximum
BID1	TSTG_AMAX	Storage temperature	–55	25	150	°C	Non-operating temperature. Per JESD22-A103 HTSL test.
BID44	ESD_HBM	Electrostatic discharge voltage	2000	–	–	V	Human body model ESD.
BID45	ESD_CDM	Electrostatic discharge voltage	500				Charged device model ESD
BID46	I_LU	Latch-up current limits	–100		100	mA	Max/min current into any input or output, pin-to-pin, pin-to-supply.

Notes

6. Usage above the absolute maximum conditions listed in **Table 3** may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150°C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.
7. In a system, if the negative spike exceeds the minimum voltage specified here, it is recommended to add Schottky diode to clamp the negative spike.
8. All voltages are relative to ground unless otherwise specified.

6.1 Device level specifications

Table 4 DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PWR#1	V_{DDD}	Regulated output voltage when VSYS powered power supply voltage (not to be driven externally)	V_{SYS} - 0.1	–	V_{SYS}	V	-40°C to +85°C T_A; Load current from V_{DDD} = 30 mA
SID.PWR#1A		Regulated output voltage when VBUS powered power supply voltage (not to be driven externally)	3		3.65		-40°C to +85°C T_A
SID.PWR#1B		Power supply voltage for USB bus power	4.25		5.35		USB-PHY internal regulator enabled
SID.PWR#1C		Power supply voltage for USB PHY in bypass mode, Parameters guaranteed	3.05		3.55		USB-PHY internal regulator in Bypass mode
SID.PWR#1D		Power supply voltage for USB PHY in bypass mode, Functionality only guaranteed	2.95		3.63		
SID.PWR#2	$V_{DDWRITE}$	Supply voltage for flash write	2.7		5.5		-40°C to +85°C T_A, All V_{DDD}.
SID.PWR#4	V_{DDIO}	Supply voltage for I/O	1.71		V_{DDD}		
SID.PWR#5	V_{DDA}	Supply voltage for I/O 12-bit ADC block	V_{DDD}		V_{DDD}		-40°C to +85°C T_A, All V_{DDD}; V_{DDA} = V_{DDD}
SID.PWR#6	V_{CCD}	Output voltage For core Logic	–	1.8	–		–
SID.PWR#7	Cefc	External regulator voltage bypass for V_{CCD}	80	100	120	nF	X5R ceramic or better
SID.PWR#8	Cexc	External regulator voltage bypass for V_{DDD}	–	4.7	–	µF	
SID.PWR#9	Cexv	Power supply decoupling capacitor for V5V_0 and V5V_1, V_{SYS}, V_{DDIO}, V_{DDA}		1			
SID.PD.PWR#1	V5V	Power supply for V_{CONN}	4.85	–	5.5	V	-40°C to +85°C T_A
SID.PD.PWR#2	VSYS_UFP	VSYS valid range	2.8		5.5		UFP applications
SID.PD.PWR#2A	VSYS_DFP_DRP		3		5.5		DFP/DRP applications
SID.PD.PWR#3	VBUS	VBUS_C_P0/1 valid range	4		30		–
SID.PD.PWR#3A	VBUS_NGDO	VBUS_IN/OUT_NGDO_P0/1 valid range	4		30		
Active mode, VDD = 1.71 V to 5.5 V							
SID16	IDD11	Execute from flash; CPU at 24 MHz	–	5.8	–	mA	Typ = 25°C @ V_{DD} = 3.3 V
SID19	IDD14	Execute from flash; CPU at 48 MHz		11.2			
Sleep mode, VDD = 2.0 V to 5.5 V (Regulator ON)							
SID22	IDD17	I^2C wakeup, WDT, and comparators on 6 MHz	–	1.3	2.2	mA	Typ = 25°C @ V_{DD} = 3.3 V Max = 85°C @ 5.5 V
SID25	IDD20	I^2C wakeup, WDT, and comparators on. 12 MHz		1.85	2.5		

Table 4 DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
Deep sleep mode, VDD = 2.7 V to 5.5 V							
SID34	IDD29	I^2C wakeup and WDT on.		250			Typ = 25°C @ V_{DD} = 3.3 V Power source = VSYS, Type-C not attached, CC enabled for wakeup, Rp and Rd connected at 70 ms intervals by CPU. Rp, Rd connection should be enabled for both PD ports If VBUS_IN_NGDO and VBUS_OUT_NGDO also present, refer to SID.PD.GD#11 and SID.PD.GD#12
SID_DS1	IDD_DS1	VSYS = 3.3 V Port-0 and 1: CC wakeup on, Type-C not connected	–	200	–	µA	Power source = VSYS, Type-C not attached, CC enabled for wakeup, Rp and Rd connected at 70 ms intervals by CPU. Rp, Rd connection should be enabled for both PD ports. If VBUS_IN_NGDO and VBUS_OUT_NGDO are also present, refer to SID.PD.GD#11 and SID.PD.GD#12
SID_DS3	IDD_DS2	VSYS = 3.3 V Port-1: CC wakeup on, Port-0: CC/VCONN/SBU/NGDO/ CSA/UVOV enabled and SBU comparators disabled		600			Power source = VSYS, One port attached, chip in Deepsleep Port-1: CC wakeup on, Port-0: CC/ VCONN/ SBU/NGDO/CSA/ UVOV enabled and SBU comparators disabled
SID_DS3_A	IDD_DS2A	VSYS = 3.3 V Port-0 and 1: CC/ VCONN/SBU/NGDO/CSA/U VOV enabled and SBU comparators disabled		1100			Both ports attached (CC/ VCONN/ SBU/NGDO/CSA/ UVOV enabled and SBU comparators disabled), chip in deep sleep
XRES current							
SID307	IDD_XR	Supply current while XRES asserted	–	130	–	µA	Power source = VSYS = 3.3 V, Type-C not attached, TA = 25°C If VBUS_IN_NGDO and VBUS_OUT_NGDO also present, refer to SID.PD.GD#11a and SID.PD.GD#12a

Table 5 AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.CPU#1	F_{CPU}	CPU frequency	DC	–	48	MHz	-40°C to +85°C TA, All V_{DDD}
SID.CPU#2	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.CPU#3	$T_{DEEPSLEEP}$	Wakeup from deep sleep mode		35			

6.2 GPIO

Table 6 GPIO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO.DC#1	Vih_CMOS	Input voltage HIGH threshold	0.7*V_{DD}	–	–	V	CMOS input
SID.GPIO.DC#2	Vil_CMOS	Input voltage LOW threshold	–		0.3 * V_{DD}		
SID.GPIO.DC#1a	Vih_VDDIO2.7-	LVTTL input, VDD < 2.7 V	0.7*V_{DD}		–		–
SID.GPIO.DC#2a	Vil_VDDIO2.7-		–		0.3 * V_{DD}		
SID.GPIO.DC#1b	Vih_VDDIO2.7+	LVTTL input, VDD ≥ 2.7 V	2		–		
SID.GPIO.DC#2b	Vil_VDDIO2.7+		–		0.8		
SID.GPIO.DC#1c	Vih_VCCHIB	V_{IH}, 1.8-V input mode	1.26		–		
SID.GPIO.DC#2c	Vil_VCCHIB	V_{IL}, 1.8-V input mode	–		0.54		
SID.GPIO.DC#4	V_{OH}	Output voltage HIGH level	V_{DD}-0.6		–		Ioh = 4 mA at 3-V V_{DD}
SID.GPIO.DC#4a	V_{OH}		V_{DD}-0.5				Ioh = 1 mA at 1.8-V V_{DD}
SID.GPIO.DC#5	V_{OL}	Output voltage LOW level	–		0.6		Iol = 4 mA at 1.8-V V_{DD}
SID.GPIO.DC#5a	V_{OL}				0.6		Iol = 10 mA at 3-V V_{DD}
SID.GPIO.DC#5b	V_{OL}				0.4		Iol = 3 mA at 3-V V_{DD}
SID.GPIO.DC#6	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	kΩ	–
SID.GPIO.DC#7	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5		–
SID.GPIO.DC#8	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25°C, V_{DD} = 3.0-V
SID.GPIO.DC#8a	I_{IL_CTBM}	Input leakage on CTBm input pins			4		–
SID.GPIO.DC#9	C_{IN}	Input capacitance			7	pF	
SID.GPIO.DC#3b	V_{HYSTTL}	Input hysteresis LVTTL VDD > 2.7 V	15	40	–	mV	
SID.GPIO.DC#3	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05* V_{DD}	–			V_{DDIO} < 4.5 V
SID.GPIO.DC#3a	$V_{HYSCMOS55}$	Input hysteresis CMOS	200.0				V_{DDIO} > 4.5 V
SID.GPIO.DC#3c	V_{HYS_VCCHIB}	Input hysteresis, 1.8 V input mode	90				

Table 6 GPIO DC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO.DC#10	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	µA	–
SID.GPIO.DC#11	I_{TOT_GPIO}	Maximum total source or sink chip current when V_{DDIO} supplied externally			200	mA	
SID.GPIO.DC#11a	$I_{TOT\_GPIO\_VDDD}$	Maximum total source or sink chip current when V_{DDD} shorted to V_{DDIO} on board			10		

Table 7 GPIO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.GPIO.AC#1	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DD}, Cload = 25 pF
SID.GPIO.AC#2	T_{FALLF}	Fall time in Fast Strong mode	2		12		
SID.GPIO.AC#3	T_{RISES}	Rise time in Slow Strong mode	10		60		
SID.GPIO.AC#4	T_{FALLS}	Fall time in Slow Strong mode	10		60		
SID.GPIO.AC#5	$F_{GPIOUT1}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V. Fast Strong mode.	–		33	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID.GPIO.AC#6	$F_{GPIOUT2}$	GPIO Fout; 1.71 V ≤ V_{DD} ≤ 3.3 V. Fast Strong mode.			16.7		
SID.GPIO.AC#7	$F_{GPIOUT3}$	GPIO Fout; 3.3 V ≤ V_{DD} ≤ 5.5 V. Slow Strong mode.			7		
SID.GPIO.AC#8	$F_{GPIOUT4}$	GPIO Fout; 1.71 V ≤ V_{DD} ≤ 3.3 V. Slow Strong mode.			3.5		
SID.GPIO.AC#9	F_{GPIOIN}	GPIO input operating frequency; 1.71 V ≤ V_{DD} ≤ 5.5 V			16		90/10% V_{IO}

6.2.1 XRES

Table 8 XRES DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID.XRES.DC#1	VIH_XRES	Input voltage HIGH threshold	0.7* V_{DD}	–	–	V	CMOS input
SID.XRES.DC#2	VIL_XRES	Input voltage LOW threshold	–		0.3* V_{DD}		
SID.XRES.DC#3	CIN_XRES	Input capacitance	–		7	pF	–
SID.XRES.DC#4	VHYSXRES	Input voltage hysteresis		0.05 * V_{DDIO}	–	mV	
SID.XRES.DC#5	IDIODE	Current through protection diode to VDD/Vss		–	100	µA	

Table 9 XRES AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.XRES.AC#1	$T_{RESETWIDTH}$	Reset pulse width	5	–	–	µs	-40°C to +85°C TA, All V_{DDIO}
SID.XRES.AC#2	T_{XRES_GF}	External reset glitch filter period	–	20		ns	
BID194	$T_{RESETWAKE}$	Wake-up time from Reset release		–	2.7	ms	–

6.3 Analog peripherals

6.3.1 Temperature sensor

Table 10 Temperature sensor specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID93	TSENSACC	Temperature sensor accuracy	-5	±1	5	C	-40 to +85°C

6.3.2 SAR ADC

Table 11 SAR ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID94	A_RES	Resolution	–	–	12	bits	–
SID95	A_CHNLS_S	Number of channels - single ended			8		8 Full Speed.
SID96	A-CHNKS_D	Number of channels - differential			4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity			–		Yes.
SID98	A_GAINERR	Gain error			±0.1	%	With external reference.
SID99	A_OFFSET	Input offset voltage. Guaranteed by characterization			2	mV	Measured with 1-V reference
SID100	A_ISAR	Current consumption			1	mA	–
SID101	A_VINS	Input voltage range - single ended	V_{SS}		V_{DDA}	V	
SID102	A_VIND	Input voltage range - differential	V_{SS}		V_{DDA}		
SID103	A_INRES	Input resistance	–		2.2	kΩ	
SID104	A_INCAP	Input capacitance			10	pF	
SID260	VREFSAR	Trimmed internal reference to SAR	1.18	1.2	1.22	V	

Table 12 SAR ADC AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID106	A_PSRR	Power supply rejection ratio	70	–	–	dB	–
SID107	A_CMRR	Common mode rejection ratio	66				Measured at 1 V
SID108	A_SAMP	Sample rate	–		1	Msps	–
SID109	A_SNR	Signal-to-noise and distortion ratio (SINAD)	65		–	dB	F_{in} = 10 kHz
SID110	A_BW	Input bandwidth without aliasing	–		A_samp/2	kHz	–
SID111	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	-1.7		2	LSB	VREF = 1 to V_{DD}
SID111A	A_INL	Integral non linearity. V_{DDD} = 1.71 to 3.6, 1 Msps	-1.5		1.7		VREF = 1.71 to V_{DD}
SID111B	A_INL	Integral non linearity. V_{DD} = 1.71 to 5.5, 500 ksps	-1.5		1.7		VREF = 1 to V_{DD}
SID112	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 1 Msps	-1		2.2		VREF = 1 to V_{DD}
SID112A	A_DNL	Differential non linearity. V_{DD} = 1.71 to 3.6, 1 Msps	-1		2		VREF = 1.71 to V_{DD}
SID112B	A_DNL	Differential non linearity. V_{DD} = 1.71 to 5.5, 500 ksps	-1		2.2		VREF = 1 to V_{DD}

Table 12 SAR ADC AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID113	A_THD	Total harmonic distortion	–	–	-65	dB	F_{in} = 10 kHz
SID261	FSARINTREF	SAR operating speed without external ref. bypass			100	ksps	12-bit resolution

6.4 Digital peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the timer mode.

6.4.1 Timer/counter/PWM

Table 13 TCPWM specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.TCPWM#1	ITCPWM1	Block current consumption at 3 MHz	–	–	45	µA	All modes (Timer/counter/PWM)
SID.TCPWM#2	ITCPWM2	Block current consumption at 12 MHz			155		
SID.TCPWM#2A	ITCPWM3	Block current consumption at 48 MHz			650		
SID.TCPWM#3	TCPWMFREQ	Operating frequency			Fc	MHz	Fc_{max} = Fcpu. Maximum = 48 MHz
SID.TCPWM#4	TPWMENEXT	Input trigger pulse width for all trigger* events	2/Fc		–	ns	Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM#5	TPWMEXT	Output trigger* pulse widths	2/Fc				Minimum possible width of overflow, underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM#5A	TCRES	Resolution of counter	1/Fc				Minimum time between successive counts
SID.TCPWM#5B	PWMRES	PWM resolution	1/Fc				Minimum pulse width of PWM output
SID.TCPWM#5C	QRES	Quadrature inputs resolution	1/Fc				Minimum pulse width between Quadrature phase inputs.

* Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected

6.4.2 I²C

Table 14 Fixed I²C DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID149	II2C1	Block current consumption at 100 kHz	–	–	60	µA	–
SID150	II2C2	Block current consumption at 400 kHz			185		
SID151	II2C3	Block current consumption at 1 Mbps			650		
SID152	II2C4	Block current consumption when I2C enabled in deep sleep mode		1	–		

Table 15 Fixed I2C AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID153	FI2C1	Bit rate	–	–	1	Mbps	–
SID.I2C#1	FSCLI2C_SM	I2C SCL clock frequency	0		100	kHz	Standard Mode
SID.I2C#2	FSCLI2C_FM		0		400		Fast Mode
SID.I2C#33	FSCLI2C_FMP		0		1000		Fast Mode Plus
SID.I2C#3	THDSTAI2C_SM	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4		–	µs	Standard Mode
SID.I2C#4	THDSTAI2C_FM	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6				Fast Mode
SID.I2C#34	THDSTAI2C_FMP		0.26				Fast Mode Plus
SID.I2C#5	TSUSTAI2C_SM	Setup time for a repeated START condition	4.7				Standard Mode
SID.I2C#6	TSUSTAI2C_FM		0.6				Fast Mode
SID.I2C#35	TSUSTAI2C_FMP		0.26				Fast Mode Plus
SID.I2C#7	TLOWI2C_SM	LOW period of the SCL clock	4.7				Standard Mode
SID.I2C#8	TLOWI2C_FM		1.3				Fast Mode
SID.I2C#36	TLOWI2C_FMP		0.5				Fast Mode Plus
SID.I2C#9	THIGHI2C_SM	HIGH period of the SCL clock	4				Standard Mode
SID.I2C#10	THIGHI2C_FM		0.6				Fast Mode
SID.I2C#37	THIGHI2C_FMP		0.3				Fast Mode Plus
SID.I2C#11	THDDATI2C	Data hold time	0				All I2C speeds
SID.I2C#12	TSUDATI2C_SM	Data setup time	250.0			ns	Standard Mode
SID.I2C#13	TSUDATI2C_FM		100				Fast Mode
SID.I2C#38	TSUDATI2C_FMP		50				Fast Mode Plus
SID.I2C#14	TSUSTOI2C_SM	Setup time for I2C STOP condition	4			µs	Standard Mode
SID.I2C#15	TSUSTOI2C_FM		0.6				Fast Mode
SID.I2C#39	TSUSTOI2C_FMP		0.26				Fast Mode Plus
SID.I2C#16	CB_SM	Capacitive load for each I2C bus line	–		400	pF	Standard Mode
SID.I2C#17	CB_FM				400		Fast Mode
SID.I2C#40	CB_FMP				550		Fast Mode Plus

Table 15 Fixed I2C AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.I2C#18	TVDDATI2C_SM	Data valid time	–	–	3.45	µs	Standard Mode
SID.I2C#19	TVDDATI2C_FM	Data valid time			0.9		Fast Mode
SID.I2C#41	TVDDATI2C_FMP	Data Valid time			0.45		Fast ode Plus
SID.I2C#20	TVDACKI2C_SM	Data valid acknowledge time			3.45		Standard Mode
SID.I2C#21	TVDACKI2C_FM	Data valid acknowledge time			0.9		Fast Mode
SID.I2C#42	TVDACKI2C_FMP	Data Valid acknowledge time			0.45		Fast Mode Plus
SID.I2C#22	TSPI2C_FM	Pulse width of spikes suppressed by input filter			50	ns	Fast Mode
SID.I2C#43	TSPI2C_FMP	Pulse width of spikes suppressed by input filter			50		Fast Mode Plus
SID.I2C#23	TBUFI2C_SM	Bus free time between a STOP and START condition	4.7		–	µs	Standard Mode
SID.I2C#24	TBUFI2C_FM	Bus free time between a STOP and START condition	1.3		–		Fast Mode
SID.I2C#44	TBUFI2C_FMP	Bus Free time between a STOP and START condition	0.5		–		Fast ode Plus
SID.I2C#25	VIL_I2C	Input low voltage	-0.5		0.3 * V_{DDIO}	V	Fast and Standard mode I^2C speeds
SID.I2C#26	VIH_I2C	Input high voltage	0.7* V_{DDIO}		–		Fast and Standard Mode I^2C speeds
SID.I2C#27	VOL_I2C_L	Output low voltage, low supply range	–		0.2 * V_{DDIO}		Fast and Standard Mode I^2C speeds, V_{DDIO} < 2V, 2 mA sink
SID.I2C#28	VOL_I2C_H	Output low voltage, high supply range			0.4		Fast and Standard Mode I^2C speeds, V_{DDIO} < 2 V, 2 mA sink
SID.I2C#29	IOL_I2C_SM	I2C output low current	3		–	mA	Standard Mode, 1.71V ≤ V_{DDIO} ≤ 5.5 V, load = CB_SM, VOL = 0.4 V
SID.I2C#30	I2C_VHYS_HV	I2C input hysteresis	0.05 * V_{DDIO}			mV	Fast and Standard Mode I^2C speeds, 2V ≤ V_{DDIO} ≤ 4.5 V
SID.I2C#30A	I2C_VHYS_5V	I2C input hysteresis	200				Fast and Standard Mode I^2C speeds, V_{DDIO} > 4.5 V
SID.I2C#31	I2C_VHYS_LV	I2C input hysteresis	0.10 * V_{DDIO}				Fast and Standard Mode I^2C speeds, V_{DDIO} < 2 V
COM.REQ#7	I2C_ADD	I2C address width	–		8	bits	7-bit address and 1 RW bit
SID.I2C#32	IOL_I2C_FM	I2C output low current	6		–	mA	Fast mode, 1.71 V ≤ V_{DDIO} ≤ 5.5 V, load = CB_SM, VOL = 0.6V

Table 15 Fixed I2C AC specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.I2C#45	IOL_I2C_FMP	I2C output low current, high voltage range	20	–	–	mA	Fast Mode Plus, 3.0 V ≤ V_{DDD} ≤ 5.5V, load = CB_FMP, –40°C to 85°C TA, GPIO_OVTV2 port only
SID.I2C#45A	IOL_I2C_FMP	I2C output low current, low voltage range	3				Fast Mode Plus, 1.71 V ≤ V_{DDD} ≤ 3.0 V, load = CB_FMP, –40°C to 85°C TA

6.4.3 UART

Table 16 Fixed UART DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID160	I_{UART1}	Block current consumption at 100 kbps	–	–	125	µA	–
SID161	I_{UART2}	Block current consumption at 1000 kbps			312		

Table 17 Fixed UART AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID162	FUART	Bit rate	–	–	1	Mbps	–

6.4.4 SPI

Table 18 Fixed SPI DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID163	ISPI1	Block current consumption at 1 Mbps	–	–	360	µA	–
SID164	ISPI2	Block current consumption at 4 Mbps			560		
SID165	ISPI3	Block current consumption at 8 Mbps			600		

Table 19 Fixed SPI AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID166	FSPI	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 20 Fixed SPI master mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID167	TDMO	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	TDSI	MISO valid before SClock capturing edge	20		–		Full clock, late MISO sampling
SID169	THMO	Previous MOSI data hold time	0				Referred to Slave capturing edge

Table 21 Fixed SPI slave mode AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID170	TDMI	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	TDSO	MISO valid after Sclock driving edge	–		48 + 3*Tcpu		Tcpu = 1/Fcpu
SID171A	TDSO_EXT	MISO valid after Sclock driving edge in Ext. Clk. mode			48		–
SID172	THSO	Previous MISO data hold time	0		–		
SID172A	TSSELSCK	SSEL valid to first SCK Valid edge	100				

6.4.5 Memory

Table 22 Flash DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID173	V_{PE}	Erase and Program voltage	1.71	–	5.5	V	–
SID173A	I_{PW}	Page write current at 16 MHz	–		3.5	mA	5.5 V VDD

Table 23 Flash AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID174	$T_{ROWWRITE}$	Row (Block) write time (erase and program)	–	–	20	ms	Row (Block) = 256 bytes
SID175	$T_{ROWERASE}$	Row erase time			16		–
SID176	$T_{ROWPROGRAM}$	Row program time after erase			7		
SID178	$T_{BULKERASE}$	Bulk erase time (32K Bytes)			35		
SID180	$T_{DEVPROG}$	Total device program time			7	seconds	
SID181	F_{END}	Flash endurance	100K	–	–	cycles	
SID182	F_{RET}	Flash retention. Ta ≤ 55°C, 100K P/E cycles.	20			years	
SID182a		Flash retention. Ta ≤ 85°C, 10K P/E cycles.	10				
SID256	T_{WS48}	Number of wait states at 48 MHz	2				CPU execution from flash
SID257	T_{WS24}	Number of wait states at 24 MHz	1				

6.5 System resources

6.5.1 Power-on reset with brown-out DC specifications

Table 24 Power-on reset specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.POR#1	SR_POWER_UP	Power supply slew rate	1	–	67	V/ms	-40°C to +85°C TA, All VDDD; At power-up
SID.POR#2	$V_{RISEIPOR}$	Rising trip voltage	0.8		1.5	V	–
SID.POR#3	$V_{FALLIPOR}$	Falling trip voltage	0.7		1.4		

Table 25 Brown-out detect (BOD) for VCCD

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.BOD#1	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID.BOD#2	$V_{FALLDPSLP}$	BOD trip voltage in deep sleep	1.1		1.5		

6.5.2 SWD

Table 26 SWD interface

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ V_{DD} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 FCPU
SID.SWD#2	F_SWDCLK2	1.71 V ≤ V_{DD} ≤ 3.3 V			7		
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T		–	ns	–
SID.SWD#4	T_SWDI_HOLD		0.25*T				
SID.SWD#5	T_SWDO_VALID		–		0.5*T		
SID.SWD#6	T_SWDO_HOLD		1		–		

6.5.3 Internal main oscillator

Table 27 IMO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.IMO.DC#1	IIMO1	IMO operating current at 48 MHz	–	–	250	µA	–
SID.IMO.DC#2	IIMO2	IMO operating current at 24 MHz			180		

Table 28 IMO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.IMO.AC#1	FIMO	IMO frequency	–	48	–	MHz	-40°C to +85°C TA, All V_{DDD}
SID.IMO.AC#2	FIMO_RES	IMO frequency resolution		0.25		%	
SID.IMO.AC#3	IMO_STL	IMO settling time when trim register is changed		–	200	ns	25°C TA, All V_{DDD}, FIMO = 48 MHz
SID.IMO.AC#4	FIMOTOL1	Frequency variation at 24, 32 and 48 MHz (trimmed)			±2	%	2.7V ≤ V_{DDD} < 5.5V. And -25°C ≤ TA ≤ 85°C
SID.IMO.AC#4a	FIMOTOLVCCD	Frequency variation at 24, 32 and 48 MHz (trimmed)			±4		All conditions
SID.IMO.AC#5	IMO_HOP_RANGE	FIMO variation range with TRIM registers	-10		10		25°C TA, All V_{DDD}, 48 MHz = F_{IMO}
SID.IMO.AC#6	TSTARTIMO	IMO startup time	–		7	µs	–
SID.IMO.AC#7	TJITRM-SIMO2	RMS jitter at 24 MHz		145	–	–	

6.5.4 Internal low-speed oscillator

Table 29 ILO DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ILO.DC#1	IILO1	ILO operating current at 32 kHz	–	0.3	1.05	µA	–
SID.ILO.DC#2	IILOLEAK	ILO leakage current		2	15	nA	

Table 30 ILO AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.ILO.AC#1	FILO	Operating frequency	20.0	40.0	80.0	kHz	–
SID.ILO.AC#2	TSTAR-TILO1	ILO start-up time	–	–	2	ms	
SID.ILO.AC#3	TLIODUTY	ILO duty cycle	40	50	60	%	

6.6 USB PD peripherals

6.6.1 Analog to digital converter

Table 31 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.ADC.DC#1	Resolution	ADC resolution	–	–	–	–	–
SID.PD.ADC.DC#2	INL	Integral non-linearity	-1.5	–	1.5	LSB	
SID.PD.ADC.DC#3	DNL	Differential non-linearity	-2.5		2.5		
SID.PD.ADC.DC#4	Gain Error	Gain error	-1.5		1.5		
SID.PD.ADC.DC#5	VREF_ADC1	Reference voltage of ADC	V_{DDD} min		V_{DDD} max	V	Reference voltage generated from V_{DDD}
SID.PD.ADC.DC#6	VREF_ADC2	Reference voltage of ADC	1.96	2	2.04		Reference voltage generated from deep sleep reference

Table 32 ADC DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.ADC.AC#7	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

6.6.2 VBUS regulator

Table 33 VBUS regulator DC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.20VREG.DC#1	VBUSREG1	VBUS regulator output voltage (minimum VBUS = 4.2 V to 28 V)	3	–	3.65	V	Chip powered through VBUS_C_P1/VBUS_C_P2 and output measured on V_{DDD}
SID.PD.20VREG.DC#2	VBUSREG2	VBUS regulator output voltage (minimum VBUS = 4 V to 4.2 V)	3		3.65		

Table 34 VBUS regulator AC specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.20VREG.AC#1	Tstart	Total start up time for the regulator supply outputs	–	–	200	µs	Apply VBUS and measure start time on VDDD pin.
SID.PD.20VREG.AC#2	Tstop	Regulator power down time from vreg_en = 0 to regulator disable			4		Time from assertion of an internal disable signal for load current on VDDD to decrease from 30 mA to 10 µA.

6.6.3 CSA

Table 35 CSA specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.HS-CSA.DC#1	Isense_scp	Current sense accuracy for SCP at 6A,10A	–	±10	–	%	–
SID.PD.HS-CSA.DC#1a	Isense_scp_epr			±12			For 30-V EPR
SID.PD.HS-CSA.DC#2	Vsense_rcp	RCP sensing threshold across “Rsense”		2	4	mV	–
SID.PD.HS-CSA.DC#3a	Isense_ocp_2A	Current sense accuracy for OCP at 2A, 3A, and 4A		±15	–	%	
SID.PD.HS-CSA.DC#3b	Isense_ocp_5A	Current sense accuracy for OCP at 5A		±10			
SID.PD.HS-CSA.DC#3c	Isense_ocp_5A_epr			±12			For 30-V EPR
SID.PD.HS-CSA.DC#3	Isense_ocp_1A	Current sense accuracy for OCP at 1A		±20			–
SID.PD.HS-CSA.DC#4	Rsense	External Rsense	4.95	5	5.05	mΩ	
SID.PD.HS-CSA.DC#5	Vtrip_slow_rcp_33pct	Slow RCP trip points set at 5V with 33% tap point selected	4.5	–	5.5	V	
SID.PD.HS-CSA.DC#5a	Vtrip_slow_rcp_10pct	Slow RCP trip points set at 20V with 10% tap point selected	18		22		
SID.PD.HS-CSA.DC#5b	Vtrip_slow_rcp_6pct	Slow RCP trip points set at 30V with 60% tap point selected	27		33		
SID.PD.HS-CSA.DC#9	Isb_csp_5v	CSP pin input leakage when SCP, OCP and RCP blocks are OFF	–		6	µA	CSP = CSN = 5 V
SID.PD.HS-CSA.DC#10	Isb_csn_5v	CSN pin input leakage when SCP, OCP and RCP blocks are OFF			5		
SID.PD.HS-CSA.DC#9a	Isb_csp_30v	CSP pin input leakage when SCP, OCP and RCP blocks are OFF			26		CSP = CSN = 30 V
SID.PD.HS-CSA.DC#10a	Isb_csn_30v	CSN pin input leakage when SCP, OCP and RCP blocks are OFF			5		
SID.PD.HS-CSA.DC#17	I_CSP_SCP_ON_OCP_ON_RCP_ON	CSP pin current when SCP, OCP and RCP blocks are ON			500		–
SID.PD.HS-CSA.DC#18	I_CSN_SCP_ON_OCP_ON_RCP_ON	CSN pin current when SCP, OCP and RCP blocks are ON			65		

Table 35 CSA specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.HS-CSA.AC#1	Tdelay_scp_6A	SCP Delay in 6A mode (5-mV overdrive)	–	–	300	ns	Guaranteed by design
SID.PD.HS-CSA.AC#2	Tdelay_scp_10A	SCP Delay in 10A mode (5-mV overdrive)			300		
SID.PD.HS-CSA.AC#3	Tdelay_rcp	RCP delay (5-mV overdrive)			250		
SID.PD.HS-CSA.AC#4	Tdelay_ocp	OCP delay (5-mV overdrive)			250		

6.6.4 VBUS discharge

Table 36 VBUS discharge specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.VBUS_DISC#1	Ron1	20V NMOS ON resistance (with dischg_ds<0> = 1; dischg_ds<4:1> = 0)	1500	–	3000	Ω	–
SID.PD.VBUS_DISC#2	Ron2	20V NMOS ON resistance (with dischg_ds<1:0> = 1; dischg_ds<4:2> = 0)	750		1500		
SID.PD.VBUS_DISC#3	Ron3	20V NMOS ON resistance (with dischg_ds<2:0> = 1; dischg_ds<4:3> = 0)	500		1000		
SID.PD.VBUS_DISC#4	Ron4	20V NMOS ON resistance (with dischg_ds<3:0> = 1; dischg_ds<4> = 0)	375		750		
SID.PD.VBUS_DISC#5	Ron5	20V NMOS ON resistance (with dischg_ds<4:0> = 1)	300		600		

6.6.5 UVOV

Table 37 UVOV specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.UVOV#1	VTHUVOV1	Voltage threshold accuracy in active mode using bandgap ref	–	+/-3	–	%	–
SID.PD.UVOV#2	VTHUVOV2	Voltage threshold accuracy in deep sleep mode using deep sleep ref.		+/-5			
SID.PD.COMP_ACC#1	COMP_ACC	Comparator input offset at 4 sigma	-15	–	15.0	mV	
SID.PD.UVOV.AC#1	Tov_gate	Delay from 0V threshold trip to external NFET power gate turn OFF	–		50	µs	

6.6.6 SBU

Table 38 SBU switch specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.SBU.DC#1	Ron_hs1	Switch on resistance in HS range (input from 0 V to 0.4 V range)	–	–	4.5	Ω	–
SID.PD.SBU.DC#2	Ron_fs	Switch on resistance in FS range (input from 0 V to 3.6 V range)			6.5		
SID.PD.SBU.DC#3	Ron_flat_hs1	Switch flat resistance in HS range (input from 0 V to 0.4 V range)			0.5		
SID.PD.SBU.DC#4	Ron_flat_fs	Switch flat resistance in FS range (input from 0 V to 3.6 V range)			2.5		
SID.PD.SBU.DC#7	Ileak1	Pin leakage current for SBU1, SBU2 @ 3.6V with AUX_P/AUX_N floating, V_{DDD} = 3.3 V @ 85°C	-4.5		4.5	µA	
SID.PD.SBU.DC#7a	Ileak2	Pin leakage current for AUX_P/AUX_N @ 3.6 V with SBU1, SBU2 floating, V_{DDD} = 3.3 V @ 85°C	-1		1		
SID.PD.SBU.DC#8	Rpu_aux_1	Pull up resistance on AUX_N	80		120	kΩ	
SID.PD.SBU.DC#9	Rpu_aux_2	Pull up resistance on AUX_P	0.8		1.2	MΩ	
SID.PD.SBU.DC#10	Rpd_aux_1	Pull down resistance on AUX_P	80		120	kΩ	
SID.PD.SBU.DC#11	Rpd_aux_2	Pull down resistance on AUX_N	0.8		1.2	MΩ	
SID.PD.SBU.DC#12	Rpd_aux_3	Pull down resistance on AUX_P	329		611	kΩ	
SID.PD.SBU.DC#13	Rpd_aux_4	Pull down resistance on AUX_N	3.29		6.11	MΩ	
SID.PD.SBU.AC#1	Con	Switch on capacitance	–		50	pF	
SID.PD.SBU.AC#2	Coff	Switch off capacitance-connector side			25		
SID.PD.SBU.AC#3	Off_isolation	Switch isolation at F = 1 MHz			–50	dB	Guaranteed by design
SID.PD.SBU.AC#4	X_talk_AC	Cross talk of switch at F = 1 MHz IN1/2 to IN2/1 when is data transferred from OUT			–50		

6.6.7 VCONN switch

Table 39 VCONN switch specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.VCONN.DC#1	Ron	Switch ON resistance at V5V = 5 V with 215 mA load current	–	0.7	1.3	Ω	–
SID.PD.VCONN.DC#3	Ileak	Connector side pin leakage current		–	10	µA	
SID.PD.VCONN.DC#4	VTHDETECT_V5V	Threshold voltage of the v5v detector	2.05		2.65	V	
SID.PD.VCONN.DC#9	Iocp	Overcurrent detection range for CC1/CC2	550			mA	
SID.PD.VCONN.DC#12	OCP_hysteresis	Overcurrent detection hysteresis	20		80		
SID.PD.VCONNAC#1	Ton	Switch turn-on time	–		200	µs	
SID.PD.VCONNAC#2	Toff	Switch turn-off time			3		
SID.PD.VCONN.DC#14	Rfrs_pd	Fast role swap request transmit driver resistance (excluding cable resistance)			5	Ω	

6.6.8 VSYS

Table 40 VSYS regulator

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.vdddsw.DC#1	Res_sw	Resistance from supply input to the output supply V_{DDD}	–	–	1.5	Ω	Measured with a load current of 5 mA - 10 mA on V_{DDD}.

6.6.9 Gate driver specifications

Table 41 NFET gate driver

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.GD#1	GD_VGS	Gate to source overdrive during ON condition	4.5		10.5	V	NFET driver is ON
SID.PD.GD#3	GD_VGS_OFF	External-FET gate to source during OFF condition	-VBUS_NGDO_ABS		+VBUS_NGDO_ABS		External NFET must be able to tolerate “VGS < -VBUS_NGDO_ABS” in OFF state as the Gate is pulled-down to “0 V”
SID.PD.GD#11	ISB_VBUS_IN_NGDO	Leakage current from VBUS_IN_NGDO when NGDO is lowest power state (disabled)	–	–	70	µA	VBUS_IN_NGDO = 5 V; en_hv = 1, ngdo_en = 1, keepoff_dis = 1, cp_en = 0, gdrv_en = 0, en_g1_chrg = 0, equalizers-off
SID.PD.GD#11a	Ixres_VBUS_IN_NGDO	Leakage current from VBUS_IN_NGDO when chip XRES asserted			650		VBUS_IN_NGDO = 5 V; Chip XRES asserted; Guaranteed by design
SID.PD.GD#12	ISB_VBUS_OUT_NGDO	Leakage current from VBUS_OUT_NGDO when NGDO is lowest power state (disabled)			140		VBUS_OUT_NGDO = 5 V; en_hv = 1, ngdo_en = 1, keepoff_dis = 1, cp_en = 0, gdrv_en = 0, en_g1_chrg = 0, equalizers-off
SID.PD.GD#12a	Ixres_VBUS_OUT_NGDO	Leakage current from VBUS_OUT_NGDO when chip XRES asserted			500		VBUS_OUT_NGDO = 5 V; Chip XRES asserted; Guaranteed by design
SID.PD.ngdo_fet_sys.AC#2	Ton	NGDO turn-on time (VBUS_IN_NGDO = 5 V)		10	–	ms	Time taken for VBUS_CTRL_1 to rise from 0.5 to VBUS_IN_NGDO+1V with 3nF load cap
SID.PD.ngdo_fet_sys.AC#3	Toff	NGDO turn-off time (non-fault) (VBUS_IN_NGDO = 5 V)		7		µs	Time taken for VBUS_CTRL_1 to fall from VBUS_IN_NGDO+10 V to VBUS_OUT_NGDO (10 µF cap) with 3 nF load cap
SID.PD.ngdo_fet_sys.AC#4	Toff-fault	NGDO turn-off in response to SCP/RCP events (VBUS_IN_NGDO = 5 V)		1			NGDO turning off by VGS equalization of VBUS_CTRL_0 pin in response to RCP Event NGDO turning off by VBUS_CTRL_1 = 0.8 V for in response to SCP event

Table 42 CC-PHY PD specifications

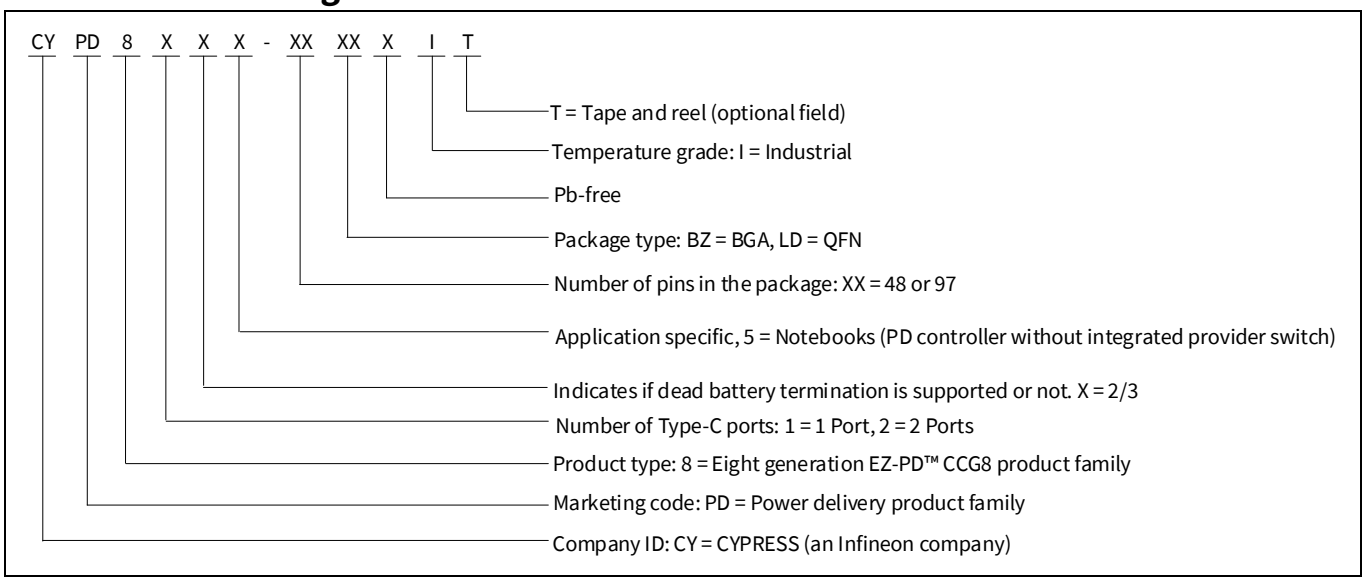
Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/conditions
SID.PD.cc_shvt. DC#1	vSwing	Transmitter output high voltage	1.05		1.2	V	–
SID.PD.cc_shvt. DC#2	vSwing_low	Transmitter output low voltage	–		0.075		
SID.PD.cc_shvt. DC#3	zDriver	Transmitter output impedance	33		75	Ω	
SID.PD.cc_shvt. DC#4	zBmcRx	Receiver input impedance	10		–	MΩ	Guaranteed by design
SID.PD.cc_shvt. DC#5	Idac_std	Source current for USB standard advertisement	64		96	µA	–
SID.PD.cc_shvt. DC#6	Idac_1p5a	Source current for 1.5A @ 5V advertisement	165.6		194.4		
SID.PD.cc_shvt. DC#7	Idac_3a	Source current for 3A @ 5V advertisement	303.6		356.4		
SID.PD.cc_shvt. DC#8	Rd	Pull down termination resistance when acting as upstream facing port (UFP)	4.59		5.61	kΩ	
SID.PD.cc_shvt. DC#9	Rd_db	Pull down termination resistance when acting as UFP, with dead battery (UFP)	4.08		6.12		
SID.PD.cc_shvt. DC#10	zOPEN	CC impedance to ground when disabled	108		–		
SID.PD.cc_shvt. DC#11	DFP_default_0p2	CC voltages on DFP side-Standard USB	0.15		0.25	V	
SID.PD.cc_shvt. DC#12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35		0.45		
SID.PD.cc_shvt. DC#13	DFP_3A_0p8	CC voltages on DFP side-3A	0.75		0.85		
SID.PD.cc_shvt. DC#14	DFP_3A_2p6		2.45		2.75		
SID.PD.cc_shvt. DC#15	UFP_default_0p66	CC voltages on UFP side-Standard USB	0.61		0.7		
SID.PD.cc_shvt. DC#16	UFP_1.5A_1p23	CC voltages on UFP side-1.5 A	1.16		1.31		
SID.PD.cc_shvt. DC#17	Vattach_ds	Deep sleep attach threshold	0.3		0.6	%	
SID.PD.cc_shvt. DC#18	Rattach_ds	Deep sleep pull-up resistor	10		50	kΩ	
SID.PD.cc_shvt. DC#19	VTX_step	TX drive voltage step size	80		120	mV	No for user and datasheet
SID.PD.cc_shvt. DC#30	FS_0p53	Voltage threshold for fast swap detect	0.49		0.58	V	–

7 Ordering information

Table 43 EZ-PD™ CCG8 ordering information

Product	Part number	Application	Type-C ports	Dead battery termination	Termination resistor	Role	Package
CCG8S	CYPD8125-48LDXI	Notebooks	1	Yes	Rp, Rd	DRP	48-pin QFN
	CYPD8125-48LDXIT						
CCG8D	CYPD8225-97BZXI		2				97-ball BGA
	CYPD8225-97BZXIT						

7.1 Ordering code definitions



8 Packaging

Table 44 Package characteristics

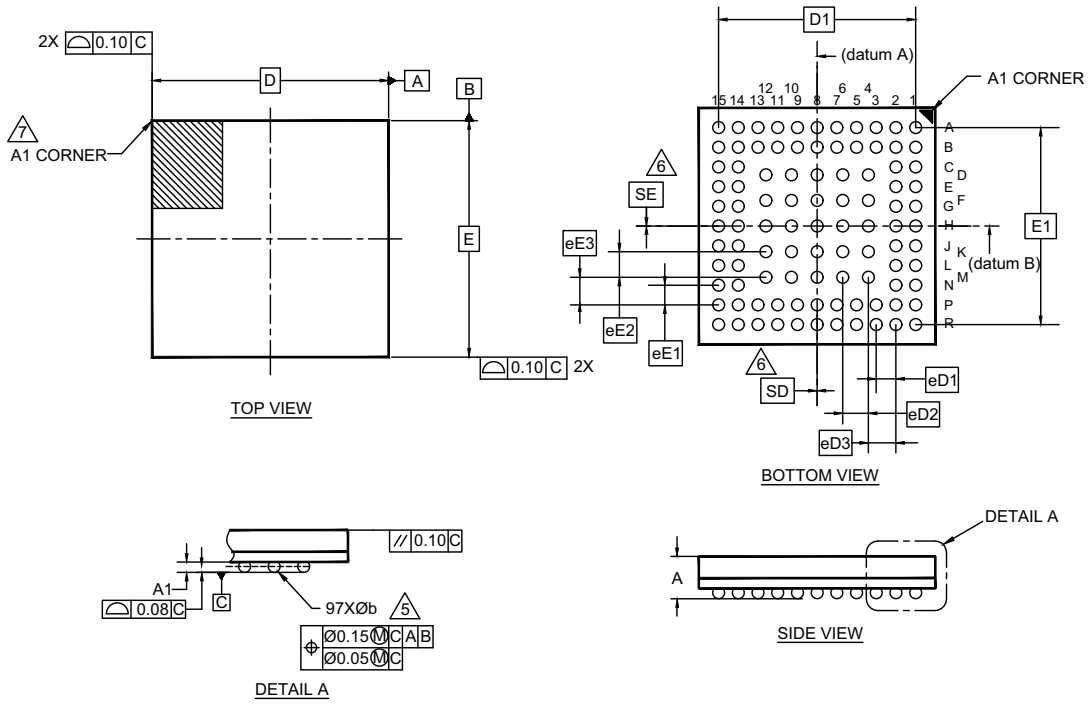
Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Industrial	-40	25	85	°C
T_J	Operating junction temperature				125	
T_{JA}	Package θ_{JA} (97-ball BGA)	–	–	42	–	°C/W
T_{JC}	Package θ_{JC} (97-ball BGA)			15.9		
T_{JA}	Package θ_{JA} (48-pin QFN)			16.6		
T_{JC}	Package θ_{JC} (48-pin QFN)			6.5		

Table 45 Solder reflow peak temperature

Package	Maximum peak temperature	Maximum time within 5°C of peak temperature
97-ball BGA	260°C	30 seconds
48-pin QFN		

Table 46 Package moisture sensitivity level (MSL), IPC/JEDEC J-STD-2

Package	MSL
97-ball BGA	MSL 3
48-pin QFN	



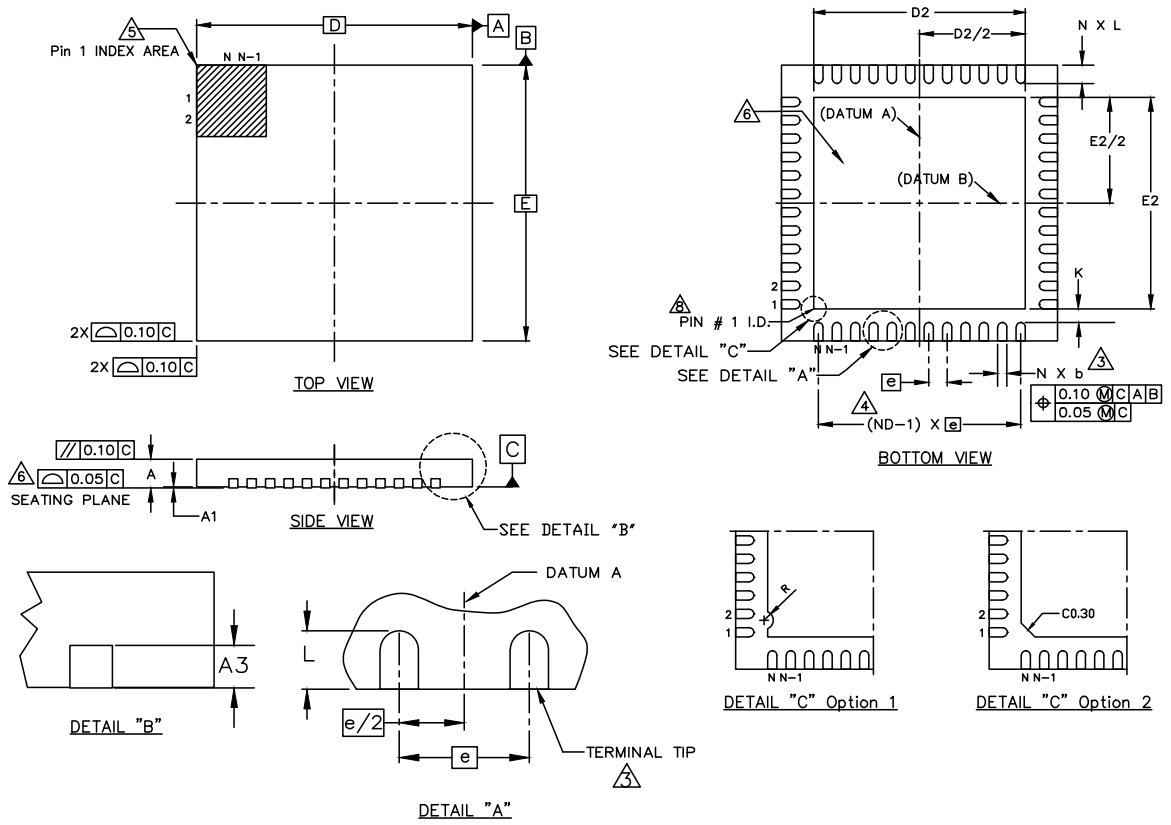
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.16	-	-
D	6.00 BSC		
E	6.00 BSC		
D1	5.00 BSC		
E1	5.00 BSC		
MD	11		
ME	11		
N	97		
Ø b	0.25	0.30	0.35
eD1	0.50 BSC		
eE1	0.50 BSC		
eD2	0.65 BSC		
eE2	0.65 BSC		
eD3	0.70 BSC		
eE3	0.70 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : MO-225.

002-31241 *A

Figure 11 97-ball BGA multi-pitch (6 × 6 × 0.5 mm/0.65mm), 6.0 x 6.0 x 1.0 mm package outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
e		0.40 BSC	
N		48	
ND		12	
L	0.30	0.40	0.50
b	0.15	0.20	0.25
D2	4.50	4.60	4.70
E2	4.50	4.60	4.70
D		6.00 BSC	
E		6.00 BSC	
A	-	-	0.60
A1	0.00	-	0.05
A3		0.152 REF	
R		0.20 TYP	
K		0.30 MIN	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. N IS THE TOTAL NUMBER OF TERMINALS.
3. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION "b" SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
4. ND REFERS TO THE NUMBER OF TERMINALS ON D SIDE.
5. PIN #1 ID ON TOP WILL BE LOCATED WITHIN THE INDICATED ZONE.
6. COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.
8. INDEX FEATURE CAN EITHER BE AN OPTION 1 : "MOUSE BITE" OR OPTION 2 : CHAMFER.

002-32392 *A

Figure 12 48L-QFN 6 mm × 6 mm × 0.6 mm package outline

9 Acronyms

Table 47 Acronyms used in this document

Acronym	Description
ADC	analog-to-digital converter
AES	advanced encryption standard
API	application programming interface
ARM	advanced RISC machine, a CPU architecture
BMC	Biphase Mark Code
CC	configuration channel
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
DFP	downstream facing port
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role port
ECC	Elliptic Curve Cryptography
EEPROM	electrically erasable programmable read-only memory
EMCA	electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FS	full-speed
GPIO	general-purpose input/output
HPD	hot plug detect
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
IOSS	input/output subsystem
I/O	input/output, see also GPIO
LDO	low-dropout regulator
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
MMIO	memory mapped input/output
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller
opamp	operational amplifier

Table 47 Acronyms used in this document *(continued)*

Acronym	Description
OCP	overcurrent protection
OVP	overvoltage protection
PASS	programmable analog sub system
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PWM	pulse-width modulator RAM
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RSA	Rivest Shamir Adleman
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCB	serial communication block
SCL	I2C serial clock
SDA	I2C serial data
S/H	sample and hold
SHA	secure hash algorithm
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TCPWM	timer/counter pulse-width modulator
Thunderbolt	Trademark of Intel
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
USB	Universal Serial Bus
USB-FS	USB Full-Speed
USBIO	USB input/output, CCG8 pins used to connect to a USB port
USB PD	USB Power Delivery
USBPD SS	USB PD subsystem
VDM	vendor defined messages
XRES	external reset I/O pin

10 Document conventions

10.1 Units of measure

Table 48 Units of measure

Symbol	Unit of measure
°C	degrees celsius
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
kHz	kilohertz
kΩ	kilo ohm
ksps	kilosamples per second
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Revision history

Document revision	Date	Description of changes
*F	2023-01-13	Release to web.
*G	2023-03-03	Added Software based Fast role swap (FRS) in **"Features"** on page 1 and added a note. Updated **"Gate drivers for VBUS NFETs"** on page 12. Added a note in **Figure 9** and **Figure 10**.

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