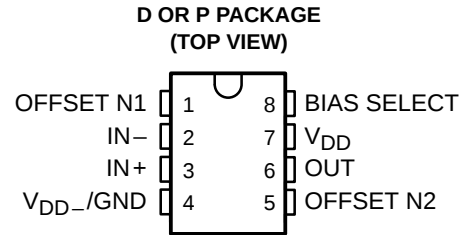


TLC251, TLC251A, TLC251B, TLC251Y LinCMOS™ PROGRAMMABLE LOW-POWER OPERATIONAL AMPLIFIERS

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- **Wide Range of Supply Voltages**
1.4-V to 16-V
- **True Single-Supply Operation**
- **Common-Mode Input Voltage Range**
Includes the Negative Rail
- **Low Noise . . . 30 nV/√Hz Typ at 1-kHz**
(High Bias)
- **ESD Protection Exceeds 2000 V Per**
MIL-STD-883C, Method 3015.1



symbol

description

The TLC251C, TLC251AC, and TLC251BC are low-cost, low-power programmable operational amplifiers designed to operate with single or dual supplies. Unlike traditional metal-gate CMOS operational amplifiers, these devices utilize Texas Instruments silicon-gate LinCMOS™ process, giving them stable input offset voltages without sacrificing the advantages of metal-gate CMOS.

This series of parts is available in selected grades of input offset voltage and can be nulled with one external potentiometer. Because the input common-mode range extends to the negative rail and the power consumption is extremely low, this family is ideally suited for battery-powered or energy-conserving applications. A bias-select pin can be used to program one of three ac performance and power-dissipation levels to suit the application. The series features operation down to a 1.4-V supply and is stable at unity gain.

These devices have internal electrostatic-discharge (ESD) protection circuits that prevent catastrophic failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling these devices as exposure to ESD may result in a degradation of the device parametric performance.

Because of the extremely high input impedance and low input bias and offset currents, applications for the TLC251C series include many areas that have previously been limited to BIFET and NFET product types. Any circuit using high-impedance elements and requiring small offset errors is a good candidate for cost-effective use of these devices. Many features associated with bipolar technology are available with LinCMOS™ operational amplifiers without the power penalties of traditional bipolar devices. Remote and inaccessible equipment applications are possible using the low-voltage and low-power capabilities of the TLC251C series.

In addition, by driving the bias-select input with a logic signal from a microprocessor, these operational amplifiers can have software-controlled performance and power consumption. The TLC251C series is well suited to solve the difficult problems associated with single battery and solar cell-powered applications.

The TLC251C series is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T _A	V _{IOmax} AT 25°C	PACKAGED DEVICES		CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	
0°C to 70°C	10 mV	TLC251CD	TLC251CP	TLC251Y
	5 mV	TLC251ACD	TLC251ACP	—
	2 mV	TLC251BCD	TLC251BCP	—

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLC251CDR). Chips are tested at 25°C.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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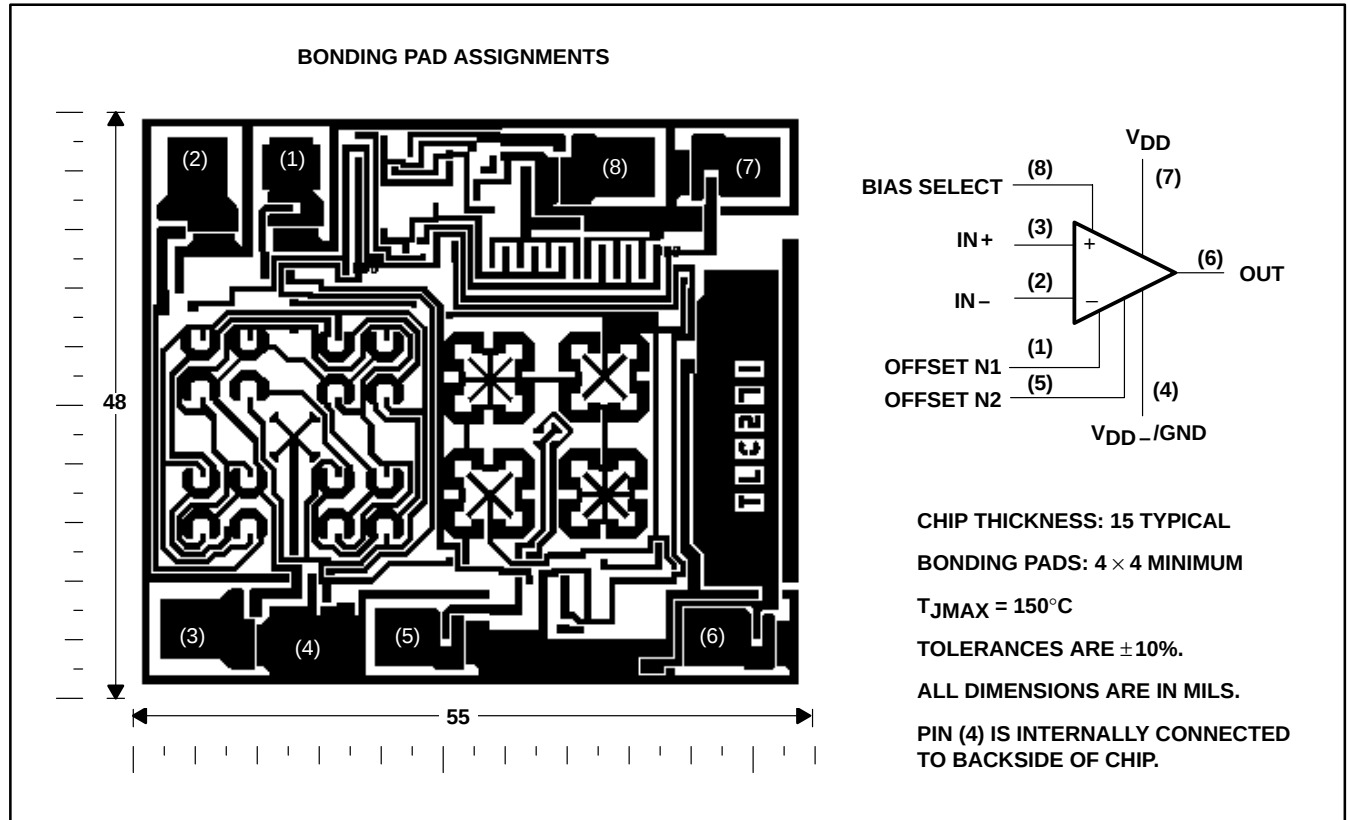
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The schematic diagram illustrates a fully differential, low offset, low noise, and low power op-amp. The circuit is powered by V_{DD} (pin 7) and V_{DD}/GND (pin 4). The input stage consists of a differential pair of NMOS transistors, each with an ESD-Protective Network (pins 3 and 2). The gates of these transistors are biased by a current control block (pin 8, BIAS SELECT) and an ESD-Protective Network. The output stage consists of a differential pair of PMOS transistors, each with an ESD-Protective Network. The gates of these transistors are biased by a current control block (pin 8, BIAS SELECT) and an ESD-Protective Network. The output is taken from a differential pair of PMOS transistors (pins 6 and 6, OUT). The circuit also includes an offset input (OFFSET N1, pin 1) and a bias select input (BIAS SELECT, pin 8).

TLC251Y chip information

These chips, properly assembled, display characteristics similar to the TLC251C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{DD} (see Note 1)	18 V
Differential input voltage, V_{ID} (see Note 2)	± 18 V
Input voltage range, V_I (any input)	-0.3 V to 18 V
Duration of short circuit at (or below) 25°C free-air temperature (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}/GND .
2. Differential voltages are at $IN+$ with respect to $IN-$.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		1.4	16	V
Common-mode input voltage, V_{IC}	$V_{DD} = 1.4$ V	0	0.2	V
	$V_{DD} = 5$ V	-0.2	4	
	$V_{DD} = 10$ V	-0.2	9	
	$V_{DD} = 16$ V	-0.2	14	
Operating free-air temperature, T_A		0	70	°C
Bias-select voltage		See Application Information		



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HIGH-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T _A [†]	TLC251C, TLC251AC, TLC251BC						UNIT
				V _{DD} = 5 V			V _{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _O = 1.4 V, V _{IC} = 0 V, R _S = 50 Ω, R _L = 10 kΩ	25°C	1.1		10	1.1		10	mV
			Full range			12			12	
			25°C	0.9		5	0.9		5	
			Full range			6.5			6.5	
			25°C	0.34		2	0.39		2	
			Full range			3			3	
α _{VIO}	Average temperature coefficient of input offset voltage		25°C to 70°C	1.8			2		μV/°C	
I _{IO}	Input offset current (see Note 4)	V _O = V _{DD} /2, V _{IC} = V _{DD} /2	25°C	0.1		60	0.1		60	pA
			70°C	7		300	7		300	
I _{IB}	Input bias current (see Note 4)	V _O = V _{DD} /2, V _{IC} = V _{DD} /2	25°C	0.6		60	0.7		60	pA
			70°C	40		600	50		600	
V _{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2	V	
			Full range	−0.2 to 3.5			−0.2 to 8.5		V	
V _{OH}	High-level output voltage	V _{ID} = 100 mV, R _L = 10 kΩ	25°C	3.2	3.8		8	8.5	V	
			0°C	3	3.8		7.8	8.5		
			70°C	3	3.8		7.8	8.4		
V _{OL}	Low-level output voltage	V _{ID} = −100 mV, I _{OL} = 0	25°C	0		50	0		50	mV
			0°C	0		50	0		50	
			70°C	0		50	0		50	
A _{VD}	Large-signal differential voltage amplification	R _L = 10 kΩ, See Note 6	25°C	5	23		10	36	V/mV	
			0°C	4	27		7.5	42		
			70°C	4	20		7.5	32		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin}	25°C	65	80		65	85	dB	
			0°C	60	84		60	88		
			70°C	60	85		60	88		
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 5 V to 10 V, V _O = 1.4 V	25°C	65	95		65	95	dB	
			0°C	60	94		60	94		
			70°C	60	96		60	96		
I _{I(SEL)}	Input current (BIAS SELECT)	V _{I(SEL)} = 0	25°C	−1.4			−1.9		μA	
I _{DD}	Supply current	V _O = V _{DD} /2, V _{IC} = V _{DD} /2, No load	25°C	675	1600		950	2000	μA	
			0°C	775	1800		1125	2200		
			70°C	575	1300		750	1700		

[†] Full range is 0°C to 70°C.

- NOTES:
- The typical values of input bias current and input offset current below 5 pA were determined mathematically.
 - This range also applies to each input individually.
 - At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.



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HIGH-BIAS MODE

operating characteristics, $V_{DD} = 5\text{ V}$

PARAMETER		TEST CONDITIONS		T _A	TLC251C, TLC251AC, TLC251BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R _L = 10 kΩ, C _L = 20 pF	V _{I(PP)} = 1 V	25°C	3.6		V/μs	
				0°C	4			
				70°C	3			
			V _{I(PP)} = 2.5 V	25°C	2.9			
				0°C	3.1			
				70°C	2.5			
V _n	Equivalent input noise voltage	f = 1 kHz, R _S = 20 Ω		25°C	25		nV/√Hz	
B _{OM}	Maximum output-swing bandwidth	V _O = V _{OH} , C _L = 20 pF, R _L = 10 kΩ		25°C	320		kHz	
				0°C	340			
				70°C	260			
B ₁	Unity-gain bandwidth	V _I = 10 mV, C _L = 20 pF		25°C	1.7		MHz	
				0°C	2			
				70°C	1.3			
φ _m	Phase margin	V _I = 10 mV, f = B ₁ , C _L = 20 pF		25°C	46°			
				0°C	47°			
				70°C	44°			

operating characteristics, $V_{DD} = 10\text{ V}$

PARAMETER		TEST CONDITIONS		T _A	TLC251C, TLC251AC, TLC251BC			UNIT
					MIN	TYP	MAX	
SR	Slew rate at unity gain	R _L = 10 kΩ, C _L = 20 pF	V _{I(PP)} = 1 V	25°C	5.3		V/μs	
				0°C	5.9			
				70°C	4.3			
			V _{I(PP)} = 5.5 V	25°C	4.6			
				0°C	5.1			
				70°C	3.8			
V _n	Equivalent input noise voltage	f = 1 kHz, R _S = 20 Ω		25°C	25		nV/√Hz	
B _{OM}	Maximum output-swing bandwidth	V _O = V _{OH} , C _L = 20 pF, R _L = 10 kΩ		25°C	200		kHz	
				0°C	220			
				70°C	140			
B ₁	Unity-gain bandwidth	V _I = 10 mV, C _L = 20 pF		25°C	2.2		MHz	
				0°C	2.5			
				70°C	1.8			
φ _m	Phase margin	V _I = 10 mV, f = B ₁ , C _L = 20 pF		25°C	49°			
				0°C	50°			
				70°C	46°			



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MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T _A [†]	TLC251C, TLC251AC, TLC251BC						UNIT
				V _{DD} = 5 V			V _{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _O = 1.4 V, V _{IC} = 0 V, R _S = 50 Ω, R _L = 10 kΩ	25°C	1.1		10	1.1		10	mV
			Full range			12			12	
			25°C	0.9		5	0.9		5	
			Full range			6.5			6.5	
			25°C	0.34		2	0.39		2	
			Full range			3			3	
α _{VIO}	Average temperature coefficient of input offset voltage		25°C to 70°C	1.7			2.1		μV/°C	
I _{IO}	Input offset current (see Note 4)	V _O = V _{DD} /2, V _{IC} = V _{DD} /2	25°C	0.1		60	0.1		60	pA
			70°C	7		300	7		300	
I _{IB}	Input bias current (see Note 4)	V _O = V _{DD} /2, V _{IC} = V _{DD} /2	25°C	0.6		60	0.7		60	pA
			70°C	40		600	50		600	
V _{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2	V	
			Full range	−0.2 to 3.5			−0.2 to 8.5		V	
V _{OH}	High-level output voltage	V _{ID} = 100 mV, R _L = 10 kΩ	25°C	3.2	3.9		8	8.7	V	
			0°C	3	3.9		7.8	8.7		
			70°C	3	4		7.8	8.7		
V _{OL}	Low-level output voltage	V _{ID} = −100 mV, I _{OL} = 0	25°C	0		50	0		50	mV
			0°C	0		50	0		50	
			70°C	0		50	0		50	
A _{VD}	Large-signal differential voltage amplification	R _L = 10 kΩ, See Note 6	25°C	25	170		25	275	V/mV	
			0°C	15	200		15	320		
			70°C	15	140		15	230		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin}	25°C	65	91		65	94	dB	
			0°C	60	91		60	94		
			70°C	60	92		60	94		
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 5 V to 10 V, V _O = 1.4 V	25°C	70	93		70	93	dB	
			0°C	60	92		60	92		
			70°C	60	94		60	94		
I _{I(SEL)}	Input current (BIAS SELECT)	V _{I(SEL)} = V _{DD} /2	25°C	−130			−160		nA	
I _{DD}	Supply current	V _O = V _{DD} /2, V _{IC} = V _{DD} /2, No load	25°C	105		280	143		300	μA
			0°C	125		320	173		400	
			70°C	85		220	110		280	

[†] Full range is 0°C to 70°C.

- NOTES:
- The typical values of input bias current and input offset current below 5 pA were determined mathematically.
 - This range also applies to each input individually.
 - At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.



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MEDIUM-BIAS MODE

operating characteristics, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC251C, TLC251AC, TLC251BC			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 100\text{ k}\Omega$, $C_L = 20\text{ pF}$	$V_{I(PP)} = 1\text{ V}$	25°C		0.43		V/ μ s
			0°C		0.46		
			70°C		0.36		
		$V_{I(PP)} = 2.5\text{ V}$	25°C		0.40		
			0°C		0.43		
			70°C		0.34		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, $R_S = 20\text{ }\Omega$		25°C		32		nV/ $\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $C_L = 20\text{ pF}$, $R_L = 100\text{ k}\Omega$		25°C		55		kHz
			0°C		60		
			70°C		50		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$		25°C		525		kHz
			0°C		600		
			70°C		400		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $f = B_1$, $C_L = 20\text{ pF}$		25°C		40°		
			0°C		41°		
			70°C		39°		

operating characteristics, $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC251C, TLC251AC, TLC251BC			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 100\text{ k}\Omega$, $C_L = 20\text{ pF}$	$V_{I(PP)} = 1\text{ V}$	25°C		0.62		V/ μ s
			0°C		0.67		
			70°C		0.51		
		$V_{I(PP)} = 5.5\text{ V}$	25°C		0.56		
			0°C		0.61		
			70°C		0.46		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, $R_S = 20\text{ }\Omega$		25°C		32		nV/ $\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $C_L = 20\text{ pF}$, $R_L = 100\text{ k}\Omega$		25°C		35		kHz
			0°C		40		
			70°C		30		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$		25°C		635		kHz
			0°C		710		
			70°C		510		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $f = B_1$, $C_L = 20\text{ pF}$		25°C		43°		
			0°C		44°		
			70°C		42°		



LOW-BIAS MODE

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS	T _A [†]	TLC251C, TLC251AC, TLC251BC						UNIT
				V _{DD} = 5 V			V _{DD} = 10 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _O = 1.4 V, V _{IC} = 0 V, R _S = 50 Ω, R _L = 10 MΩ	25°C	1.1		10	1.1		10	mV
			Full range			12			12	
			25°C	0.9		5	0.9		5	
			Full range			6.5			6.5	
			25°C	0.24		2	0.26		2	
			Full range			3			3	
α _{VIO}	Average temperature coefficient of input offset voltage		25°C to 70°C	1.1			1			μV/°C
I _{IO}	Input offset current (see Note 4)	V _O = V _{DD} /2, V _{IC} = V _{DD} /2	25°C	0.1		60	0.1		60	pA
			70°C	7		300	7		300	
I _{IB}	Input bias current (see Note 4)	V _O = V _{DD} /2, V _{IC} = V _{DD} /2	25°C	0.6		60	0.7		60	pA
			70°C	40		600	50		600	
V _{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 4	−0.3 to 4.2		−0.2 to 9	−0.3 to 9.2		V
			Full range	−0.2 to 3.5			−0.2 to 8.5			V
V _{OH}	High-level output voltage	V _{ID} = 100 mV, R _L = 1 MΩ	25°C	3.2	4.1		8	8.9		V
			0°C	3	4.1		7.8	8.9		
			70°C	3	4.2		7.8	8.9		
V _{OL}	Low-level output voltage	V _{ID} = −100 mV, I _{OL} = 0	25°C	0		50	0		50	mV
			0°C	0		50	0		50	
			70°C	0		50	0		50	
A _{VD}	Large-signal differential voltage amplification	R _L = 1 MΩ, See Note 6	25°C	50	520		50	870		V/mV
			0°C	50	700		50	1030		
			70°C	50	380		50	660		
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin}	25°C	65	94		65	97		dB
			0°C	60	95		60	97		
			70°C	60	95		60	97		
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 5 V to 10 V, V _O = 1.4 V	25°C	70	97		70	97		dB
			0°C	60	97		60	97		
			70°C	60	98		60	98		
I _{I(SEL)}	Input current (BIAS SELECT)	V _{I(SEL)} = V _{DD}	25°C	65			95			nA
I _{DD}	Supply current	V _O = V _{DD} /2, V _{IC} = V _{DD} /2, No load	25°C	10		17	14		23	μA
			0°C	12		21	18		33	
			70°C	8		14	11		20	

[†] Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 10 V, V_O = 1 V to 6 V.

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LOW-BIAS MODE

operating characteristics, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC251C, TLC251AC, TLC251BC			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$	$V_{I(PP)} = 1\text{ V}$	25°C		0.03		V/ μ s
			0°C		0.04		
			70°C		0.03		
		$V_{I(PP)} = 2.5\text{ V}$	25°C		0.03		
			0°C		0.03		
			70°C		0.02		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, $R_S = 20\text{ }\Omega$		25°C		68		nV/ $\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $C_L = 20\text{ pF}$, $R_L = 1\text{ M}\Omega$		25°C		5		kHz
			0°C		6		
			70°C		4.5		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$		25°C		85		kHz
			0°C		100		
			70°C		65		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $f = B_1$, $C_L = 20\text{ pF}$		25°C		34°		
			0°C		36°		
			70°C		30°		

operating characteristics, $V_{DD} = 10\text{ V}$

PARAMETER	TEST CONDITIONS		T_A	TLC251C, TLC251AC, TLC251BC			UNIT
				MIN	TYP	MAX	
SR Slew rate at unity gain	$R_L = 1\text{ M}\Omega$, $C_L = 20\text{ pF}$	$V_{I(PP)} = 1\text{ V}$	25°C		0.05		V/ μ s
			0°C		0.05		
			70°C		0.04		
		$V_{I(PP)} = 5.5\text{ V}$	25°C		0.04		
			0°C		0.05		
			70°C		0.04		
V_n Equivalent input noise voltage	$f = 1\text{ kHz}$, $R_S = 20\text{ }\Omega$		25°C		68		nV/ $\sqrt{\text{Hz}}$
B_{OM} Maximum output-swing bandwidth	$V_O = V_{OH}$, $C_L = 20\text{ pF}$, $R_L = 1\text{ M}\Omega$		25°C		1		kHz
			0°C		1.3		
			70°C		0.9		
B_1 Unity-gain bandwidth	$V_I = 10\text{ mV}$, $C_L = 20\text{ pF}$		25°C		110		kHz
			0°C		125		
			70°C		90		
ϕ_m Phase margin	$V_I = 10\text{ mV}$, $f = B_1$, $C_L = 20\text{ pF}$		25°C		38°		
			0°C		40°		
			70°C		34°		



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electrical characteristics at specified free-air temperature, $V_{DD} = 1.4\text{ V}$

PARAMETER		TEST CONDITIONS†	TA‡	BIAS	TLC251C, TLC251AC, TLC251BC			UNIT
					MIN	TYP	MAX	
VIO	Input offset voltage	TLC251C	VO = 0.2 V, RS = 50 Ω	25°C	Any	10		mV
		Full range		12				
		TLC251AC	25°C	Any	5			
		Full range	6.5					
		TLC251BC	25°C	Any	2			
			Full range		3			
αVIO	Average temperature coefficient of input offset voltage		25°C to 70°C	Any	1		μV/°C	
IIO	Input offset current	VO = 0.2 V	25°C	Any	1	60	pA	
			Full range		300			
IIB	Input bias current	VO = 0.2 V	25°C	Any	1	60	pA	
			Full range		600			
VICR	Common-mode input voltage range		25°C	Any	0 to 0.2		V	
VOM	Peak output voltage swing§	VID = 100 mV	25°C	Any	450	700	mV	
AVD	Large-signal differential voltage amplification	VO = 100 to 300 mV, RS = 50 Ω	25°C	Low	20			
				High	10			
CMRR	Common-mode rejection ratio	RS = 50 Ω, VIC = VICRmin, VO = 0.2 V	25°C	Any	60	77	dB	
IDD	Supply current	VO = 0.2 V, No load	25°C	Low	5	17	μA	
				High	150	190		

[†] All characteristics are measured under open-loop conditions with zero common-mode input voltage unless otherwise specified. Unless otherwise noted, an output load resistor is connected from the output to ground and has the following values: for low bias, $R_L = 1\text{ M}\Omega$, for medium bias, $R_L = 100\text{ k}\Omega$, and for high bias, $R_L = 10\text{ k}\Omega$.

[‡] Full range is 0°C to 70°C.

[§] The output swings to the potential of V_{DD-}/GND .

operating characteristics, $V_{DD} = 1.4\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	BIAS	TLC251C, TLC251AC, TLC251BC			UNIT
				MIN	TYP	MAX	
B ₁	Unity-gain bandwidth	C _L = 100 pF	Low	12			kHz
			High	12			
SR	Slew rate at unity gain	See Figure 1	Low	0.001			V/μs
			High	0.1			
	Overshoot factor	See Figure 1	Low	35%			
			High	30%			



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electrical characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TLC251Y									UNIT
			HIGH-BIAS MODE			MEDIUM-BIAS MODE			LOW-BIAS MODE			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V _{IO}	Input offset voltage	V _O = 1.4 V, V _{IC} = 0 V, R _S = 50 Ω, R _L [†]		1.1	10		1.1	10		1.1	10	mV
α _{VIO}	Average temperature coefficient of input offset voltage			1.8			1.7			1.1		μV/°C
I _{IO}	Input offset current (see Note 4)	V _O = V _{DD} /2, V _{IC} = V _{DD} /2		0.1	60		0.1	60		0.1	60	pA
I _{IB}	Input bias current (see Note 4)	V _O = V _{DD} /2, V _{IC} = V _{DD} /2		0.6	60		0.6	60		0.6	60	pA
V _{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		−0.2 to 4	−0.3 to 4.2		V
V _{OH}	High-level output voltage	V _{ID} = 100 mV, R _L [†]	3.2	3.8		3.2	3.9		3.2	4.1		V
V _{OL}	Low-level output voltage	V _{ID} = −100 mV, I _{OL} = 0		0	50		0	50		0	50	mV
A _{VD}	Large-signal differential voltage amplification	V _O = 0.25 V, R _L [†]	5	23		25	170		50	480		V/mV
CMRR	Common-mode rejection ratio	V _{IC} = V _{ICRmin}	65	80		65	91		65	94		dB
k _{SVR}	Supply-voltage rejection ratio (ΔV _{DD} /ΔV _{IO})	V _{DD} = 5 V to 10 V, V _O = 1.4 V	65	95		70	93		70	97		dB
I _{I(SEL)}	Input current (BIAS SELECT)	V _{I(SEL)} = V _{DD} /2		−1.4			−0.13			0.065		μA
I _{DD}	Supply current	V _O = V _{DD} /2, V _{IC} = V _{DD} /2, No load		675	1600		105	280		10	17	μA

† For high-bias mode, $R_L = 10\text{ k}\Omega$; for medium-bias mode, $R_L = 100\text{ k}\Omega$; and for low-bias mode, $R_L = 1\text{ M}\Omega$.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

operating characteristics, $V_{DD} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TLC251Y									UNIT
				HIGH-BIAS MODE			MEDIUM-BIAS MODE			LOW-BIAS MODE			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	$R_L^\dagger$, $C_L = 20\text{ pF}$	$V_{I(PP)} = 1\text{ V}$	3.6			0.43			0.03			V/ μs
			$V_{I(PP)} = 2.5\text{ V}$	2.9			0.40			0.03			
V_n	Equivalent input noise voltage	$f = 1\text{ kHz}$,	$R_S = 20\text{ }\Omega$	25			32			68			nV/ $\sqrt{\text{Hz}}$
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, $R_L = 10\text{ k}\Omega$	$C_L = 20\text{ pF}$,	320			55			4.5			kHz
B_1	Unity-gain bandwidth	$V_I = 10\text{ mV}$,	$C_L = 20\text{ pF}$	1700			525			65			kHz
ϕ_m	Phase margin	$f = B_1$, $C_L = 20\text{ pF}$	$V_I = 10\text{ mV}$,	46°			40°			34°			

[†] For high-bias mode, $R_L = 10\text{ k}\Omega$; for medium-bias mode, $R_L = 100\text{ k}\Omega$; and for low-bias mode, $R_L = 1\text{ M}\Omega$.

PARAMETER MEASUREMENT INFORMATION

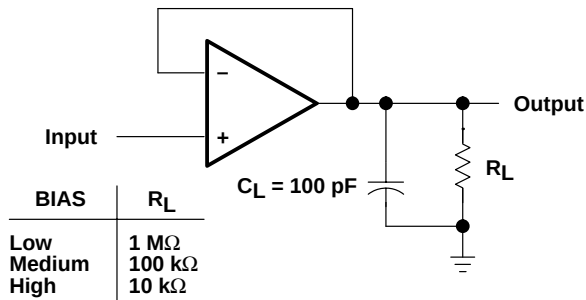


Figure 1. Unity-Gain Amplifier

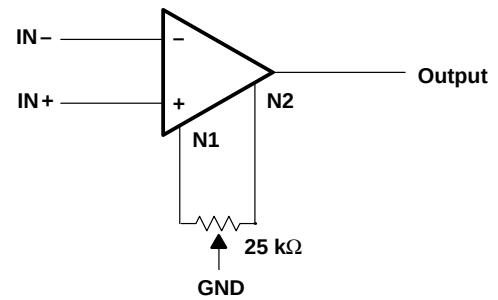


Figure 2. Input Offset Voltage Null Circuit

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
I_{DD}	Supply current	vs Bias-select voltage	3
		vs Supply voltage	4
		vs Free-air temperature	5
A_{VD}	Large-signal differential voltage amplification	Low bias vs Frequency	6
		Medium bias vs Frequency	7
		High bias vs Frequency	8
	Phase shift	Low bias vs Frequency	6
		Medium bias vs Frequency	7
		High bias vs Frequency	8

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TYPICAL CHARACTERISTICS

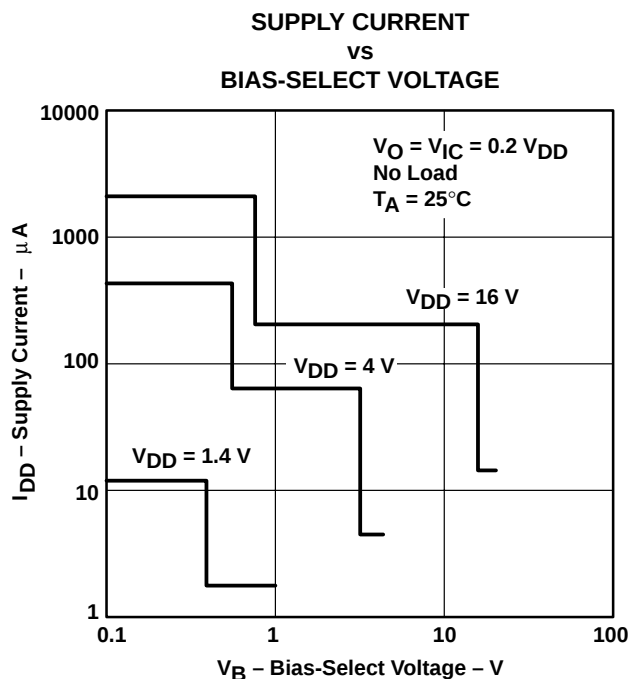


Figure 3

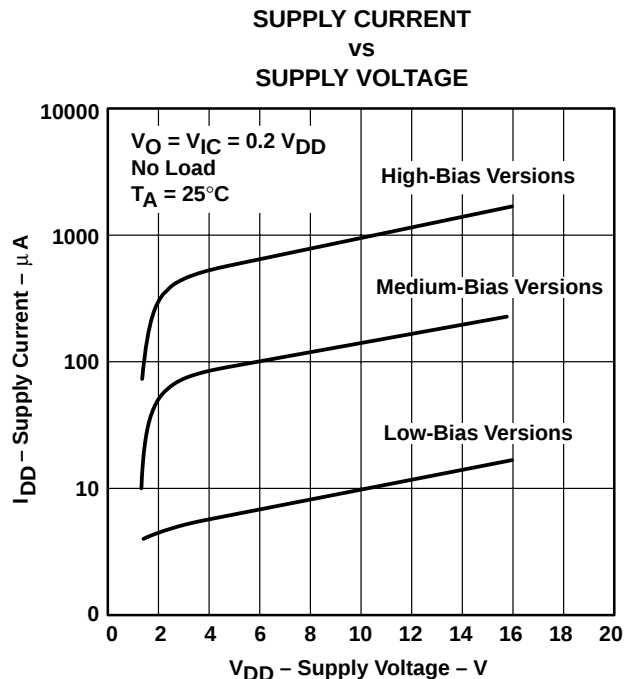


Figure 4

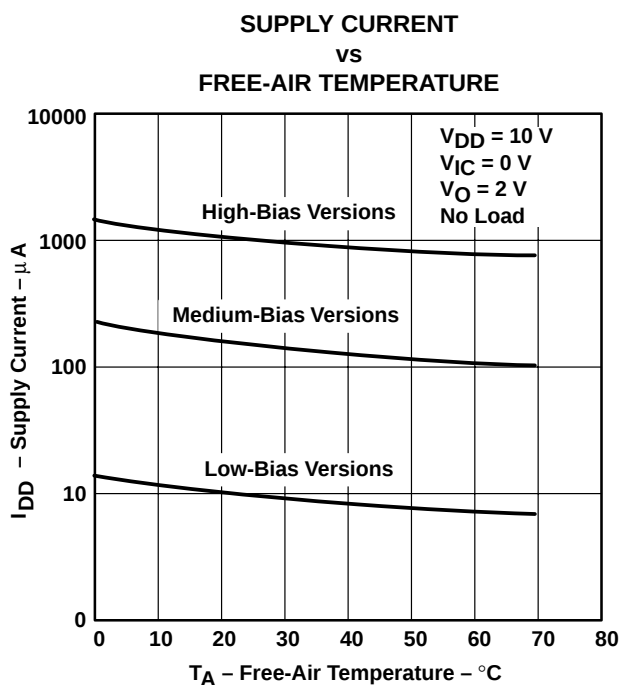


Figure 5

TYPICAL CHARACTERISTICS

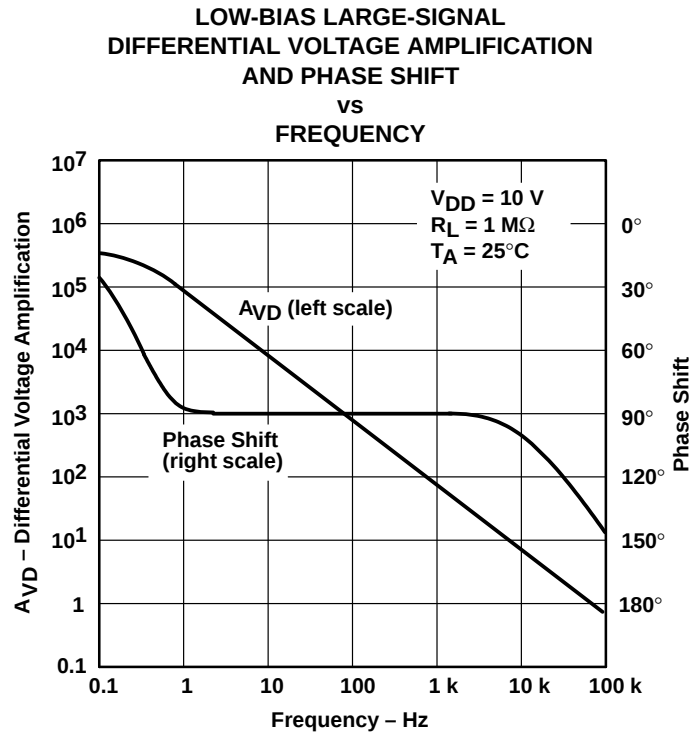


Figure 6

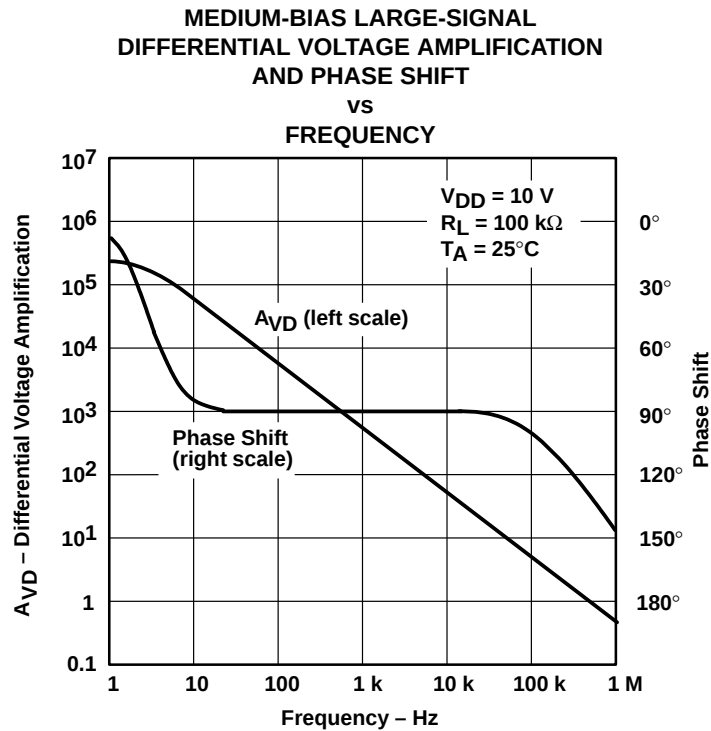


Figure 7

TYPICAL CHARACTERISTICS

HIGH-BIAS LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
AND PHASE SHIFT
VS
FREQUENCY

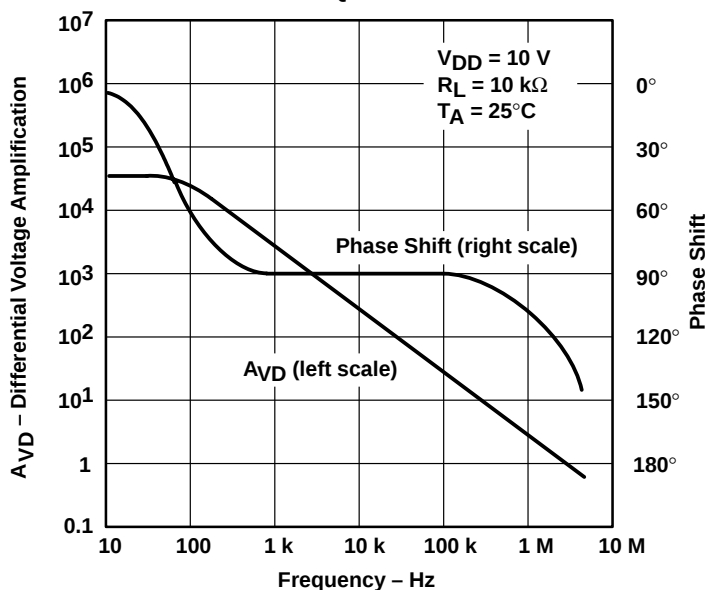


Figure 8

APPLICATION INFORMATION

latch-up avoidance

Junction-isolated CMOS circuits have an inherent parasitic PNP structure that can function as an SCR. Under certain conditions, this SCR may be triggered into a low-impedance state, resulting in excessive supply current. To avoid such conditions, no voltage greater than 0.3 V beyond the supply rails should be applied to any pin. In general, the operational amplifier supplies should be applied simultaneously with, or before, application of any input signals.

APPLICATION INFORMATION

using BIAS SELECT

The TLC251 has a terminal called BIAS SELECT that allows the selection of one of three I_{DD} conditions (10, 150, and 1000 μA typical). This allows the user to trade-off power and ac performance. As shown in the typical supply current (I_{DD}) versus supply voltage (V_{DD}) curves (Figure 4), the I_{DD} varies only slightly from 4 V to 16 V. Below 4 V, the I_{DD} varies more significantly. Note that the I_{DD} values in the medium- and low-bias modes at $V_{DD} = 1.4$ V are typically 2 μA , and in the high mode are typically 12 μA . The following table shows the recommended BIAS SELECT connections at $V_{DD} = 10$ V.

BIAS MODE	AC PERFORMANCE	BIAS SELECT CONNECTION [†]	TYPICAL I_{DD} [‡]
Low	Low	V_{DD}	10 μA
Medium	Medium	0.8 V to 9.2 V	150 μA
High	High	Ground pin	1000 μA

[†] Bias selection may also be controlled by external circuitry to conserve power, etc. For information regarding BIAS SELECT, see Figure 3 in the typical characteristics curves.

[‡] For I_{DD} characteristics at voltages other than 10 V, see Figure 4 in the typical characteristics curves.

output stage considerations

The amplifier's output stage consists of a source-follower-connected pullup transistor and an open-drain pulldown transistor. The high-level output voltage (V_{OH}) is virtually independent of the I_{DD} selection and increases with higher values of V_{DD} and reduced output loading. The low-level output voltage (V_{OL}) decreases with reduced output current and higher input common-mode voltage. With no load, V_{OL} is essentially equal to the potential of V_{DD-}/GND .

input offset nulling

The TLC251C series offers external offset null control. Nulling may be achieved by adjusting a 25-k Ω potentiometer connected between the offset null terminals with the wiper connected to the device V_{DD-}/GND pin as shown in Figure 2. The amount of nulling range varies with the bias selection. At an I_{DD} setting of 1000 μA (high bias), the nulling range allows the maximum offset specified to be trimmed to zero. In low or medium bias or when the amplifier is used below 4 V, total nulling may not be possible for all units.

supply configurations

Even though the TLC251C series is characterized for single-supply operation, it can be used effectively in a split-supply configuration when the input common-mode voltage (V_{ICR}), output swing (V_{OL} and V_{OH}), and supply voltage limits are not exceeded.

circuit layout precautions

The user is cautioned that whenever extremely high circuit impedances are used, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup, as well as excessive dc leakages.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC251ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	251AC	
TLC251ACP	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC251ACP	
TLC251BCP	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC251BCP	
TLC251CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	251C	
TLC251CDR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	251C	
TLC251CP	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC251CP	
TLC251CPE4	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TLC251CP	

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC251CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

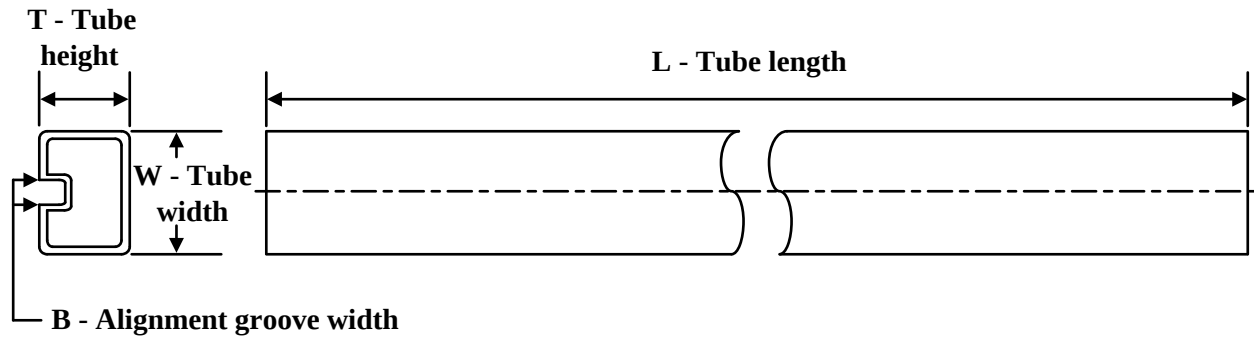
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC251CDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TLC251ACD	D	SOIC	8	75	505.46	6.76	3810	4
TLC251ACD	D	SOIC	8	75	507	8	3940	4.32
TLC251ACP	P	PDIP	8	50	506	13.97	11230	4.32
TLC251BCP	P	PDIP	8	50	506	13.97	11230	4.32
TLC251CD	D	SOIC	8	75	507	8	3940	4.32
TLC251CD	D	SOIC	8	75	505.46	6.76	3810	4
TLC251CP	P	PDIP	8	50	506	13.97	11230	4.32
TLC251CPE4	P	PDIP	8	50	506	13.97	11230	4.32

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