# MP7752

## 18V, 2x15W Stereo BTL, Fixed Frequency, Inductorless Class-D Audio Amplifier

The Future of Analog IC Technology

## DESCRIPTION

The MP7752 is an analog input inductorless class-D audio amplifier, which drives stereo speakers in bridge-tied-load configuration. It is a fully integrated audio amplifier, which reduces solution size dramatically. It integrates 240mΩ power MOSFETs and short-circuit protection circuits, and it features start-up/shutdown pop elimination and advanced EMI performance. Also, it is inductorless while passing the EMC test.

The MP7752 utilizes a stereo BTL structure capable of delivering 15W per channel into 8Ω speakers with a 16V power supply. MPS class-D audio amplifiers exhibit the high fidelity of class-AB amplifiers at high efficiency.

The MP7752 includes an internal circuit which allows the system to shut down automatically after the absence of the audio signal is detected. This feature is used for energy-using products and battery operated applications.

Also, it has an adjustable power limit function. The PLIMIT circuit sets a limit on the output peak-to-peak voltage. This is done by limiting the duty cycle to a fixed maximum value. This limit can be thought of as a "virtual" voltage rail, which is lower than the supply connected to PVCC.

The MP7752 is available in a TSSOP-28 EP package.

## FEATURES

- 5V to 18V Operation from a Single Supply
- ±5A Peak Current Output
- Output Power:
  9.5W/Channel at 12V, 8Ω Load, 10%THD
  15W/Channel at 16V, 8Ω Load, 10%THD
- 90% Efficiency with 8Ω Load, 10%THD, 1kHz, 12V Supply Voltage
- 240mΩ Power MOSFETs
- Start-UP/Shutdown Pop Elimination
- Short-Circuit Protection Circuits
- Inductorless Topology
- Advanced EMI performance
- All Switches Current Limited
- Internal Under-Voltage Protection
- Internal Thermal Protection
- TSSOP-28 EP Package
- Adjustable Power Limiter
- Automatic Shutdown with Zero Input Signal Detection
- Fault Output Flag

## APPLICATIONS

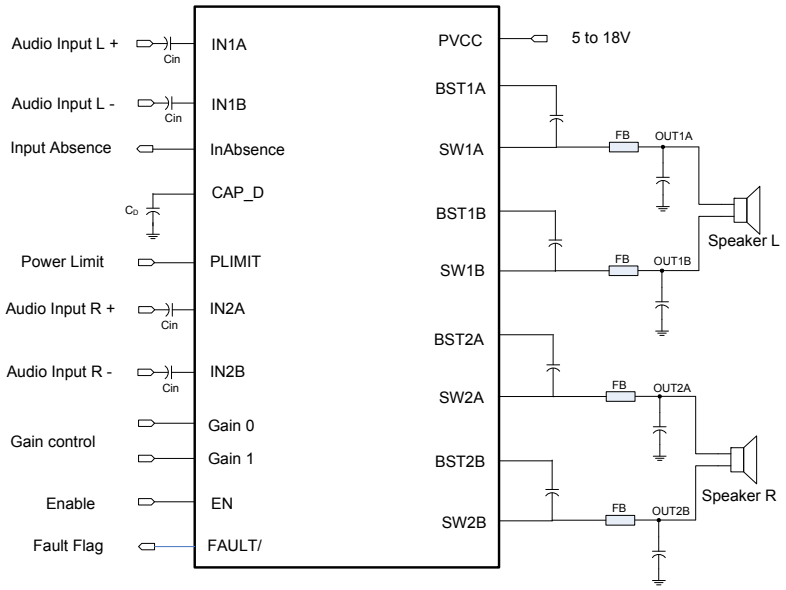
- TV
- DVD Receiver
- Active Speaker

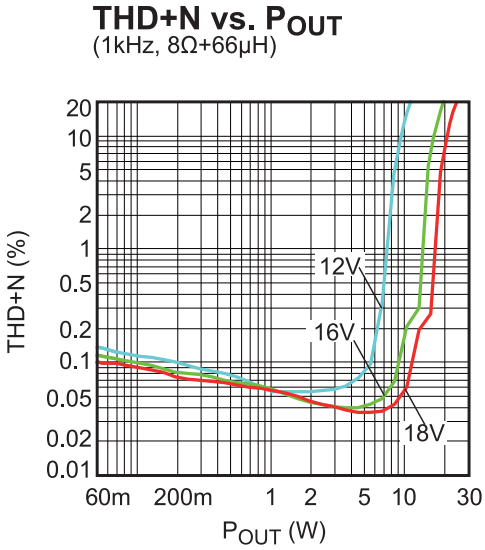
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# TYPICAL APPLICATION





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## ORDERING INFORMATION

| Part Number* | Package | Top Marking |
|---|---|---|
| MP7752GF | TSSOP-28 EP | *See Blow* |

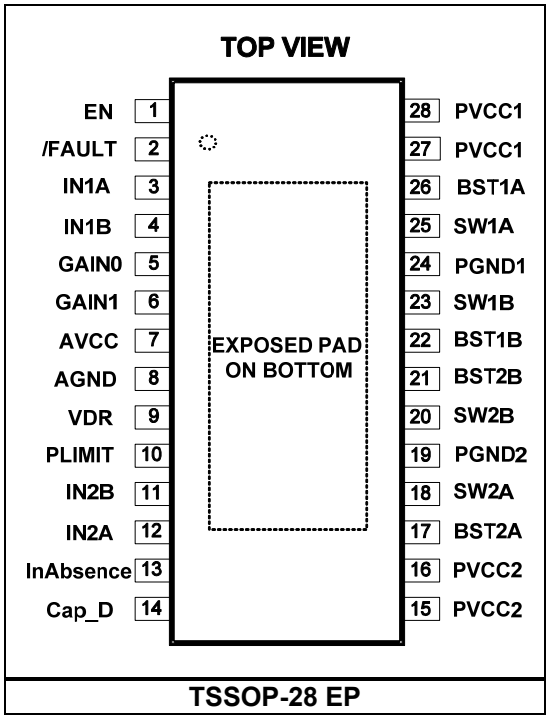
* For Tape & Reel, add suffix –Z (e.g. MP7752GF–Z)

## TOP MARKING

MPSYYWW
MP7752
LLLLLLLLL

MPS: MPS prefix:
YY: year code;
WW: week code:
MP7752: part number;
LLLLLLLLL: lot number;

## PACKAGE REFERENCE




TSSOP-28 EP


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## ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage $V_{CC}$ .....–0.3V to +20V
$V_{SW}$ ..... –1V to $V_{CC}$ + 1V
$V_{EN}$, $V_{/FAULT}$, $V_{GAIN}$, $V_{InAbsence}$ – 0.3V to $V_{CC}$ + 0.3V
BS Voltage $V_{BST}$ ..... $V_{SW}$ – 0.3V to $V_{SW}$ + 6V
$V_{PLIMIT}$ ..... – 0.3V to $V_{AVCC}$ + 0.3V
$V_{INXX}$ ..... – 0.3V to 6.5V
AGND to PGND .....–0.3V to +0.3V
Continuous Power Dissipation ($T_A$ = +25°C) (2)
……...3.9W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

## *Recommended Operating Conditions* (3)

Supply Voltage $V_{IN}$ .....5V to 18V
Operating Junction Temp. ($T_J$). -40°C to +125°C

## *Thermal Resistance* (4)

| | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| TSSOP-28 EP ……. …. ….. ….32 | 6 | °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX)-$T_A$)/$\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.


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## ELECTRICAL CHARACTERISTICS (5, 6)

**$V_{CC}$ = 18V, $V_{EN}$ = 5V, $T_J$ = -40°C to 125°C, unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Standby Current | $I_{QSTBY}$ | $V_{EN}$ = 0V,NIN=PIN=Float | | 130 | 200 | μA |
| Quiescent Current | $I_Q$ | $V_{EN}$ = 5V, no load, no LC filter | | 20 | 40 | mA |
| Output Offset Voltage | $V_{OS}$ | $V_I$ = 0 V, Gain = 36 dB, $T_j$ = 25°C | | 20 | 65 | mV |
| SW On Resistance | $R_{dsON}$ | $I_O$ = 500mA, $T_J$ = 25°C | | 0.24 | | Ω |
| Short Circuit Current | | Sourcing and Sinking, $T_J$ = 25°C | 4 | 5 | 6 | A |
| Closed Loop Gain | G | GAIN0 = L, GAIN1 = L | 19 | 20 | 21 | dB |
| | | GAIN0 = H, GAIN1 = L | 25 | 26 | 27 | |
| | | GAIN0 = L, GAIN1 = H | 31 | 32 | 33 | |
| | | GAIN0 = H, GAIN1 = H | 35 | 36 | 37 | |
| EN Enable Threshold Voltage | | $V_{EN}$ Rising | | 1.3 | 2.0 | V |
| | | $V_{EN}$ Falling | 0.4 | 0.9 | | V |
| EN Enable Input Current | | $V_{EN}$ = 5V | | 12 | 25 | μA |
| Under Voltage Protection | | $V_{UVP}$ Rising | | 4.6 | 5 | V |
| | | $V_{UVP}$ Falling | 4 | 4.3 | | V |
| AVCC Operating Voltage | | | 5 | 5.5 | 6 | V |
| VDR Operating Voltage | | | 5 | 5.5 | 6 | V |
| $V_{INN/INP}$ Common Mode Voltage | | | 2.3 | 2.5 | 2.7 | V |
| GAIN0/GAIN1 Threshold | | $V_{GAIN}$ Rising | | 1.6 | 2 | V |
| | | $V_{GAIN}$ Falling | 0.6 | 1.1 | | V |
| Turn-on Time | $t_{ON}$ | | | 13 | | ms |
| Turn-off Time | $t_{OFF}$ | | | 0.2 | | us |
| Switching frequency | | | 260 | 325 | 360 | kHz |
| Input signal absence sensitivity | | | 2 | 5 | 8 | mV |
| Thermal Shutdown Trip Point | | $T_J$ Rising | | 150 | | °C |
| Thermal Shutdown Hysteresis | | | | 20 | | °C |

**Notes:**

5) The device is not guaranteed to function outside its operating rating.

6) Electrical Characteristics are for the IC only with no external components except bypass capacitors.


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## OPERATING SPECIFICATIONS (7)

**Circuit of figure 5, $V_{CC}$ = 18V, Gain=20dB, $V_{EN}$ = 5V, $R_{LOAD}$ = 8Ω+66uH, $T_A$ = +25°C, unless otherwise noted.**

| Parameters | Symbol | Condition | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Power Output | | f = 1kHz, THD+N = 10%, $V_{CC}$ = 18V | | | 20 | | W |
| | | f = 1kHz, THD+N = 10%, $V_{CC}$ = 16V | | | 15 | | |
| | | f = 1kHz, THD+N = 10%, $V_{CC}$ = 12V | | | 9.5 | | |
| THD+ Noise | | $P_{OUT}$ = 5W, f = 1kHz, $V_{CC}$ = 12V | | | 0.5 | | % |
| | | $P_{OUT}$ = 15W, f = 1kHz, $V_{CC}$ = 18V | | | 0.5 | | % |
| Efficiency | | $P_{OUT}$ = 9.5W + 9.5W, THD+N = 10%, $V_{CC}$ = 12 V, 1kHz, $R_{LOAD}$ = 8Ω | | | 90 | | % |
| Deadtime | | $I_O$=0.5A | | | 40 | | nS |
| Cross Talk | | $V_O$ = 1 Vrms, f = 217Hz | | | -110 | | dB |
| Noise Floor | | A-Weighted, 22 Hz to 22 kHz | | | 115 | | μV |
| Signal-to-noise ratio | | f = 1kHz, THD+N = 1%, A-Weighted | | | 100 | | dB |
| Power Supply Rejection | | $V_{RIPPLE}$=300m$V_{PP}$, Inputs ac-coupled to AGND | f = 1kHz | | -60 | | dB |
| | | | f = 217Hz | | -70 | | dB |

**Notes:**

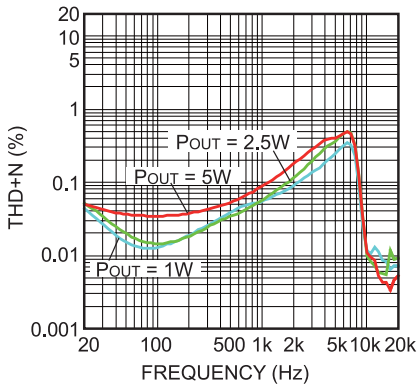
7) Operating Specifications are for the IC in Typical Application circuit. Not production tested.


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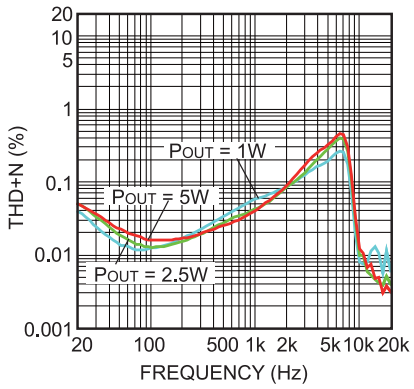
# TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{CC}$ = 12V, GAIN = 20dB, f = 1kHz, $T_A$ = 25°C, unless otherwise noted.**

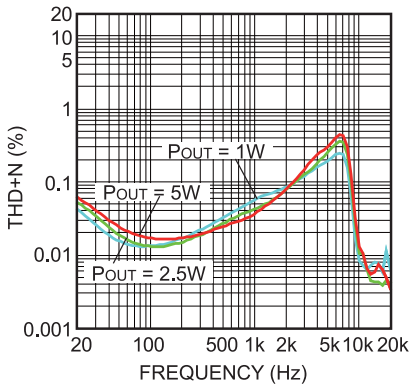
### THD+N vs. Frequency
(12V, 8Ω+66μH)



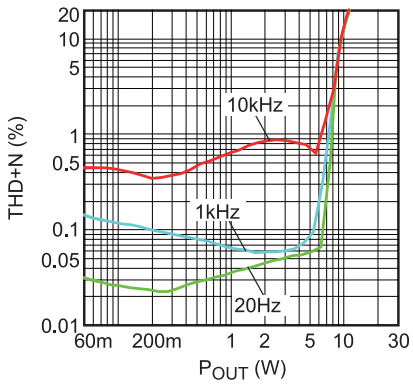

### THD+N vs. Frequency
(16V, 8Ω+66μH)



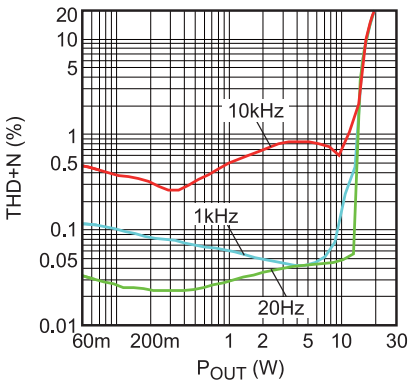

### THD+N vs. Frequency
(18V, 8Ω+66μH)



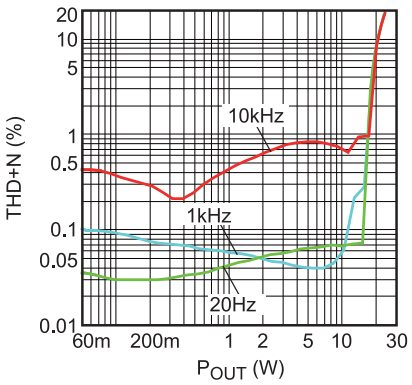

### THD+N vs. $P_{OUT}$
(12V, 8Ω+66μH)



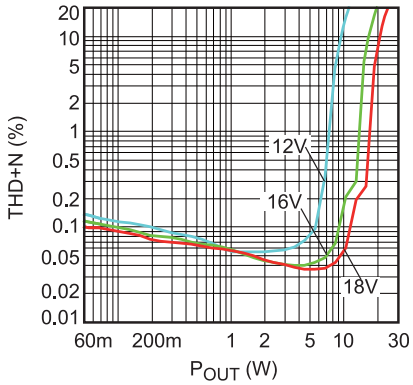

### THD+N vs. $P_{OUT}$
(16V, 8Ω+66μH)



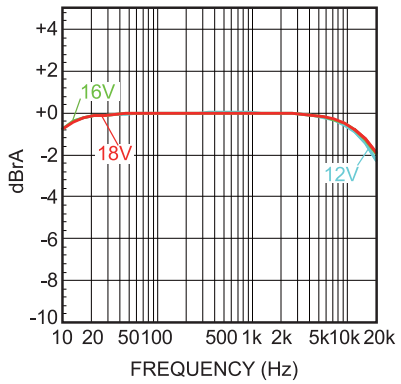

### THD+N vs. $P_{OUT}$
(18V, 8Ω+66μH)



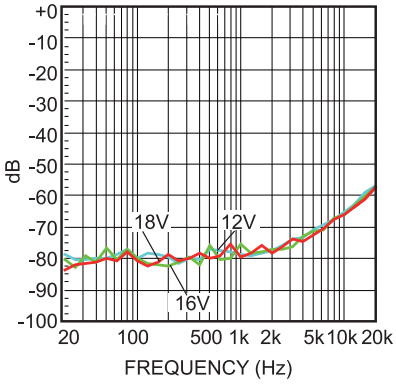

### THD+N vs. $P_{OUT}$
(1kHz, 8Ω+66μH)




### Frequency Response
(1W, 8Ω+66μH)




### PSRR Test
(8Ω+66μH, Gain=20dB,
$V_{AC_RIPPLE}$=300m$V_{PP}$)



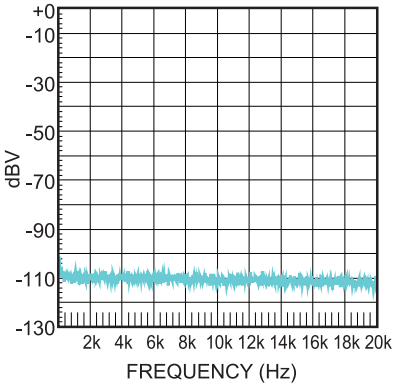


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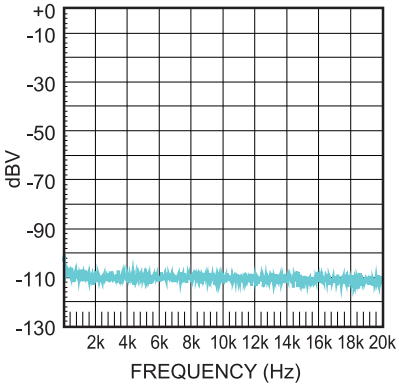
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{CC}$ = 12V, GAIN = 20dB, f = 1kHz, $T_A$ = 25°C, unless otherwise noted.**

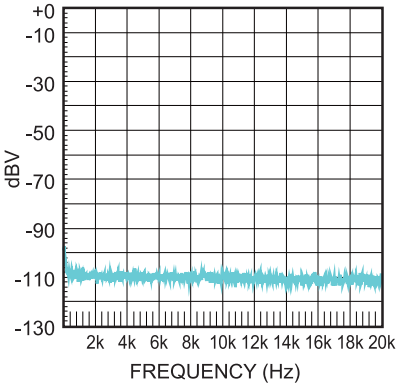
**FFT Noise Floor Test**
(12V, 8Ω+66μH)



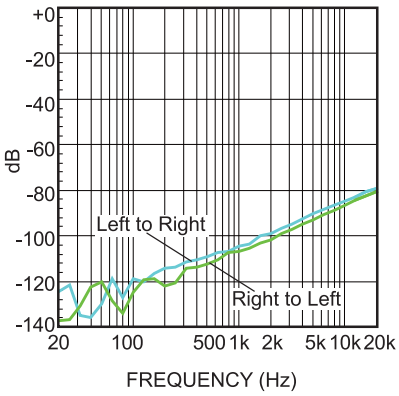

**FFT Noise Floor Test**
(16V, 8Ω+66μH)



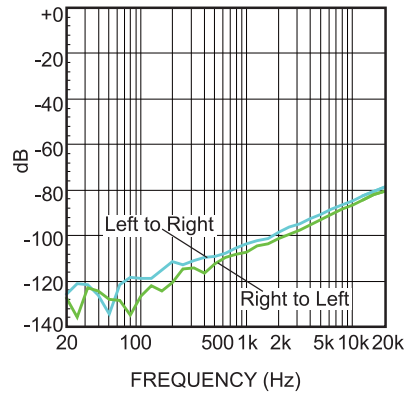

**FFT Noise Floor Test**
(18V, 8Ω+66μH)



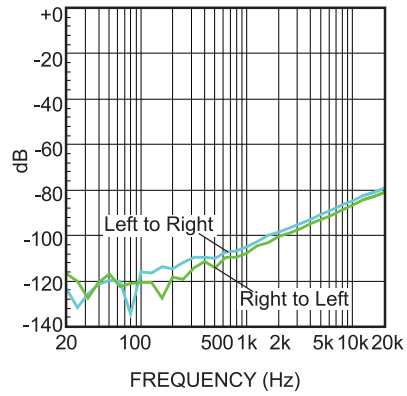

**Cross Talk**
(12V, 8Ω+66μH, $P_{OUT}$=5W)



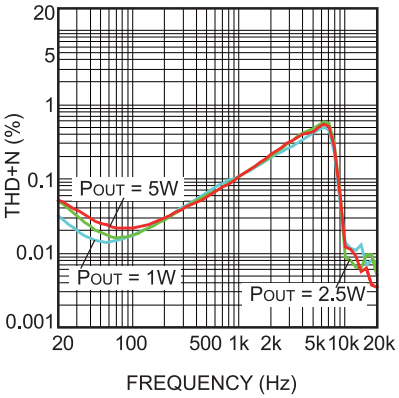

**Cross Talk**
(16V, 8Ω+66μH, $P_{OUT}$=5W)



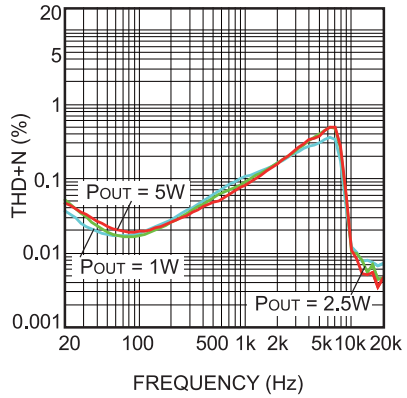

**Cross Talk**
(18V, 8Ω+66μH, $P_{OUT}$=5W)



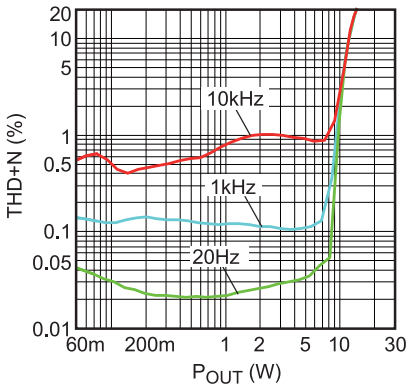

**THD+N vs. Frequency**
(12V, 6Ω+44μH)




**THD+N vs. Frequency**
(16V, 6Ω+44μH)




**THD+N vs. $P_{OUT}$**
(12V, 6Ω+44μH)



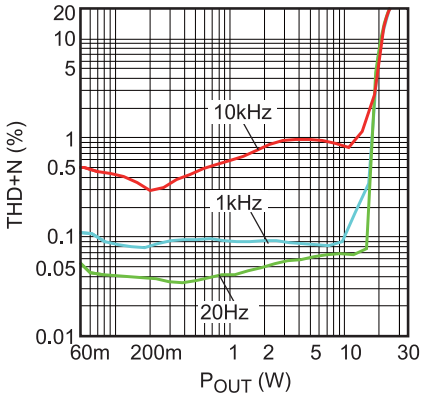


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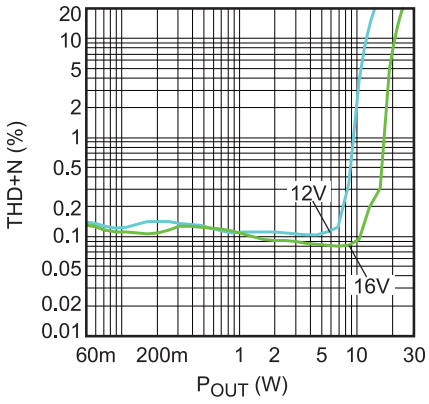
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{CC}$ = 12V, GAIN = 20dB, f = 1kHz, $T_A$ = 25°C, unless otherwise noted.**

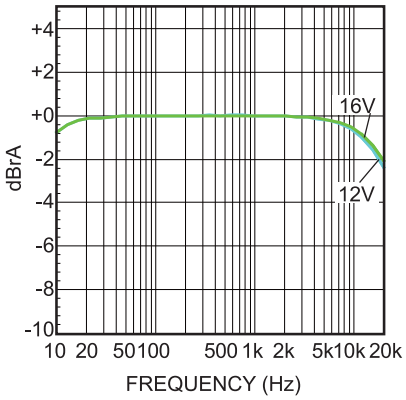
### THD+N vs. $P_{OUT}$
(16V, 6Ω+44μH)



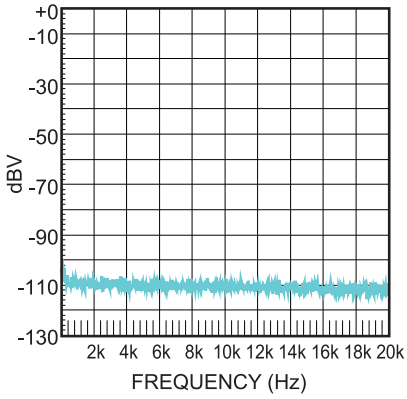

### THD+N vs. $P_{OUT}$
(1kHz, 6Ω+44μH)



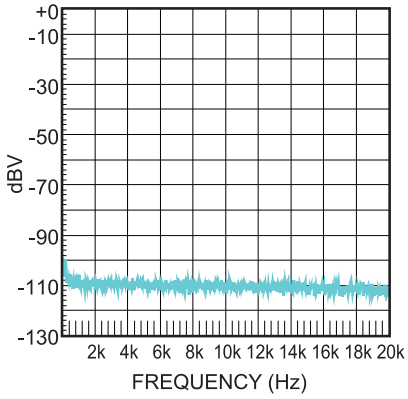

### Frequency Response
(1W, 6Ω+44μH)



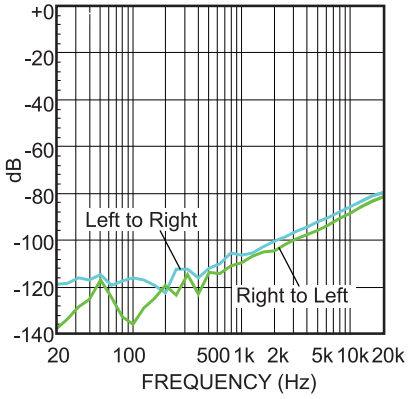

### FFT Noise Floor Test
(12V, 6Ω+44μH)



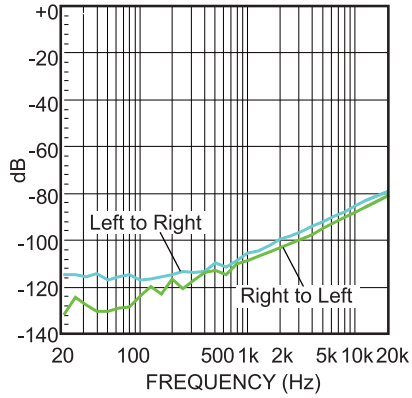

### FFT Noise Floor Test
(16V, 6Ω+44μH)



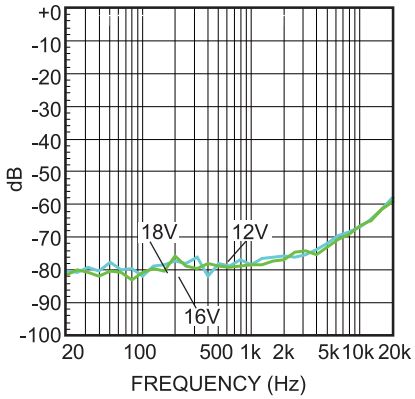

### Cross Talk Test
(12V, 6Ω+44μH, $P_{OUT}$=5W)




### Cross Talk Test
(16V, 6Ω+44μH, $P_{OUT}$=5W)




### PSRR Test
(6Ω+44μH, Gain=20dB,
$V_{AC_RIPPLE}$=300m$V_{PP}$)



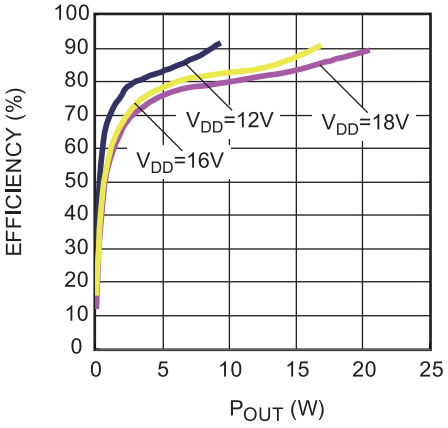


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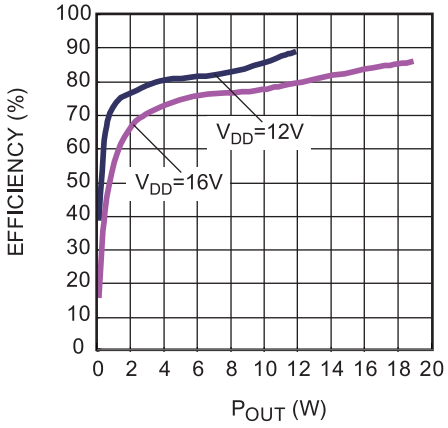
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

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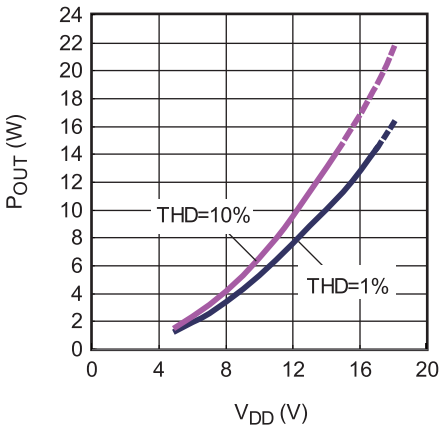
**Efficiency vs. $P_{OUT}$**
(8Ω+66μH)



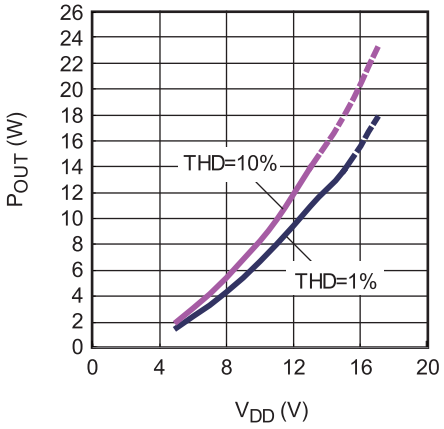

**Efficiency vs. $P_{OUT}$**
(6Ω+44μH)




**$V_{DD}$ vs. $P_{OUT}$**
(8Ω+66μH)




**$V_{DD}$ vs. $P_{OUT}$**
(6Ω+44μH)



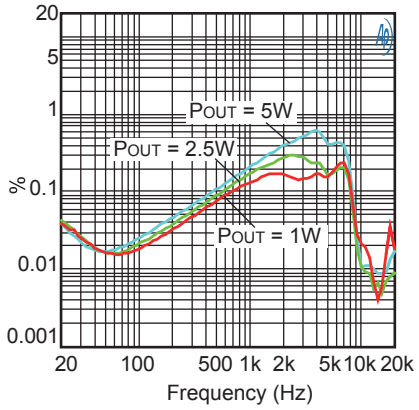


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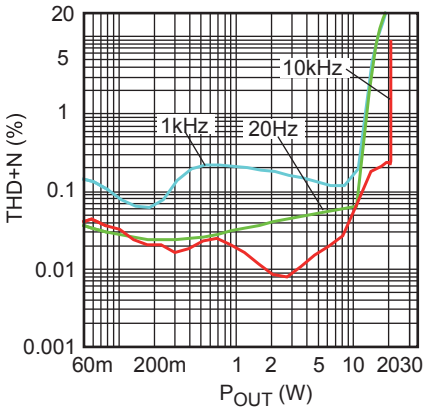
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{CC}$ = 12V, GAIN = 20dB, f = 1kHz, $T_A$ = 25°C, unless otherwise noted.**

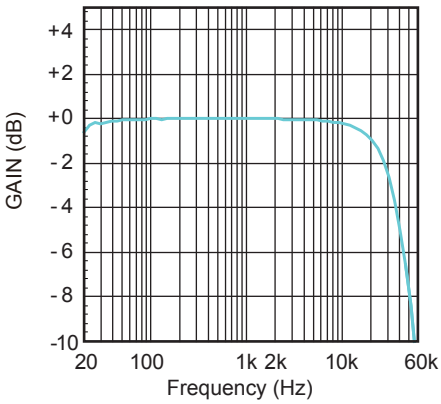
### THD+N vs. Frequency
(12V, 4Ω+33μH)



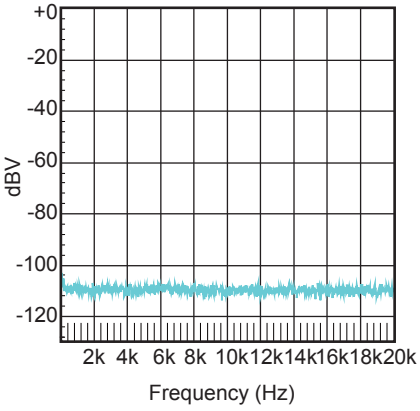

### THD+N vs. $P_{OUT}$
(12V, 4Ω+33μH)



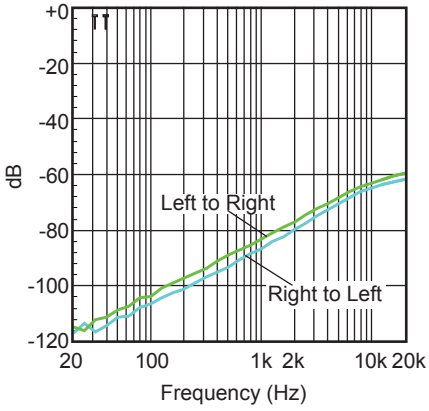

### Frequency Response
(12V, 4Ω+33μH, 1W)



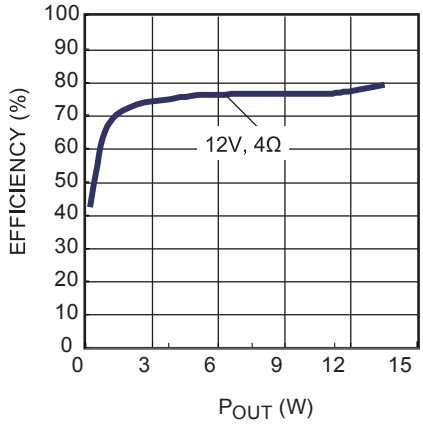

### FFT Noise Floor Test
(12V, 4Ω+33μH)



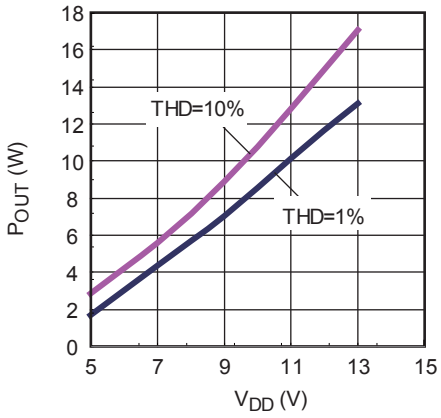

### Cross Talk
(12V, 4Ω+33μH, $P_{OUT}$=5W)




### Efficiency vs. $P_{OUT}$
(4Ω+33μH)




### $V_{DD}$ vs. $P_{OUT}$
(4Ω+33μH)





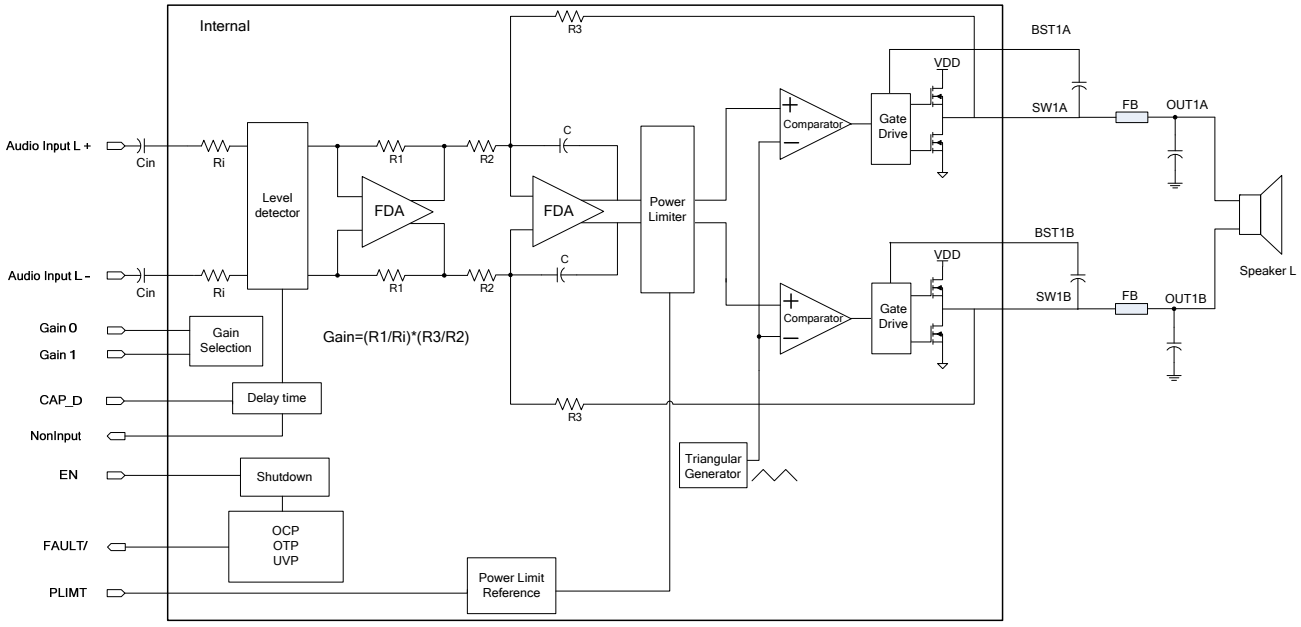
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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | EN | Enable input. Drive EN high to turn on the Amplifier 1A/1B/2A/2B, low to turn them off. |
| 2 | /FAULT | Fault Output. A low output at FAULT indicates that the IC has detected an over temperature or over current condition. This output is open drain. |
| 3 | IN1A | Positive audio input for channel 1. Biased at 2.5V. |
| 4 | IN1B | Negative audio input for channel 1. Biased at 2.5V. |
| 5 | GAIN0 | Gain selection bit. |
| 6 | GAIN1 | Gain selection bit. |
| 7 | AVCC | Internal analog reference, 5.5V, need connect a bypass capacitor from AVCC to AGND. |
| 8 | AGND | Analog ground. |
| 9 | VDR | Gate Drive Supply Bypass. VDR powers the internal circuitry, internal MOSFET gate drive. Bypass VDR to AGND with a 0.1μF to 10μF capacitor. |
| 10 | PLIMIT | Power limit and anti-clipping feature control.<br>Connect a resistor divider from AVCC to GND to set power limit. Connect directly to AVCC for no power limit. |
| 11 | IN2B | Negative audio input for channel 2. Biased at 2.5V. |
| 12 | IN2A | Positive audio input for channel 2. Biased at 2.5V. |
| 13 | InAbsence | Open drain output used to report the input signal absence. |
| 14 | Cap_D | Delay Time control for input signal absence report function. This holding time can be adjusted with external capacitor. Connect this pin to AGND to disable automatic shutdown with zero signal input function. |
| 15, 16 | PVCC2 | Power supply input for channel 2. Bypass PVCC2 to PGND2 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the PVCC2 and PGND2 pins. |
| 17 | BST2A | High-side MOSFET bootstrap input for Amplifier 2A. A capacitor from BST2A to SW2A supplies the gate drive current to the internal high-side MOSFET. |
| 18 | SW2A | Switched power output for Amplifier 2A (the positive output of channel 2). |
| 19 | PGND2 | Power ground for Amplifier 2A/2B. |
| 20 | SW2B | Switched power output for Amplifier 2B (the negative output of channel 2). |
| 21 | BST2B | High-side MOSFET bootstrap input for Amplifier 2B. A capacitor from BST2B to SW2B supplies the gate drive current to the internal high-side MOSFET. |
| 22 | BST1B | High-side MOSFET bootstrap input for Amplifier 1B. A capacitor from BST1B to SW1B supplies the gate drive current to the internal high-side MOSFET. |
| 23 | SW1B | Switched power output for Amplifier 1B (the negative output of channel 1). |
| 24 | PGND1 | Power ground for Amplifier 1A/1B. |
| 25 | SW1A | Switched power output for Amplifier 1A (the positive output of channel 1). |
| 26 | BST1A | High-side MOSFET bootstrap input for Amplifier 1A. A capacitor from BST1A to SW1A supplies the gate drive current to the internal high-side MOSFET. |
| 27, 28 | PVCC1 | Power supply input for channel 1. Bypass PVCC1 to PGND1 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the PVCC1 and PGND1 pins. |


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# FUNCTIONAL BLOCK DIAGRAM




**Functional Block Diagram (only one channel)**


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# OPERATION

The MP7752 is a fully integrated Class D stereo BTL audio amplifier. Because of the switching Class D output stage, power dissipation in the amplifier is drastically reduced when compared to Class A, B or A/B amplifiers while maintaining high fidelity and low distortion.

The amplifier has fully differential outputs and inputs. The differential input is useful to minimize the common-mode noise (any noise that appears on both input lines of the channel). This device can still be used with a single-ended input.

The MP7752 includes eight high-power MOSFETs wherein for each half-bridge channel the output driver stage uses two N-Channel MOSFETs to deliver the pulses to the magnetic bead and capacitor output filter which in turn drives the load. To fully enhance the high-side MOSFET, the gate is driven to a voltage higher than the source by the bootstrap capacitor between OUTxx and BSTxx pins. While the output is driven low, the bootstrap capacitor is charged from power supply through an internal circuit. The gate of the high-side MOSFET is driven high from the voltage at Bootstrap Supply, forcing the MOSFET gate to a voltage higher than power supply voltage and allowing the MOSFET to fully turn on, reducing power loss in the amplifier.

The gain of the MP7752 is set by the input terminals, GAIN0 and GAIN1. The actual gain settings are controlled by ratios of the input and feedback resistors

### Enable Function

The MP7752 EN input is an active high enable control. To enable the MP7752, drive EN with a 2.0V or higher voltage. To disable the amplifier, drive it below 0.4V. While the MP7752 is disabled, the PVCC operating current is around 250μA and the output driver MOSFETs are turned off.

### Input signal Absence detect

The MP7752 includes an internal circuit which allows the system automatic shutdown after the absence of the audio signal. This feature is used for energy-using products and for battery operated applications.

The MP7752 includes a delay circuit which allows the IC continues to hold the flag after the absence of the audio signal. This holding time can be adjusted with external capacitor.

1. The input absence flag will be high initially when power on. After device enabled, the internal circuit start to detect the input signal. MP7752 will then hold the output report and normal operation for a delay time which can be adjusted by the Capacitor value @ pin 14. Then MP7752 will turn off the all MOSFETs and pull low the input absence output, until the input signal detected again.

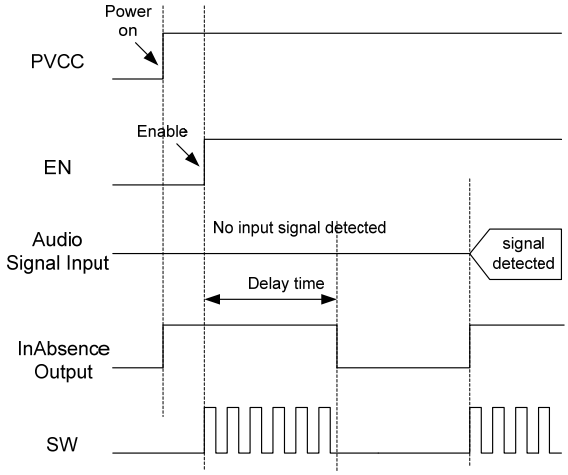



**Figure 1a: enable on with no signal detected**

2. The input absence flag output will be or maintain high when input signal is detected. The delay circuit will only be activated when the input signal absence. MP7752 will then hold the output report for a delay time which can be adjusted by the Capacitor value @ pin 14. Then MP7752 will turn off the all MOSFETs and pull low the input absence output, until the input signal detected again.


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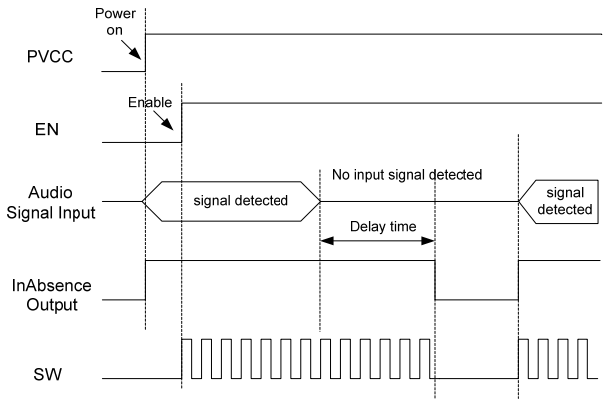



**Figure 1b: enable on with audio signal present**

## Adjustable Power Limit

Power limit and anti-clipping feature control. The voltage at pin 10 can used to limit the power to levels below that which is possible based on the supply rail.
Connect a resistor divider from AVCC to GND to set power limit. Connect directly to AVCC for no power limit.

An external reference may also be used if tighter tolerance is required. Also add a 1μF capacitor from pin 10 to ground.

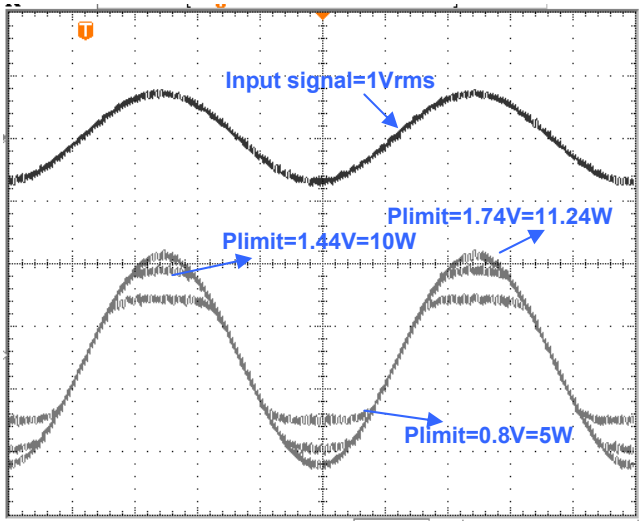



**Figure 2. PLIMT Circuit Operation**

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. This "virtual" rail is 9 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L}$$

for unclipped power
Where:

$R_S$ is the total output series resistance (including Rdson and the resistance of output filter.

$R_L$ is the load resistance.

$V_P$ is the peak amplifier of the output voltage.

$V_P$ = 9 x PLIMIT voltage if 8 x PLIMIT < PVCC
And

$$P_{OUT}\ @10\%THD \approx 1.25 \times \text{unclipped } P_{OUT}$$

**Table 2: Power Limit Typical Operation**

| Test Condition | PLIMIT Voltage | Output Voltage (Vp-p) | Output Power (10% THD) |
|---|---|---|---|
| VDD=12V, Vin=1Vrms, Load=8Ω, Gain=20dB | 0.80V | 14.9 | 5.0W |
| VDD=16V, Vin=1Vrms, Load=8Ω, Gain=20dB | 0.80V | 14.9 | 5.0W |
| VDD=16V, Vin=1Vrms, Load=8Ω, Gain=20dB | 1.44V | 23.6 | 10.0W |
| VDD=18V, Vin=1Vrms, Load=8Ω, Gain=20dB | 1.44V | 23.6 | 10.0W |

## Gain Setting

The gain of the MP7752 is set by the input terminals, GAIN0 and GAIN1. The actual gain settings are controlled by ratios of the internal input and feedback resistors, details please see the below table.


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**Table 2: Gain Setting**

| GAIN0 | GAIN1 | Typ. GAIN (dB) | Typ. Input Impedance (kΩ) |
|---|---|---|---|
| 0 | 0 | 20 | 75 |
| 1 | 0 | 26 | 50 |
| 0 | 1 | 32 | 30 |
| 1 | 1 | 36 | 20 |

### Over-Temperature Shutdown

Thermal monitoring is also integrated into the MP7752. If the die temperature rises above 150°C, all switches turn off. The temperature must fall below 130°C before normal operation resumes, with the same power-up sequence used to prevent popping noise.

### Short Circuit Performance

The MP7752 has internal overload and short circuit protection. The currents in both the high-side and low-side MOSFETs are measured. Upon detection of short circuit, all MOSFETs of the over current full bridge channel will go into high impedance for a fixed duration before resuming normal operation. After the fixed duration and the short circuit condition is removed, the MP7752 will restart with the start up sequence that is used for normal starting to prevent a pop from occurring.

### Fault Output

The MP7752 includes an open drain, active low fault indicator output on the /FAULT pin. A fault triggers if either the current limit or thermal shutdown is tripped.

A fault on any channel will cause the FAULTB pin to pull low. A fault on either channel will cause the all outputs to go into high impedance. When the fault goes away, the MP7752 will resume normal operation.

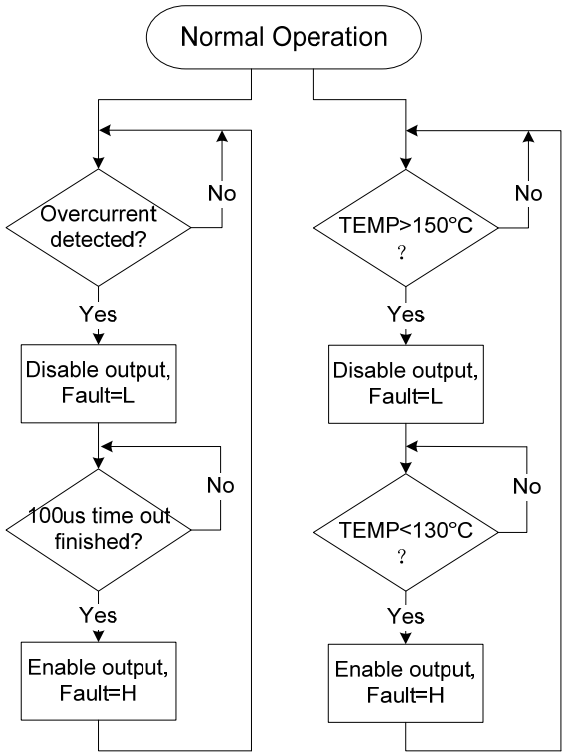



**Figure 3: Fault Timing Chart**


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# APPLICATION INFORMATION

## COMPONENT SELECTION

### Delay time for input signal absence report

The Recovery time is defined as follows.

$$T_{delay} = 1.6 \times 10^8 \times C_R [sec]$$

### Choosing the Output EMI Filter

The magnetic bead-capacitor filter converts the pulses at SW to the output voltage that drives the speaker. Both PVCC line and output current flow needed magnetic beads to prevent large radiation from high slew-rate pulse. The larger impedance of the magnetic bead, the better EMI performance can be approach.

### Input Coupling Capacitor

The input coupling capacitor transmits the AC signal from the source to the MP7752 while blocking the DC voltage. Choose an input coupling capacitor such that the corner frequency ($f_{IN}$) is less than the passband frequency. The corner frequency is calculated as:

$$f_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}}$$

The impedance of the input resister is different with the different gain setting. At the same gain setting, the input impedance from part-to-part may shift by ±20% due to shifts in the actual resistance of the input resistors. But please note that the gain variation from part-to-part is small.

For design purposes, the input network should be designed assuming an input impedance of 16 kΩ, which is the absolute minimum input impedance of the MP7752. At the lower gain settings, the input impedance could increase as high as 90 kΩ.

### Power Source

For maximum output power, the amplifier circuit requires a regulated external power source. A high power-supply voltage can deliver more power to a given load resistance, but a power-source voltage exceeding the maximum voltage of 18V can damage the MP7752. The MP7752's power supply rejection is excellent, though power-supply noise can pass to the output, so care must be taken to minimize power supply noise within the pass-band frequencies. Bypass the power supply with a large capacitor (typically aluminum electrolytic) along with two smaller 1μF and 1nF ceramic capacitors at the MP7752 VCC supply pins.

### PCB Layout

Circuit layout is critical for optimal performance, low output distortion, and noise. Duplicate the EVB layout for best results. For layout changes, follow these guidelines.

1) Place the following components as close to the MP7752 as possible:

Bootstrap Capacitors

$C_{BS}$ supply the gate drive current to the internal HS-FET. Place $C_{BS}$ as close to BST pin and SW pin as possible.

Power Supply Bypass Capacitors

$C_{BYP}$ carry the transient current for the switching power stage. To avoid overstressing the MP7752 and excessive output noise, place $C_{BYP}$ as close to the PVCC pins as possible.

2) The magnetic bead-Capacitor filter converts the pulse train at SW to the output voltage that drives the speaker. Please keep the filter capacitor close to the magnetic bead.

3) Make sure that any traces carrying the switch node (SW) voltages are routed far from any input signal traces. If the trace must run near the SW trace near the input, shield the input with a ground plane between the traces. Physically separate each channel to prevent crosstalk.

Route each power supply from the source to each channel individually, not serially. This prevents channel-to-channel coupling through the power supply input.


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### Electro-Magnetic Interference (EMI) Considerations

Due to the switching nature of Class D amplifiers, care must be taken to minimize the effects of electromagnetic interference from the amplifier. However, proper component selection and careful attention to circuit layout can minimize the effects of the EMI due to the amplifier switching.

The magnetic beads are used for blocking radiated emissions from SW nodes. For the best EMI performance, use high current and high impedance magnetic bead. muRata NFZ2M series CLASS D EMI filter has been tested work well in series with PVCC and four SW outputs.

The size of high-current loops that carry rapidly changing currents must be minimized: Make sure that the $V_{CC}$ bypass capacitors are as close to the MP7752 as possible.

Nodes that carry rapidly changing voltage, such as SW, need to be made as small as possible. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.

MP7752 EVB passed CISPR22 CLASS B standard with stereo full power output.

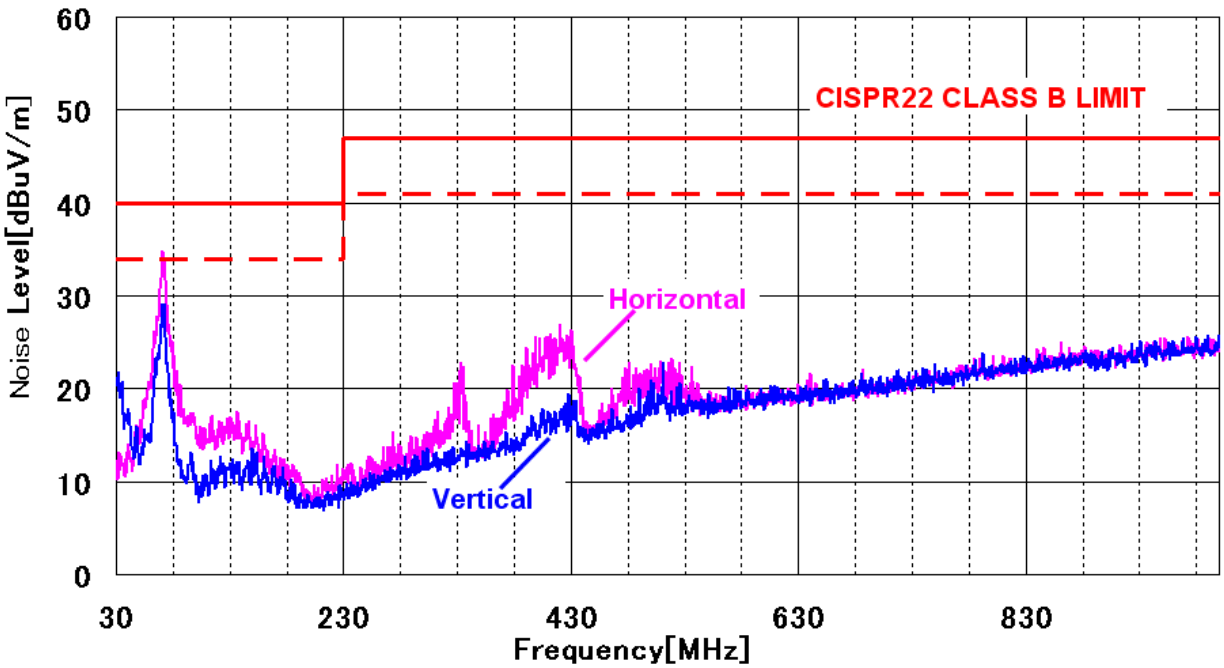



**Figure 4: EMI Test Data of MP7752 EVB**

Test Condition: 10 meter EMI chamber, 1.2 meter twist speaker cable, MP7752 EVB stereo test. VDD=12V, LOAD=8ohm+66uH, $P_{OUT}$=9.5W X 2, 1 kHz Signal.


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# TYPICAL APPLICATION CIRCUITS

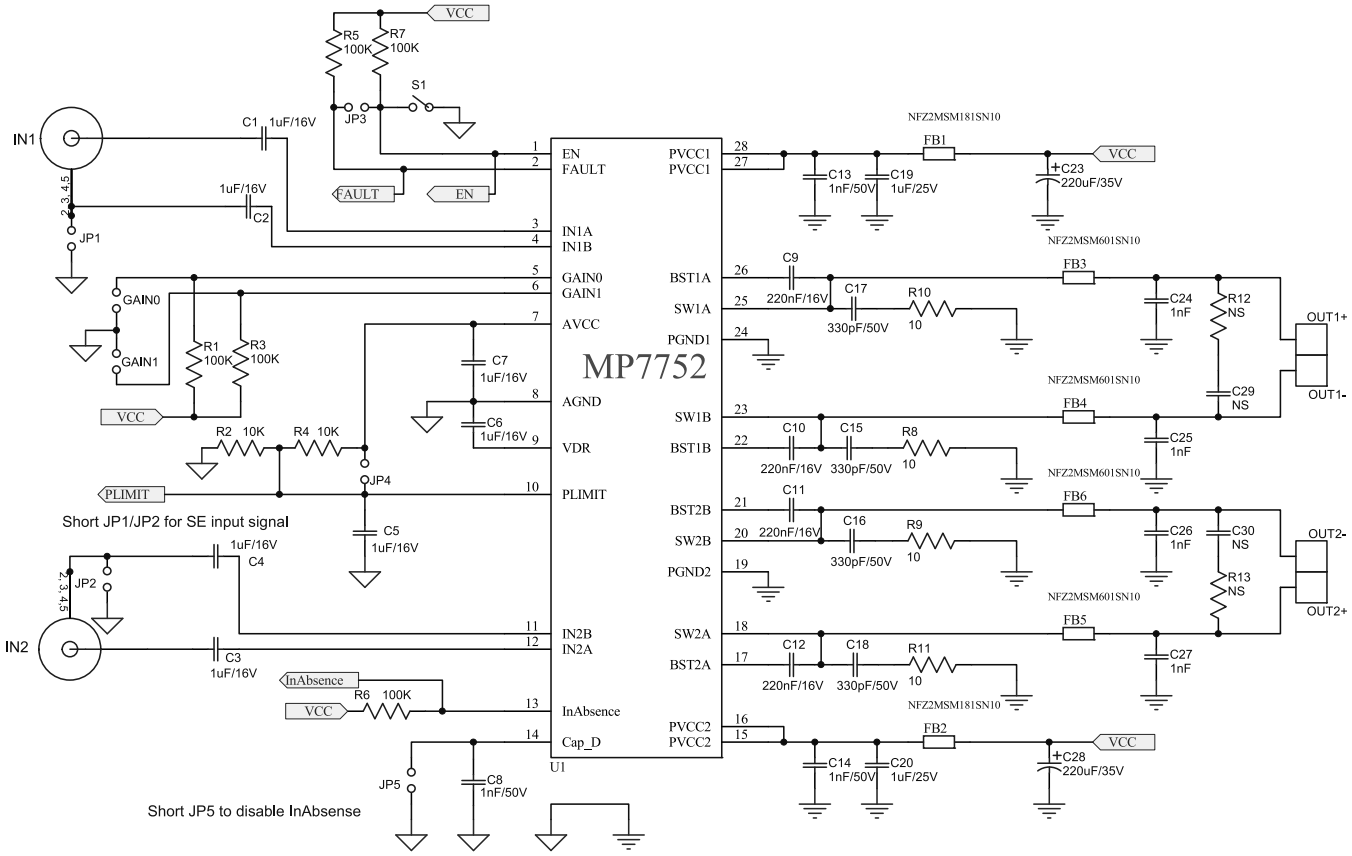
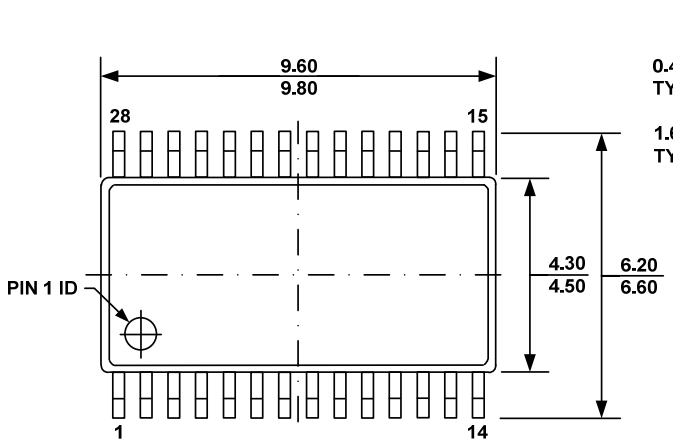



**Figure 5: Typical Application Circuit**

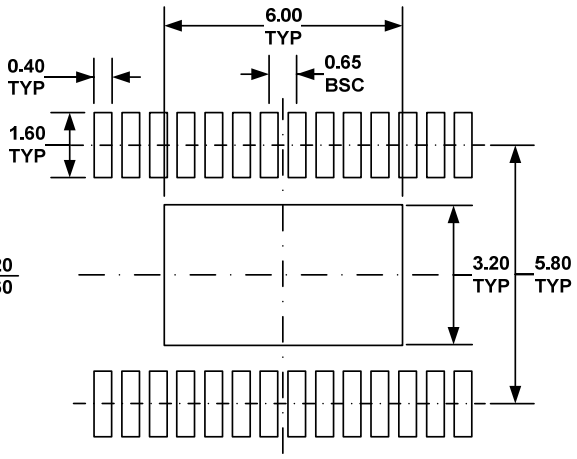

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# PACKAGE INFORMATION

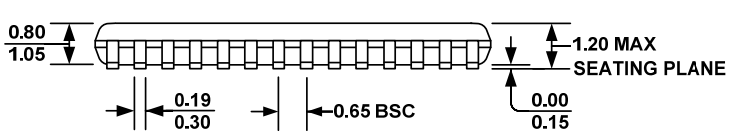
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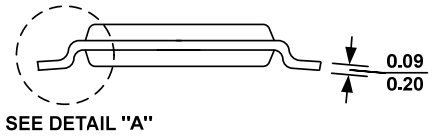

TOP VIEW



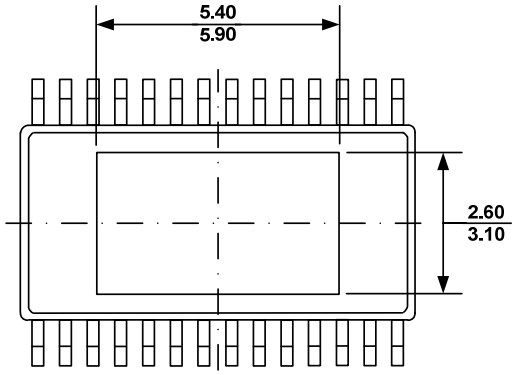

RECOMMENDED LAND PATTERN



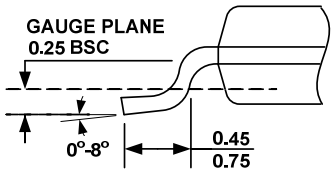

FRONT VIEW




SIDE VIEW




BOTTOM VIEW




DETAIL “A”

**NOTE:**

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2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE.

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