# PRELIMINARY DATA SHEET



# BIPOLAR ANALOG INTEGRATED CIRCUIT $\mu$ PC8112TB

# SILICON MMIC 1st FREQUENCY DOWNCONVERTER FOR CELLULAR/CORDLESS TELEPHONE

#### **DESCRIPTION**

The µPC8112TB is a silicon monolithic integrated circuit designed as 1st frequency downconverter for cellular/cordless telephone receiver stage. This IC consists of mixer and local amplifier. The  $\mu$ PC8112TB features high impedance output of open collector. Similar ICs of the  $\mu$ PC2757TB and  $\mu$ PC2758TB feature low impedance output of emitter follower. These TB suffix ICs which are smaller package than conventional T suffix ICs contribute to reduce your system size.

The µPC8112TB is manufactured using NEC's 20 GHz ft NESAT™III silicon bipolar process. This process uses silicon nitride passivation film and gold electrodes. These materials can protect chip surface from external pollution and prevent corrosion/migration. Thus, this IC has excellent performance, uniformity and reliability.

#### **FEATURES**

· Excellent RF performance

: IIP3 = -7 dBm@fnFin = 1.9 GHz (reference)

IM3 = -88 dBc@PRFin = -38 dBm, 1.9 GHz (reference)

Minimized carrier leakage

Similar conversion gain to  $\mu$ PC2757TB and lower noise figure than  $\mu$ PC2758TB : RFio = -80 dB@ fRFin = 900 MHz (reference)

RFIo = -55 dB@ fRFin = 1.9 GHz (reference)

High linearity

: Po (sat) = -2.5 dBmTyp. @fRFin = 900 MHz

Po (sat) = -3 dBmTYP. @fRFin = 1.9 GHz

Low current consumption

: Icc = 8.5 mAtyp.

Supply voltage

: Vcc = 2.7 to 3.3 V

· High-density surface mounting: 6-pin super mini mold package

#### **APPLICATION**

- 1.5 GHz to 1.9 GHz cellular/cordless telephone (PHS, DECT, PDC1.5G and so on)
- 800 MHz to 900 MHz cellular telephone (PDC800M and so on)

## ORDER INFORMATION

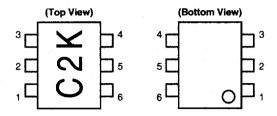
Part Number	Package	Markings	Supplying Form
μPC8112TB-E3	6 pin super minimold	C2K	Embossed tape 8 mm wide. Pin 1, 2, 3 face to tape perforation side. QTY 3kp/Reel.

Remark To order evaluation samples, please contact your local NEC sales office. (Part number for sample order: μPC8112TB)

Caution Electro-static sensitive devices

The information in this document is subject to change without notice.

## PIN CONNECTIONS



Pin No.	Pin Name
1	RFin
2	GND
3	LOin
4	PS
5	Vcc
6	IFout

PRODUCT LIN-UP (TA = +25 °C, Vcc = 3.0 V, ZL = Zs = 50  $\Omega$ )

ltems Part Number	No RF Icc (mA)	900 MHz SSB · NF (dB)	1.5 GHz SSB · NF (dB)	1.9 GHz SSB · NF (dB)	900 MHz CG (dB)	1.5 GHz CG (dB)	1.9 GHz CG (dB)	900 MHz IIP <sub>3</sub> (dBm)	1.5 GHz IIP <sub>3</sub> (dBm)	1.9 GHz IIP₃ (dBm)
μPC2757T	5.6	10	10	13	15	15	13	-14	-14	-12
μPC2757TB										
μPC2758T	11	9	10	13	19	18	17	-13	-12	-11
μPC2758TB										
μPC8112T	8.5	9	11	11	15	13	13	-10	-9	-7
μPC8112TB										*

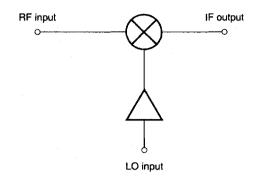
Part Number	900 MHz Poset (dBm)	1.5 GHz Posal (dBm)	1.9 GHz Posat (dBm)	900 MHz RFio (dB)	1.5 GHz RFio (dB)	1.9 GHz RFio (dB)	IF Output Configuration	Package
μPC2757T	-3	-	-8	-	_	-	Emitter follower	6-pin minimold
μPC2757TB								6-pin super minimold
μPC2758T	+1	-	4	-		-		6-pin minimold
μPC2758TB								6-pin super minimold
μPC8112T	-2.5	-3	-3	-80	57	-55	Open collector	6-pin minimold
μPC8112TB								6-pin super minimold

Remark Typical performance. Please refer to ELECTRICAL CHARACTERISTICS in detail.

Notice 1.  $\mu$ PC2757,  $\mu$ PC2758's IIP3 are measured with the condition as same as  $\mu$ PC8112.

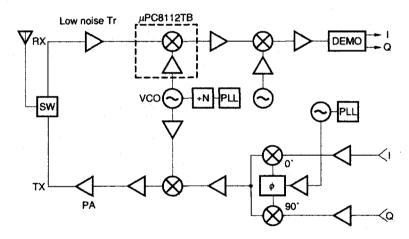
2. This document is to be specified for  $\mu$ PC8112TB. The other part number mentioned in this document should be referred to the data sheet of each part number.

# INTERNAL BLOCK DIAGRAM



# $\mu$ PC8112 LOCATION EXAMPLE IN THE SYSTEM

# Digital cordiess phone



# PIN EXPLANATION

Pin No.	Pin Name	Applied Voltage V	Pin Voltage V	Function and Application	Internal Equivalent Circuit
5	Vcc	2.7 to 3.3		Supply voltage pin.  This pin should be connected with bypass capacitor (eg 1000 pf) to minimize ground impedance.	
6	IF output	as same as Vcc voltage through external inductor	-	IF output pin. This output is configured with open collector of high impedance. This pin should be externally equipped with matching circuit of inductor should be selected as small resistance and high frequency use.	From (b)
	RF input	ļ	1.2	RF input pin of mixer. This mixer is designed as double balanced type. This pin should be externally coupled to front stage with DC cut capacitor.	
2	GND	0	<del>-</del>	Ground pin. This pin must be connected to the system ground. Form the ground pattern as wide as possible and the truck length as short as possible to minimize ground impedance.	
3	LO input	-	1.4	Input pin of local amplifier. This amplifier is designed as differential type.  This pin should be externally coupled to local signal source with DC cut capacitor.  Recommendable input level is –15 to 0 dBm.	To mixer
	PS	Vcc or GND	<del>-</del>	Power save control pin. This pin can control ON/OFF operation with bias as follows;  Bias: V Operation  VPS ≥ 2.5 ON  0 - 0.5 OFF	\$ \\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\

## **ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Conditions	Ratings	Unit
Supply Voltage	Vcc	T <sub>A</sub> = +25 °C	3.6	V
Total Circuit Current	lcc	T <sub>A</sub> = +25 °C	77.7	mA
Total Power Dissipation	Po	Mounted on double sided copper clad $50 \times 50 \times 1.6$ mm epoxy glass PWB (T <sub>A</sub> = +85 °C)	200	mW
Operating Ambient Temperature	TA		-40 to +85	°C
Storage Temperature	Tatg		-55 to +150	°C

# RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Notice
Supply Voltage	V∞	2.7	3.0	3.3	٧	5 pin and 6 pin should be applied to same voltage.
Operating Ambient Temperature	Ta	-40	+25	+85	°C	
LO Input Level	PLOin	-15	-10	0	dBm	Zs = 50 Ω
RF Input Frequency	f8Fin	0.8	1.9	2.0	GHz	
IF Output Frequency	fiFoul	100	250	300	MHz	With external matching

# ELECTRICAL CHARACTERISTICS (Unless otherwise specified, $T_A = +25$ °C, $V_{CC} = V_{PS} = V_{IFout} = 3.0 \text{ V}$ , $P_{LOin} = -10 \text{ dBm}$ , $Z_S = Z_L = 50 \Omega$ )

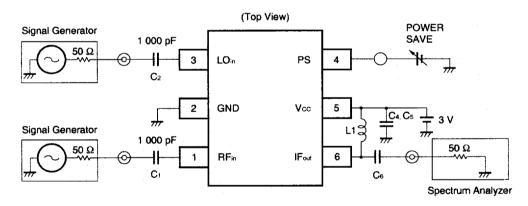
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Circuit Current	lcc	No signals	4.9	8.5	11.7	mA
Circuit Current at power save mode	Icc(PS)	Vcc = 3.0 V, Vps = 0.5 V			0.1	μΑ
Conversion Gain	CG	farin = 900 MHz, floin = 1000 MHz farin = 1.9 GHz, floin = 1.66 GHz	11.5 9.5	15 13	17.5 15.5	dB
Single Side Band Noise Figure	SSB NF	farin = 900 MHz, floin = 1000 MHz farin = 1.9 GHz, floin = 1.66 GHz		9.0 11.2	11 13.2	d₿
Saturated Output Power	PO(sat)	fRFin = 900 MHz, fLoin = 1000 MHz fRFin = 1.9 GHz, fLoin = 1.66 GHz (PAFin = -10 dBm each)	-6.5 7	-2.5 -3		dBm

STANDARD CHARACTERISTICS FOR REFERENCE (Ta = +25 °C, Vcc = Vps = ViFout = 3.0 V,  $P_{LOin}$  = -10 dBm, Zs = ZL = 50  $\Omega$ )

Parameter	Symbol	Test Conditions	Reference	Unit
Conversion Gain	CG	farin = 1.5 GHz, floin = 1.6 GHz	13	dB
Single Side Band Noise Figure	SSB NF	frein = 1.5 GHz, floin = 1.6 GHz	11	dΒ
LO Leakage at RF pin	LOn	faFin = 900 MHz, fLoin = 1000 MHz faFin = 1.5 GHz, fLoin = 1.6 GHz faFin = 1.9 GHz, fLoin = 1.66 GHz	-45 -46 -45	ďΒ
RF Leakage at LO pin	RFIO	farin = 900 MHz, floin = 1000 MHz farin = 1.5 GHz, floin = 1.6 GHz farin = 1.9 GHz, floin = 1.66 GHz	80 57 55	dΒ
LO Leakage at IF pin	LOit	farin = 900 MHz, floin = 1000 MHz farin = 1.5 GHz, floin = 1.6 GHz farin = 1.9 GHz, floin = 1.66 GHz	-32 -33 -30	dΒ
Input 3rd Order Intercept Point****	IIP3	farin = 900 MHz, floin = 1000 MHz farin = 1.5 GHz, floin = 1.6 GHz farin = 1.9 GHz, floin = 1.66 GHz	10 9 7	dBm

Note IIP3 is determined by comparing two method; theoretical calculation and cross point of IM3 curve. IIP3 =  $(\Delta IM3 \times Pin + CG - IM3) \div (\Delta IM3 - 1)$  (dBm) [ $\Delta IM3$ : IM3 curve inclination in linear range]  $\mu$ PC8112's  $\Delta IM3$  is closer to 3 (theoretical inclination) than  $\mu$ PC2757 and  $\mu$ PC2758 of conventional ICs.

## **TEST CIRCUIT**



# LO input Ca PS bias PS bias

#### ILLUSTRATION OF THE TEST CIRCUIT ASSEMBLED ON EVALUATION BOARD

Component Number	IF 100 MHz Matching	IF 200 MHz Matching	Remarks
C1 to C5	1000 pF	1000 pF	CHIP C
C6	5 pF	2 pF	CHIP C
L1	330 nH	84 nH	CHIP L

# **EVALUATION BOARD CHARACTERS AND NOTE**

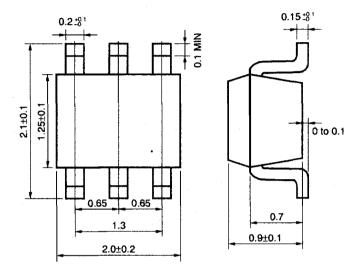
- (1) 35  $\mu$ m thick double-sided copper clad 35  $\times$  42  $\times$  0.4 mm polyimide board
- (2) Back side: GND pattern
- (3) Solder plated patterns
- (4) O: Through holes
- (5) To mount C6, pattern should be cut.

**ATTENTION** Test circuit or print pattern in this sheet is for testing IC characteristics. They are not an application circuit or recommended system circuit.

In the case of actual system application, external circuits including print pattern and matching circuit constant of output port should be designed in accordance with IC's S parameters and environmental components.

# PACKAGE DIMENSIONS

6 pin super minimold (Unit: mm)



#### NOTE ON CORRECT USE

- (1) Observe precautions for handling because of electro-static sensitive devices.
- (2) Form a ground pattern as wide as possible to minimize ground impedance (to prevent undesired oscillation).
- (3) Keep the track length of the ground pins as short as possible.
- (4) The bypass capacitor (e.g. 1 000 pF) should be attached to the Vcc pin.
- (5) The matching circuit should be externally attached to the IF output pin.
- (6) The DC cut capacitor must be each attached to the input and output pins.

#### RECOMMENDED SOLDERING CONDITIONS

This product should be soldered under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

#### μPC8112TB

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared Reflow	Package peak temperature: 235 °C or below Time: 30 seconds or less (at 210 °C) Count: 3, Exposure limit**init: None	IR35-00-3
VPS	Package peak temperature: 215 °C or below Time: 40 seconds or less (at 200 °C) Count: 3, Exposure limit***: None	VP15-00-3
Wave Soldering	Soldering bath temperature: 260 °C or below Time: 10 seconds or less Count: 1, Exposure limit <sup>Note</sup> : None	WS60-00-1
Partial Heating	Pin temperature: 300 °C Time: 3 seconds or less (per side of device) Exposure limit***: None	-

Note After opening the dry pack, keep it in a place below 25 °C and 65 % RH for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

For details of recommended soldering conditions for surface mounting, refer to information document SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL (C10535E).

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Anti-radioactive design is not implemented in this product.

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