Synchronus presettable 4-bit binary down counter — 54F193

FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset (clear)
- Expandable without external logic

DESCRIPTION

The 54F193 is a 4-bit synchronous up/ down counter in the binary mode. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the Low-to-High transition of either Clock input. If the CP_U clock is pulsed while CP_D is held High, the device will count up ... if CP_D is pulsed while CP_U is held High, the device will count down. Only one Clock input can be held High at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous reset pin – it may also be loaded in parallel by activating the asynchronous parallel load pin.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
16-Pin Ceramic DIP	54F193/BEA	GDIP1-T16
16-Pin Ceramic Flat Pack	54F193/BFA	GDFP2-F16
20-Pin Ceramic LLCC	54F193/B2A	CQCC2-N20

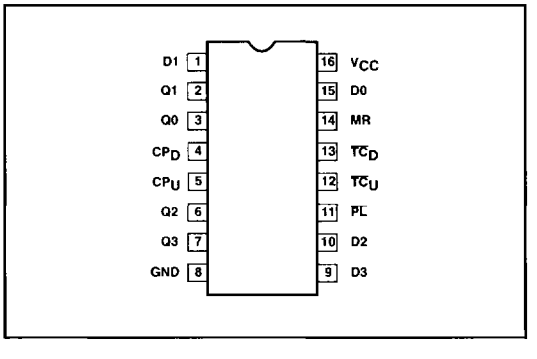
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

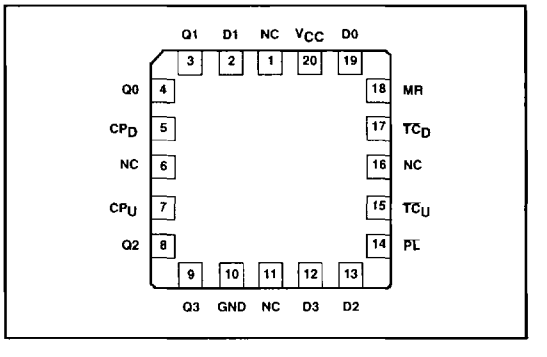
PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
CP_U	Count up clock input (active rising edge)	1.0/2.0	20µA/1.2mA
CP_D	Count down clock input (active rising edge)	1.0/2.0	20µA/1.2mA
MR	Asynchronous master reset input (active High)	1.0/1.0	20µA/0.6mA
$\overline{PL}$	Asynchronous parallel load input (active Low)	1.0/1.0	20µA/0.6mA
D0 - D3	Parallel data inputs	1.0/1.0	20µA/0.6mA
Q0 - Q3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}_D$	Terminal count down (borrow) output (active Low)	50/33	1.0mA/20mA
$\overline{TC}_U$	Terminal count up (carry) output (active Low)	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20µA in the High state and 0.6mA in the Low state.

PIN CONFIGURATION

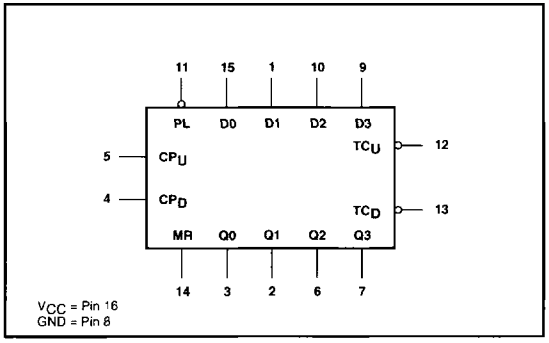


LLCC LEAD CONFIGURATION



Synchronus presettable 4-bit binary down counter | 54F193

LOGIC SYMBOL



Inside the device are four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

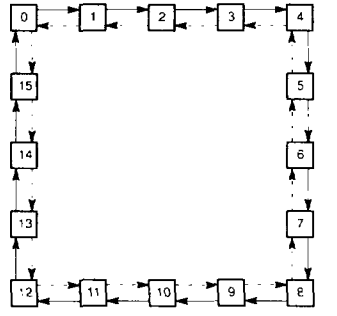
Each flip-flop contains JK feedback from slave to master, such that a Low-to-High transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held High while counting with the other, because the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either Clock input is Low. Applications requiring reversible operation must make the reversing decision while the activating clock is High to avoid erroneous counts.

The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally High. When the circuit has reached the maximum count state of 15, the next High-to-Low transition of CP_U will cause $\overline{TC}_U$ to go Low. $\overline{TC}_U$ will stay Low until CP_U goes High again, duplicating the count up clock, although delayed by two gate delays. Likewise, the $\overline{TC}_D$ output will go Low when the circuit is in the zero state and the CP_D goes Low. The $\overline{TC}$ outputs can be used as the Clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a two- gate delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel Data inputs D0 - D3) is loaded into the counter and appears on the outputs regardless of the conditions of the Clock inputs when the Parallel Load ($\overline{PL}$) input is Low. A High level on the Master Reset (MR) in put will disable the parallel load gates, override both Clock inputs, and set all Q outputs Low. If one of the Clock inputs is Low during and after a reset or load operation, the next Low-to-High transition of that clock will be interpreted as a legitimate signal and will be counted.

STATE DIAGRAM



Logic Equations for Terminal Count

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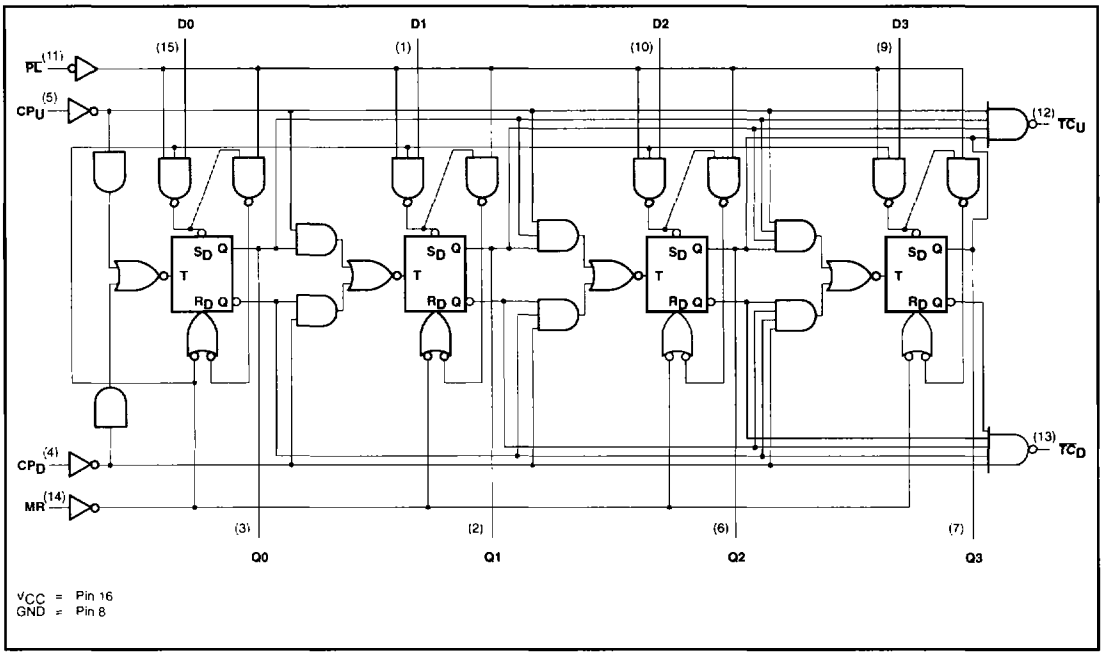
LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\overline{TC}_U$	$\overline{TC}_D$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	Count up				H[1]	H
Count down	L	H	H	↑	X	X	X	X	Count down				H	H[2]

H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5.0	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[3]		LIMITS			UNIT
				MIN	TYP[4]	MAX	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OH} = MAX, V_{IH} = MIN		2.5			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX, I_{OL} = MAX, V_{IH} = MIN			.35	.5	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH1}	High-level input current	V_{CC} = MAX, V_I = 2.7V			1	20	µA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5V	CP_U, CP_D			-1.8	mA
			Other inputs		-0.4	-0.6	mA
I_{OS}	Short-circuit output current[5]	V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current[6] (total)	V_{CC} = MAX			32	50	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{MAX}	Maximum clock frequency	Waveform 1	100	125		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 2	2.5 3.0	5.5 5.0	8.5 8.0	2.5 3.0	9.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP_U or CP_D to Qn	Waveform 1	2.5 5.0	5.5 8.5	8.5 12.0	3.0 6.0	9.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay D_n to Qn	Waveform 4	2.0 6.0	4.0 9.5	7.0 13.5	1.5 6.0	7.5 15.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to Qn	Waveform 3	4.5 5.5	6.5 8.5	10.0 12.0	4.0 5.0	11.0 13.0	ns ns
t_{PHL}	Propagation delay MR to Qn	Waveform 5	5.0	7.5	11.0	5.5	12.5	ns
t_{PLH}	Propagation delay MR to $\overline{TC}_U$	Waveform 5	6.0	8.5	12.0	5.5	12.5	ns
t_{PHL}	Propagation delay MR to $\overline{TC}_D$	Waveform 5	5.0	7.5	11.0	5.0	11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 3	6.0 6.0	9.5 9.0	13.5 12.0	6.0 6.0	15.0 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Dn to $\overline{TC}_U$ or $\overline{TC}_D$	Waveform 4	5.5 4.5	9.0 8.5	13.0 12.5	5.0 4.5	14.0 13.5	ns ns

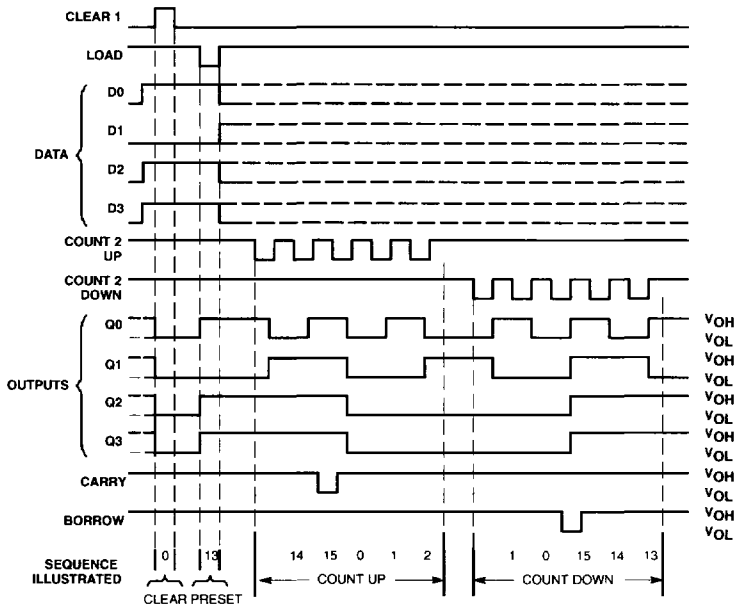
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_s(H) t_s(L)	Setup time, High or Low Dn to $\overline{PL}$	Waveform 6	4.5 4.5			5.0 5.0		ns ns
t_h(H) t_h(L)	Hold time, High or Low Dn to $\overline{PL}$	Waveform 6	2.0 2.0			2.0 2.0		ns ns
t_w(L)[5]	$\overline{PL}$ Pulse width Low	Waveform 1	6.0			6.0		ns
t_w(H)[5] t_w(L)[5]	CP_U or CP_D Pulse width High or Low	Waveform 1	3.5 5.0			3.5 5.0		ns ns
t_w(L)[5]	CP_U or CP_D Pulse width Low (Change of direction)	Waveform 1	10.0			10.0		ns
t_w(H)[5]	MR Pulse width High	Waveform 5	6.0			6.0		ns
t_{rec}	Recovery time, $\overline{PL}$ to CP_U or CP_D	Waveform 3	6.0			8.0		ns
t_{rec}	Recovery time MR to CP_U or CP_D	Waveform 5	4.0			4.0		ns

NOTES:

1. TC_U = CP_U at terminal count up (HHHH).
2. TC_D = CP_D at terminal count down (LLLL).
3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
4. All typical values are at V_{CC} = 5V, T_A = 25°C.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Measure I_{CCH} with parallel load and Master Reset inputs grounded, all other inputs at 4.5V and all outputs open.
7. Pulse width tests are guaranteed as specified, but are tested at 7.0ns due to tester limitations.

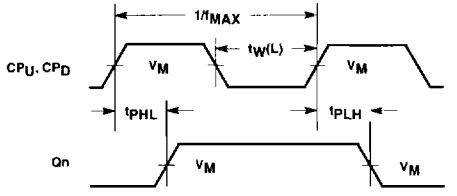
FUNCTIONAL WAVEFORM (Typical clear, load, and count sequences)



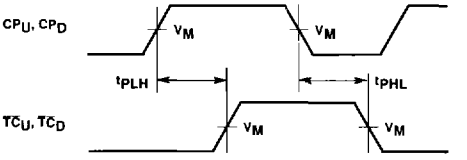
NOTES:
1. Clear overrides load, data, and count inputs.
2. When counting up, count-down input must be High; when counting down, count-up input must be High.

Binary Counter

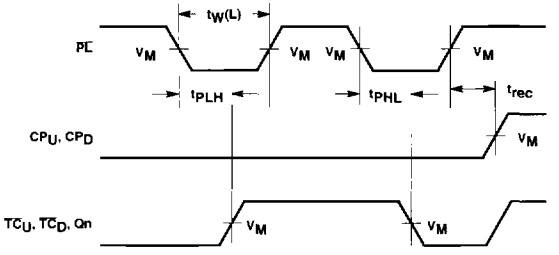
AC WAVEFORMS



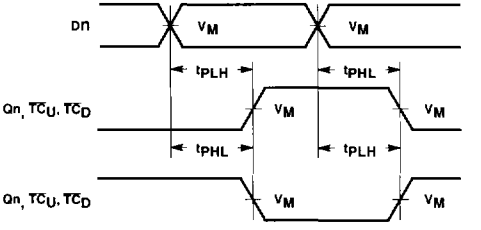
Waveform 1. Propagation Delay, Clock Input to Output, Clock Width and Maximum Clock



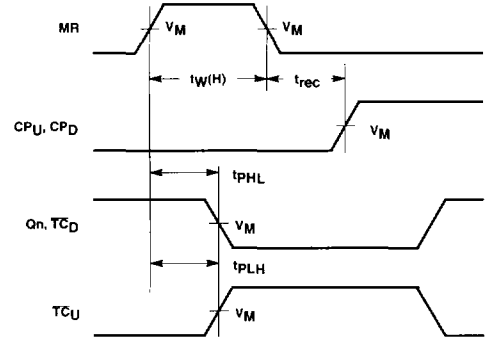
Waveform 2. Propagation Delay, Clock Pulse to Terminal Count



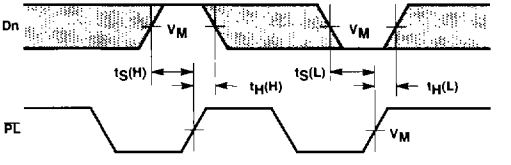
Waveform 3. Parallel Load Pulse Width, Parallel Load to Output Delays, and Parallel Load to Clock Recovery Time



Waveform 4. Propagation Delay, Data to Flip-Flop Outputs, Terminal Count Up and Down Outputs



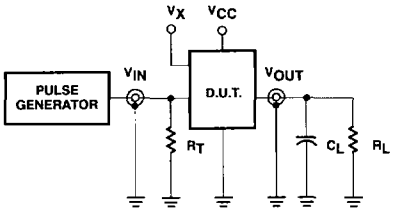
Waveform 5. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery



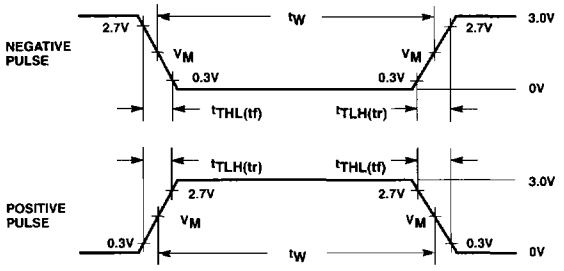
Waveform 6. Setup Time and Hold Time for Dn to $\overline{PL}$

V_M = 1.5V

TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns