MP4571

High-Efficiency, 1A, 60V, Fully Integrated Synchronous Buck Converter

DESCRIPTION

The MP4571 is a fully integrated, fixed-frequency, synchronous step-down converter. It can achieve up to 1A of continuous output current with peak current control for excellent transient response.

The wide 4.5V to 60V input voltage range accommodates a variety of step-down applications in an automotive input environment. A 2µA shutdown mode quiescent current makes it ideal for battery-powered applications.

The MP4571 integrates internal high-side and low-side power MOSFETs for high efficiency without an external Schottky diode, and is available in a 12-pin QFN package.

The MP4571 employs advanced asynchronous modulation (AAM), which achieves high efficiency during light load by scaling down the frequency to reduce the switching and gate driver losses.

The MP4571 offers standard features including built-in soft start, enable control, and a power good indicator. High duty cycle and low-dropout mode are provided for automotive cold crank conditions. In addition, the chip provides over-current protection with valley current detection, which helps prevent current runaway. It also has hiccup short-circuit protection (SCP), input under-voltage lockout (UVLO), and auto-recovery thermal protection.

With internal compensation, the MP4571 offers a very compact solution with a minimum number of readily available, standard external components. It is available in a QFN-12 (2.5mmx3mm) package.

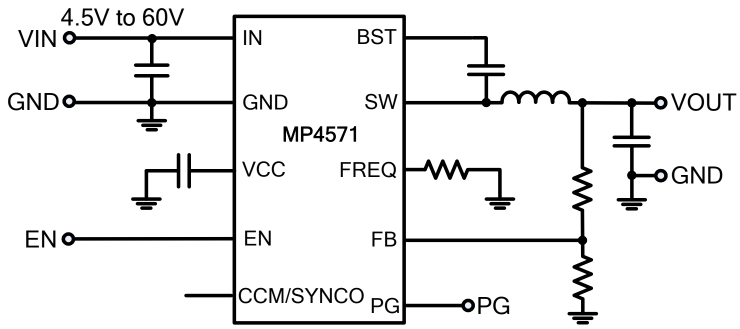
FEATURES

- Wide 4.5V to 60V Operating Input Range
- 1A Continuous Output Current
- High-Efficiency Synchronous Mode Control
- 250mΩ/45mΩ Internal Power MOSFETs
- Configurable Frequency Up to 2.2MHz
- 180° Out-of-Phase SYNCO Clock
- 40µA Quiescent Current
- Low Shutdown Mode Current: 2µA
- FB Tolerance: 1% at Room Temp, 2% at Full Temp
- Selectable AAM or Forced CCM Operation at Light Load
- Internal 0.45ms Soft Start
- Remote EN Control
- Power Good (PG) Indicator
- Low-Dropout Mode
- Over-Current Protection (OCP)
- Short-Circuit Protection with Hiccup Mode
- V_{IN} Under-Voltage Lockout (UVLO)
- Thermal Shutdown
- Available in a QFN-12 (2.5mmx3mm) Package
- Available in a Wettable Flank Package

APPLICATIONS

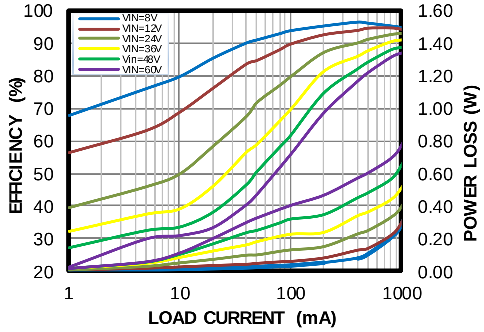
- Automotive Infotainment
- Automotive Lamps and LEDs
- Automotive Motor Control
- Industrial Power Systems

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 5V, L = 15μH, f_{SW} = 400kHz, AAM



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating**
MP4571GQB	QFN-12 (2.5mmx3mm)	*See Below*	1
MP4571GQBE***	QFN-12 (2.5mmx3mm)	*See Below*	1

* For Tape & Reel, add suffix -Z (e.g. MP4571GQB-Z).
** Moisture Sensitivity Level Rating
*** Wettable flank

TOP MARKING (MP4571GQB)

BFF
YWW
LLL

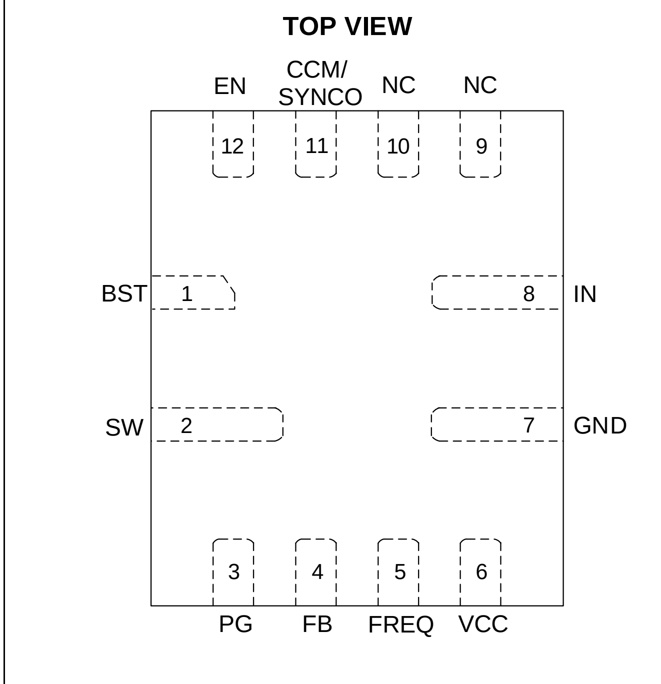
BFF: Product code of MP4571GQB (Non-wettable flank)
Y: Year code
WW: Week code
LLL: Lot number

TOP MARKING (MP4571GQBE)

BMN
YWW
LLL

BMN: Product code of MP4571GQBE (Wettable flank)
Y: Year code
WW: Week code
LLL: Lot number

PACKAGE REFERENCE



QFN-12 (2.5mmx3mm)

PIN FUNCTIONS

Pin #	Name	Description
1	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
2	SW	**Switch output.** SW is the output of the internal power switches. A wide PCB trace is recommended.
3	PG	**Power good indicator.** The pin is an open drain; it requires a pull-up resistor to the power source. PG is pulled up to the power source if the output voltage is within 90% to 108% of the nominal voltage. It goes low when the output voltage exceeds 116% or falls below 94% of the nominal voltage.
4	FB	**Feedback point.** FB is the negative input of the error amplifier. Connect FB to the tap of an external resistor divider between the output and GND to set the regulation voltage. In addition, power good and under-voltage lockout circuits use FB to monitor the output voltage.
5	FREQ	**Configurable switching frequency.** Connect a resistor to GND to set the switching frequency.
6	VCC	**Internal bias supply.** VCC supplies power to the internal control circuit and gate drivers. A minimum 1µF decoupling capacitor to ground is required close to this pin.
7	GND	**IC ground.** Connect the pin to larger copper areas to the negative terminals of the input and output capacitors.
8	IN	**Input supply.** This pin supplies all power to the converter. Place a decoupling capacitor to ground, as close as possible to the IC, to reduce switching spikes.
9, 10	NC	**No connection.** These pins can be connected to GND to improve thermal and EMI performance in PCB layout.
11	CCM/ SYNCO	**Mode selection/synchronization output.** Connect the CCM pin to GND through a 10kΩ to 300kΩ resistor to force the converter into CCM. Float the CCM pin for nonsynchronous AAM mode under light-load conditions. CCM/SYNCO is a synchronization output pin. It outputs a 180° out-of-phase clock to the other devices.
12	EN	**Enable.** Drive EN high to turn on the device; float or drive it low to turn off the device.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} 65V
V_{SW} .... -0.3V to V_{IN} + 0.3V
V_{BST} .... V_{SW} + 6V
All Other Pins .... -0.3V to +6V
Continuous power dissipation (T_A = 25°C) (2)
QFN-12 (2.5mmx3mm) 2.08W
Junction temperature .... 150°C
Lead temperature .... 260°C
Storage temperature .... -65°C to +150°C

Electrostatic Discharge (ESD) Rating

Human body model (HBM) .... ±2kV
Charged device model (CDM) .... ±750V

Recommended Operating Conditions

Continuous supply voltage (V_{IN}).......4.5V to 60V
Output voltage (V_{OUT})...................1V to 0.9 x V_{IN}
Load current range .... 0A to 1A
Operating junction temp (T_J)……………………..
……………………………….. -40°C to +125°C (3)

Thermal Resistance

	θ_{JA}	θ_{JC}	
QFN-12 (2.5mmx3mm)			
JESD51-7 (4)	60	13	°C/W
EVQ4571-QB-00A (5)	45	11	°C/W

Notes:

1) Absolute maximum ratings are rated under room temperature unless otherwise noted. Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J (MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the module will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) This device is not guaranteed to function outside its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) Measured on MPS standard EVB: 8.9cmx8.9cm, 2oz. copper, 4-layer PCB.

Electrical CharacteristicS

V_{IN} = 24V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply and UVLO						
Supply current (quiescent)	I_Q	No load, V_{FB} = 0.85V, AAM		40	65	μA
Supply current (shutdown)	I_{SD}	V_{EN} = 0V		2	5	μA
V_{IN} under-voltage lockout rising threshold	$INUV_{Vth\text{-}R}$		3.8	4.0	4.2	V
V_{IN} under-voltage lockout falling threshold	$INUV_{Vth\text{-}F}$		3.3	3.5	3.7	V
V_{IN} UVLO threshold hysteresis	$INUV_{HYS}$			500		mV
Output and Regulation						
Regulated FB reference	V_{REF}	T_J = 25°C	0.792	0.800	0.808	V
		T_J = -40°C to +125°C	0.784		0.816	V
FB input current	I_{FB}	V_{FB} = 0.85V		10	50	nA
Switches and Frequency						
High-side switch on resistance	$R_{DSON\text{-}H}$	V_{BST} - V_{SW} = 5V, T_J = 25°C	150	250	350	mΩ
		V_{BST} - V_{SW} = 5V, T_J = -40°C to +125°C	100		500	
Low-side switch on resistance	$R_{DSON\text{-}L}$	T_J = 25°C	30	45	60	mΩ
		T_J = -40°C to +125°C	20		90	
SW leakage current	$I_{SW\text{-}LKG}$	V_{EN} = 0V, V_{SW} = 0V or 60V		0.1	30	μA
Switching frequency	f_{SW}	R_{FREQ} = 76.8kΩ	300	400	500	kHz
		R_{FREQ} = 28kΩ	750	1000	1250	kHz
		R_{FREQ} = 12.1kΩ	1800	2200	2700	kHz
Minimum on time (7)	$t_{ON\text{-}MIN}$			90		ns
Minimum off time (7)	$t_{OFF\text{-}MIN}$			100		ns
Power Good (PG) Indicator						
PG sink current capacity	$V_{PG\text{-}SINK}$	Sink 4mA			300	mV
PG delay time	$t_{PG\text{-}DELAY}$	Rising edge		70		μs
		Falling edge		25		μs
PG leakage current	$I_{PG\text{-}LKG}$			10	1000	nA
PG rising threshold (V_{FB} / V_{REF})	PG_{RISING}	V_{FB} rising		90		%
		V_{FB} falling		108		%
PG falling threshold (V_{FB} / V_{REF})	$PG_{FALLING}$	V_{FB} falling		84		%
		V_{FB} rising		116		%
Enable (EN) Control						
EN input rising threshold	$V_{EN\text{-}RISING}$		1.38	1.45	1.52	V
EN input falling threshold	$V_{EN\text{-}FALLING}$		1.05	1.12	1.19	V
EN threshold hysteresis	$V_{EN\text{-}HYS}$			330		mV
EN input current	I_{EN}	V_{EN} = 2V		0.7		μA
EN turn-off delay	$t_{EN\text{-}DELAY}$		5			μs
BST						
BST-SW UVLO				1.4	2.5	V
BST-SW UVLO hysteresis				60		mV
Soft Start and VCC						
Soft-start time	t_{SS}			0.45		ms
VCC regulator	V_{CC}	I_{CC} = 0mA	4.6	4.9	5.2	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{EN} = 2V, T_J = -40°C to +125°C (6), typical values are at T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Protections						
Peak current limit	$I_{PEAK-LIMIT}$	20% duty cycle	1.4	1.95	2.5	A
Valley current limit	$I_{VALLEY-LIMIT}$		1.4			A
Zero cross threshold	I_{ZCD}	AAM	-100	140	+300	mA
Negative current limit	$I_{NEG-LIMIT}$	FCCM	-2	-1.3	-0.8	A
Thermal shutdown (7)	T_{SD}	Temperature rising		170		°C
Thermal shutdown hysteresis (7)	T_{SD-SYS}			25		°C

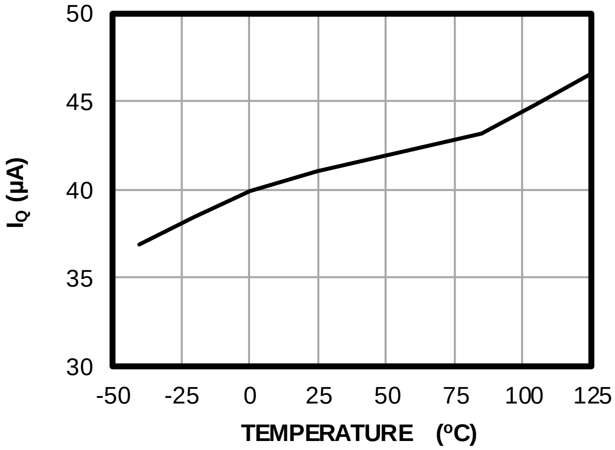
Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Derived from the bench characterization. Not tested in production.

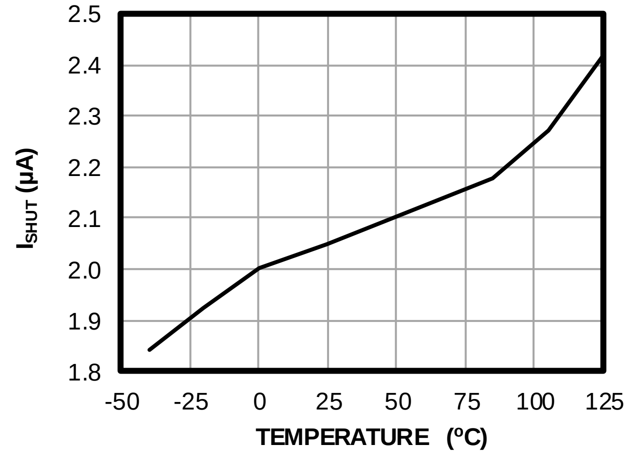
TYPICAL CHARACTERISTICS

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

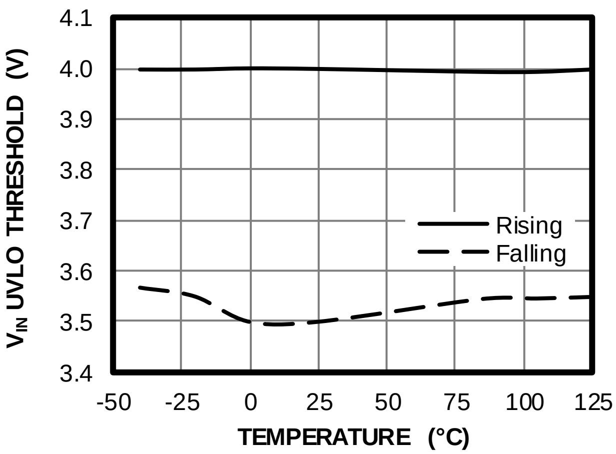
Quiescent Current vs. Temperature



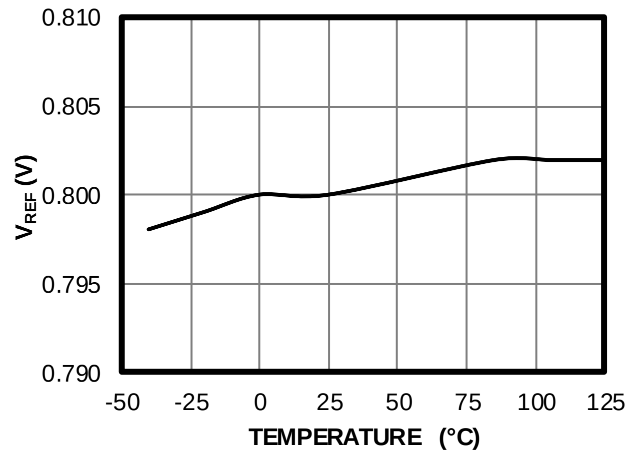
Shutdown Current vs. Temperature



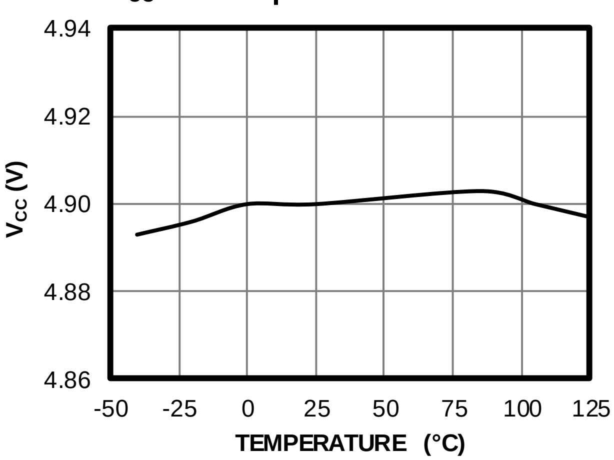
V_{IN} UVLO Threshold vs. Temperature



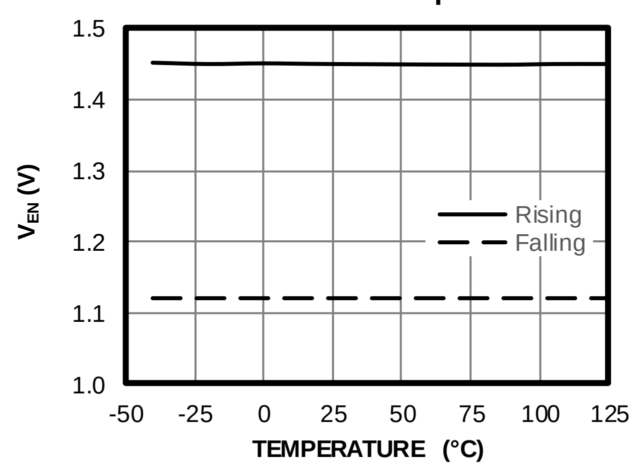
Feedback Reference vs. Temperature



V_{CC} vs. Temperature



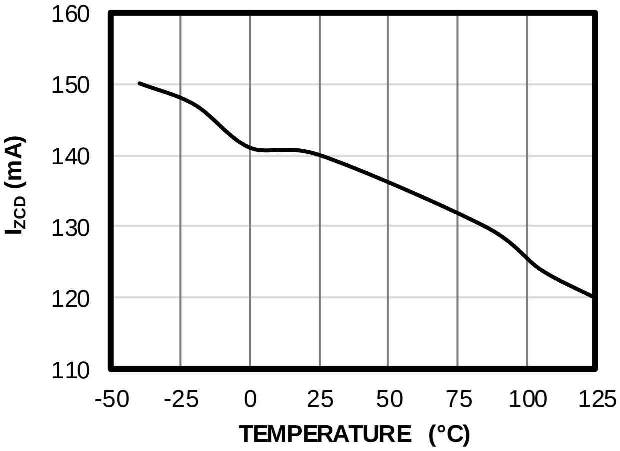
EN Threshold vs. Temperature



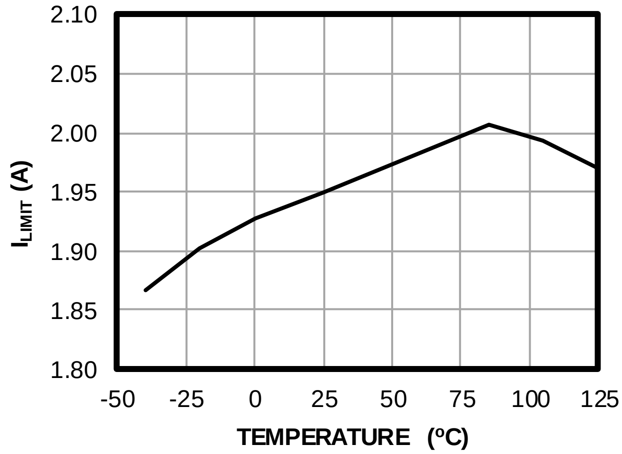
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

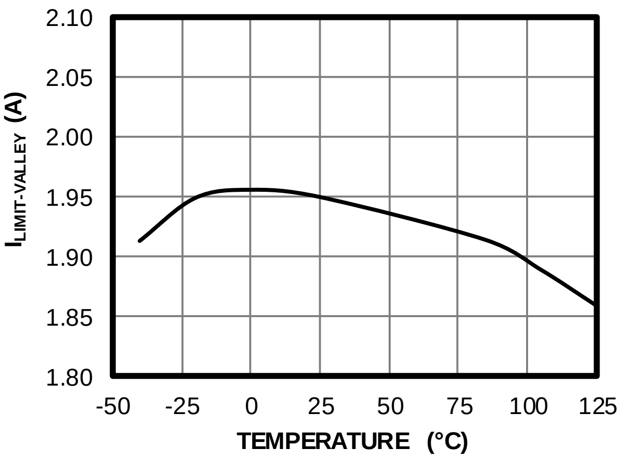
Zero-Current Detection vs. Temperature



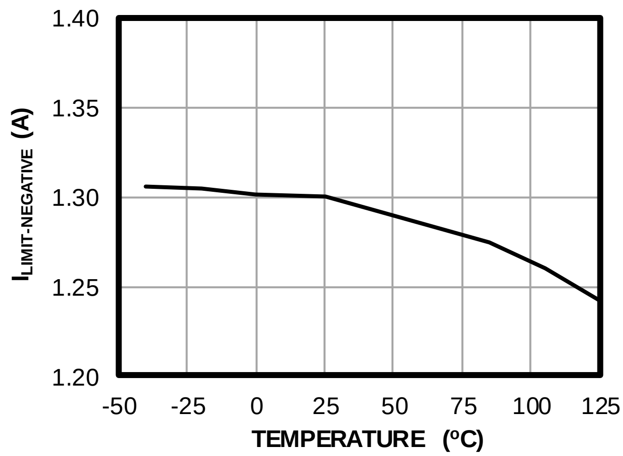
Peak Current Limit vs. Temperature



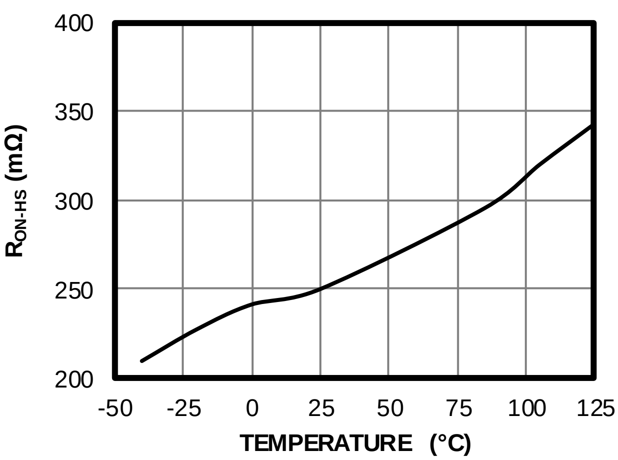
Valley Current Limit vs. Temperature



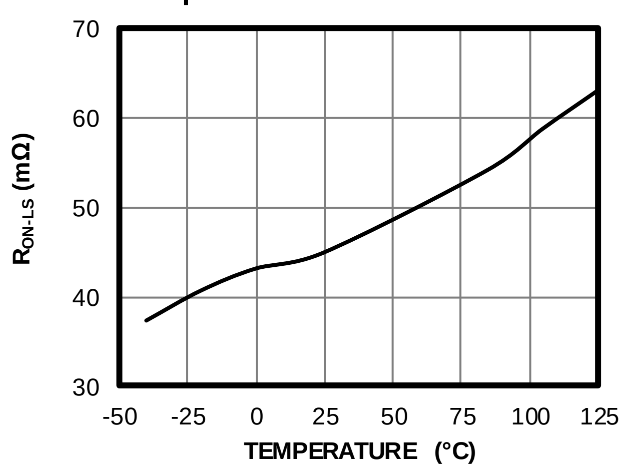
Negative Current Limit vs. Temperature



HS-FET On Resistance vs. Temperature



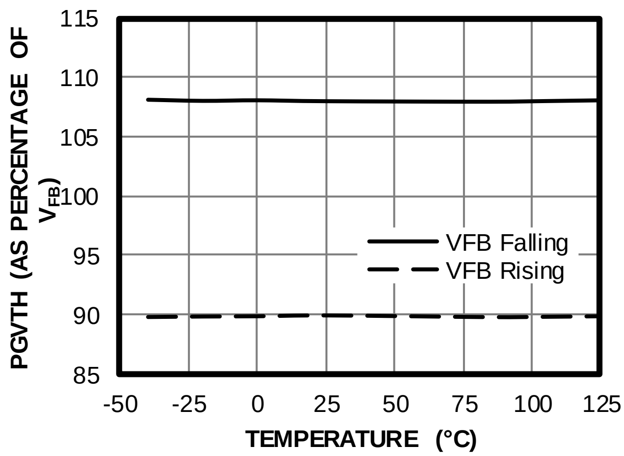
LS-FET On Resistance vs. Temperature



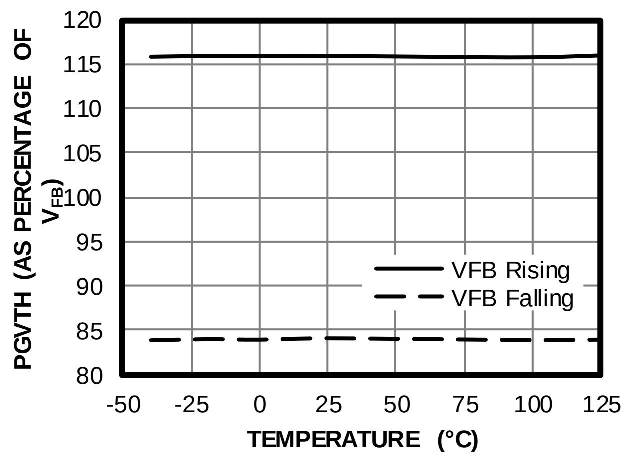
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = -40°C to +125°C, unless otherwise noted.

PG Rising Threshold vs. Temperature



PG Falling Threshold vs. Temperature

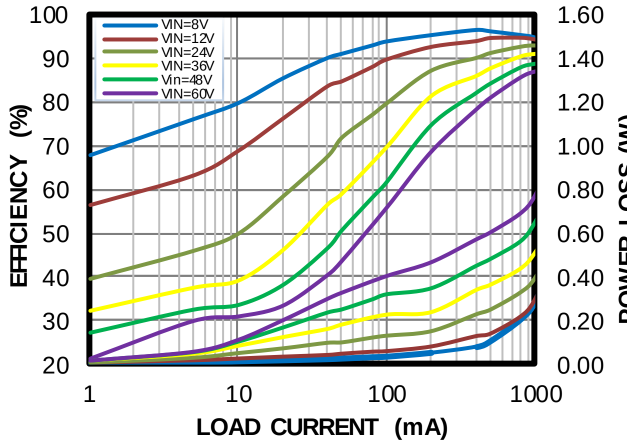


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 5V, L = 15µH, f_{SW} = 400kHz, AAM, T_A = 25°C, unless otherwise noted.

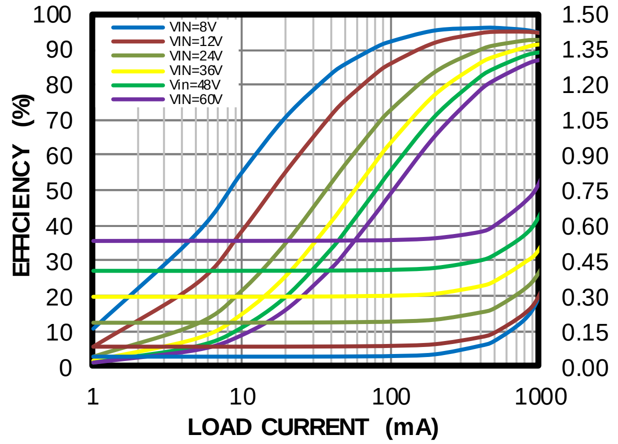
Efficiency vs. Load Current

f_{SW} = 400kHz, L = 15µH, AAM



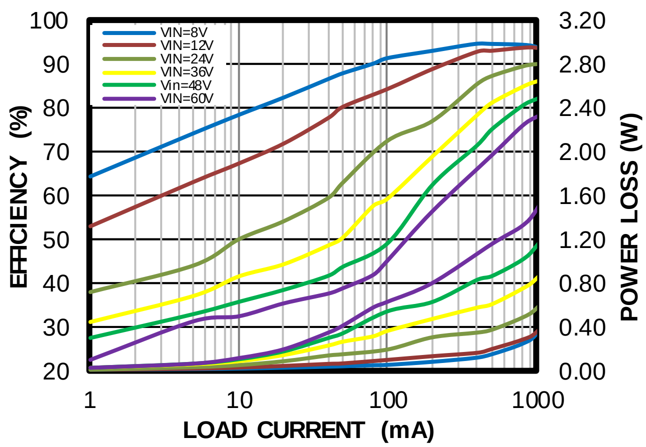
Efficiency vs. Load Current

f_{SW} = 400kHz, L = 15µH, CCM



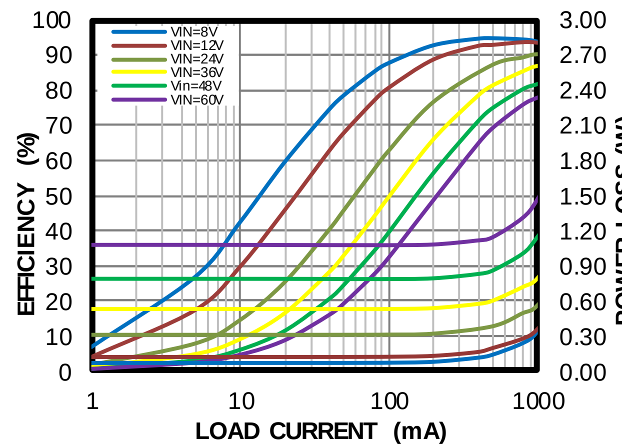
Efficiency vs. Load Current

f_{SW} = 1MHz, L = 10µH, AAM



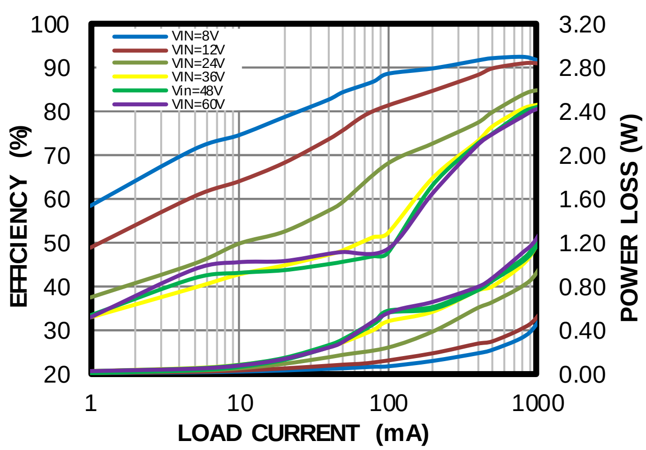
Efficiency vs. Load Current

f_{SW} = 1MHz, L = 10µH, CCM



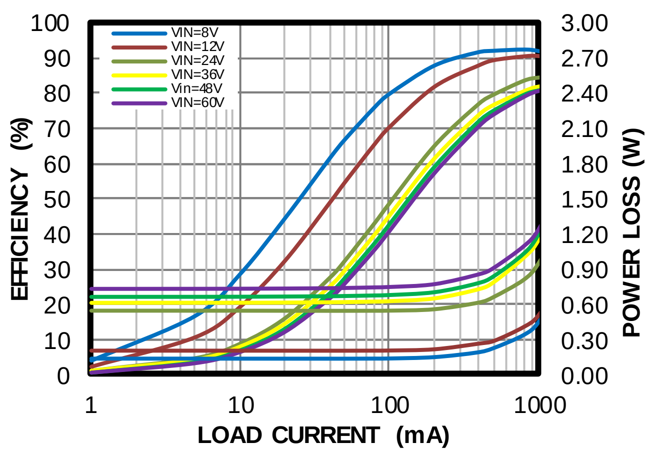
Efficiency vs. Load Current

f_{SW} = 2.2MHz, L = 4.7µH, AAM



Efficiency vs. Load Current

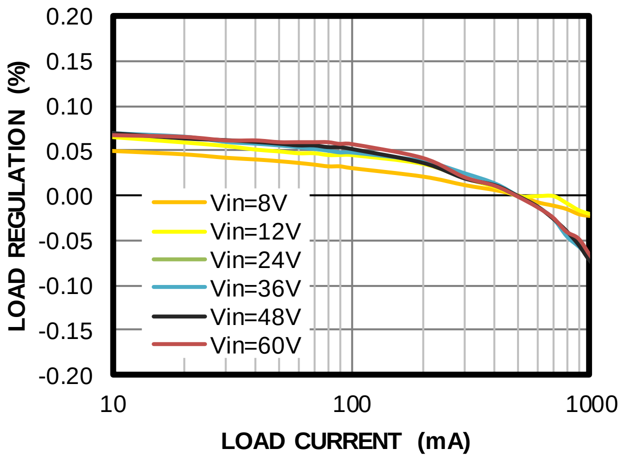
f_{SW} = 2.2MHz, L = 4.7µH, CCM



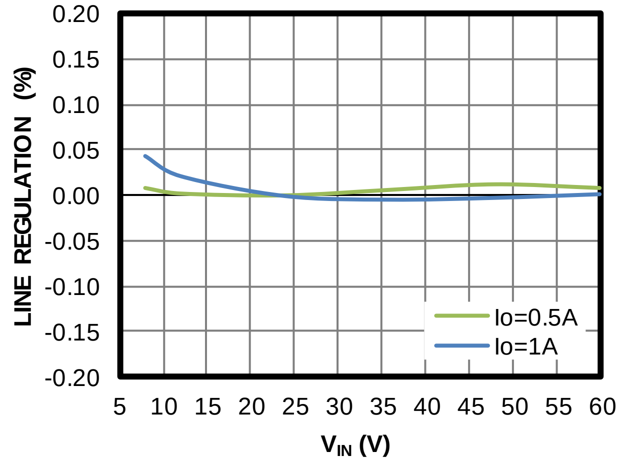
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 15µH, f_{SW} = 400kHz, AAM, T_A = 25°C, unless otherwise noted.

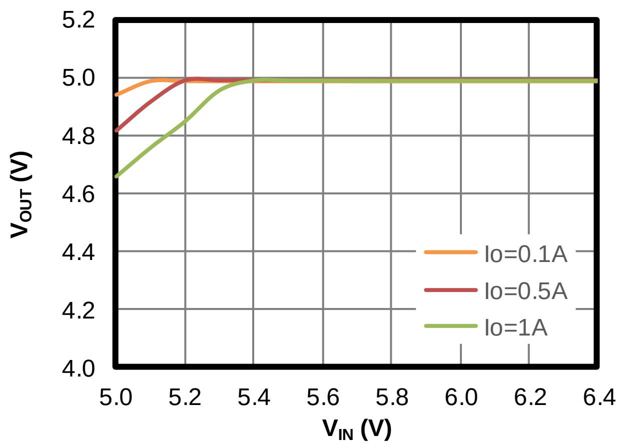
Load Regulation



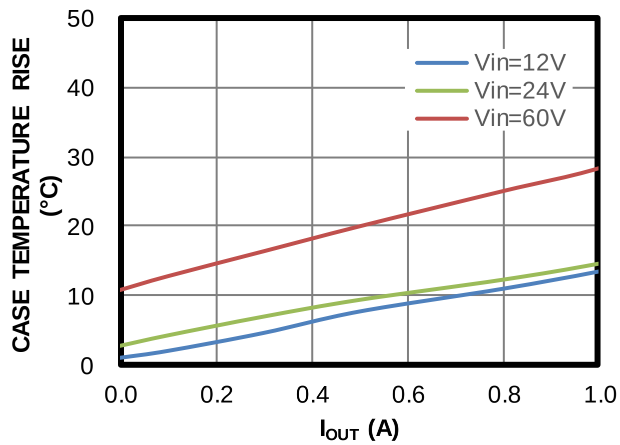
Line Regulation



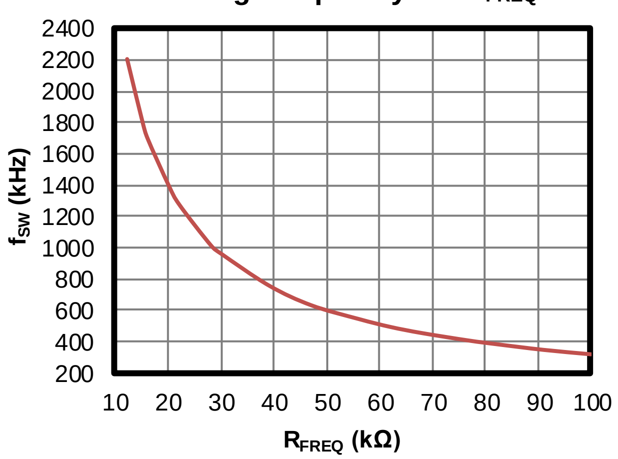
Dropout vs. Input Voltage



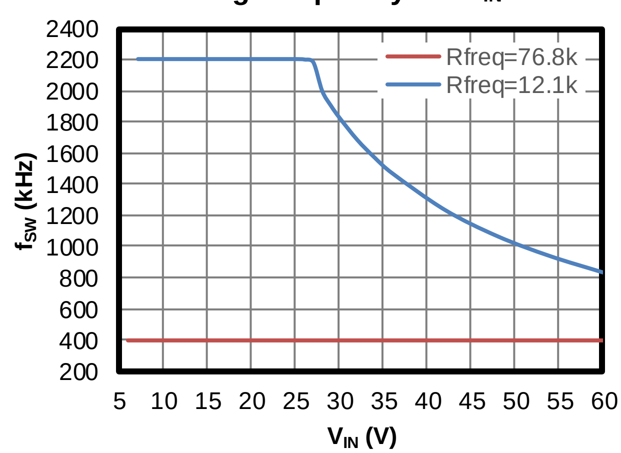
Case Temp Rise vs. Load Current



Switching Frequency vs. R_{FREQ}



Switching Frequency vs. V_{IN}

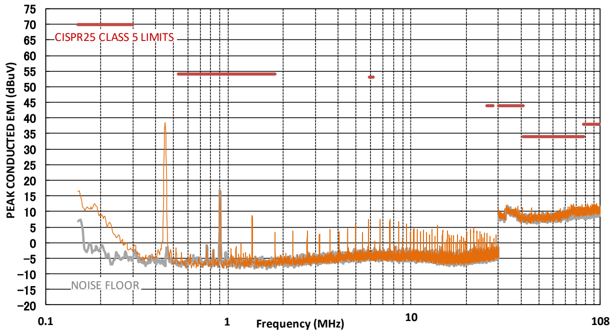


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 15µH, f_{SW} = 450kHz, AAM, T_A = 25°C, unless otherwise noted. [8]

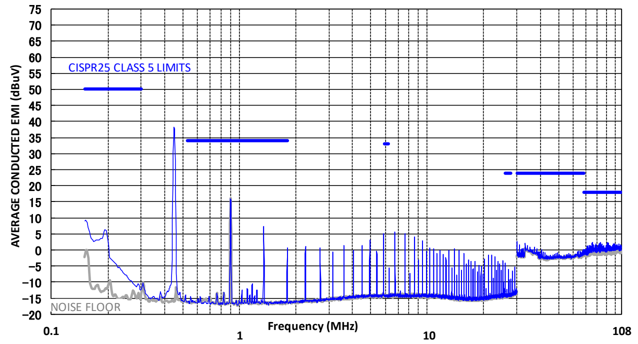
CISPR25 Class 5 Peak Conducted Emissions

150kHz to 108MHz



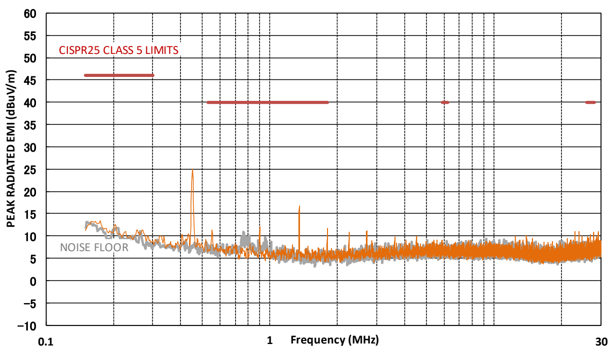
CISPR25 Class 5 Average Conducted Emissions

150kHz to 108MHz



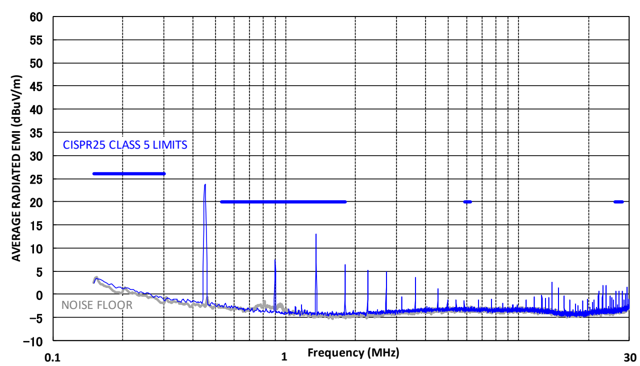
CISPR25 Class 5 Peak Radiated Emissions

150kHz to 30MHz



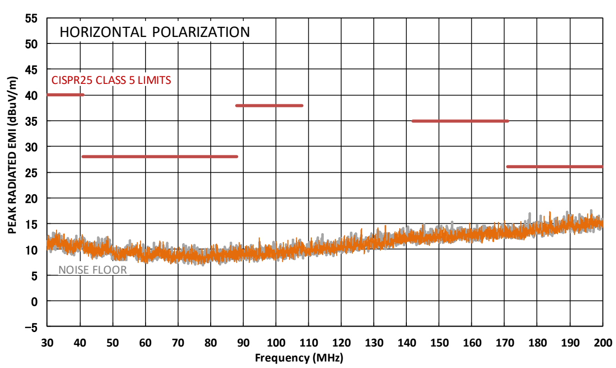
CISPR25 Class 5 Average Radiated Emissions

150kHz to 30MHz



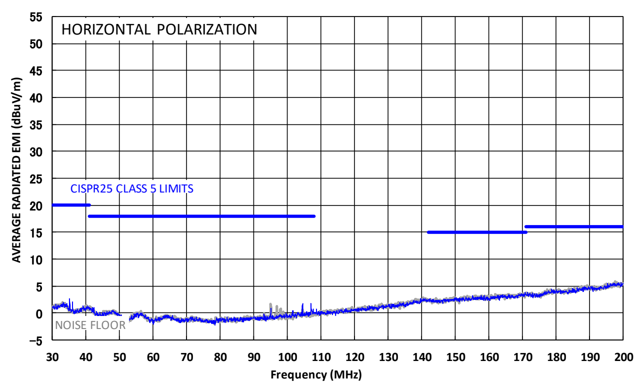
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 30MHz to 200MHz



CISPR25 Class 5 Average Radiated Emissions

Horizontal, 30MHz to 200MHz

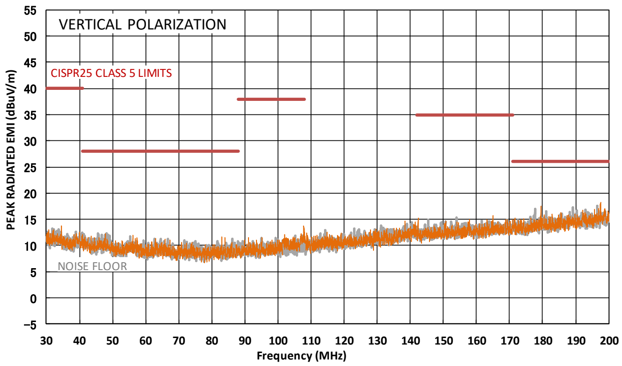


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{OUT} = 5V, L = 15µH, f_{SW} = 450kHz, AAM, T_A = 25°C, unless otherwise noted.

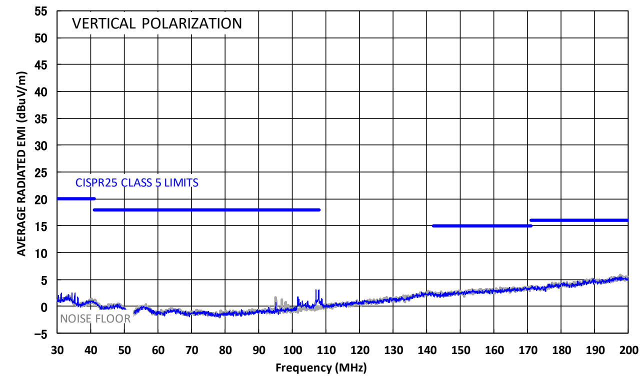
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 30MHz to 200MHz



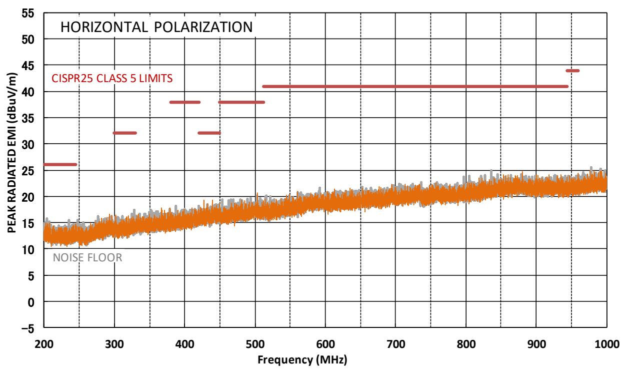
CISPR25 Class 5 Average Radiated Emissions

Vertical, 30MHz to 200MHz



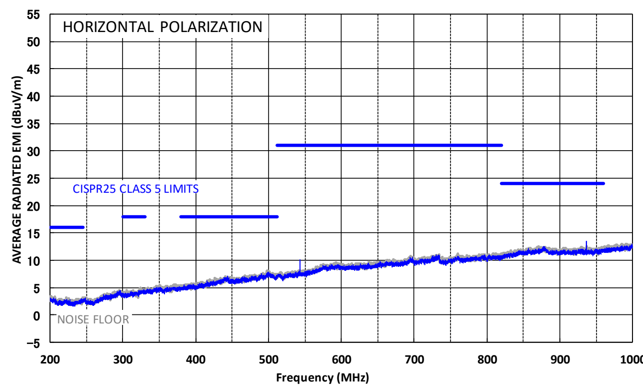
CISPR25 Class 5 Peak Radiated Emissions

Horizontal, 200MHz to 1GHz



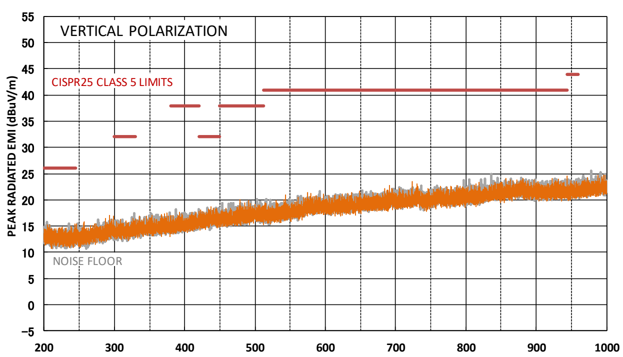
CISPR25 Class 5 Average Radiated Emissions

Horizontal, 200MHz to 1GHz



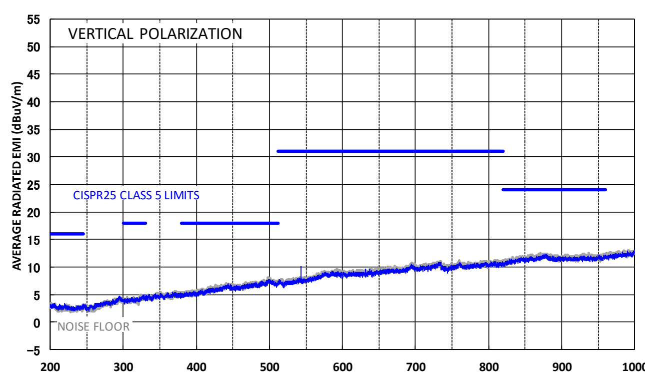
CISPR25 Class 5 Peak Radiated Emissions

Vertical, 200MHz to 1GHz



CISPR25 Class 5 Average Radiated Emissions

Vertical, 200MHz to 1GHz



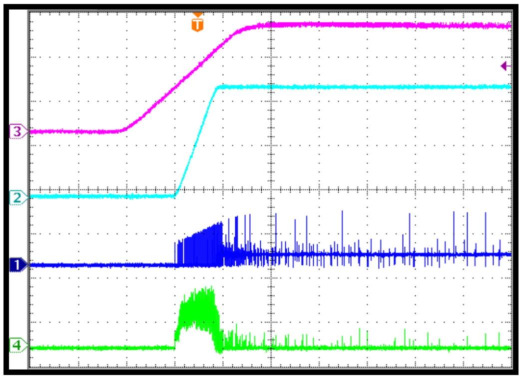
Note:

8) The EMC test results are based on the application circuit with EMI filters (see Figure 8) and are tested on the EVQ4571-QB-00A.

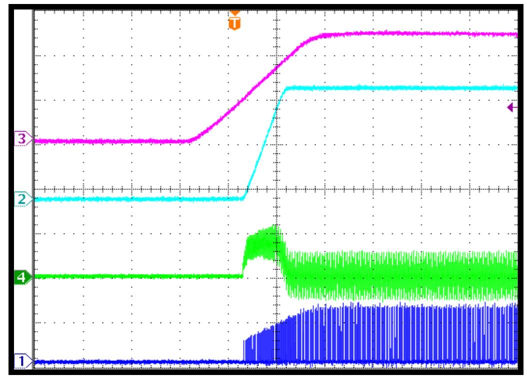
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 15µH, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

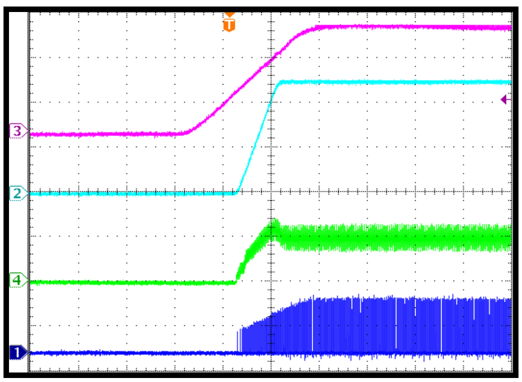
Start-Up through Input Voltage
I_{OUT} = 0A, AAM



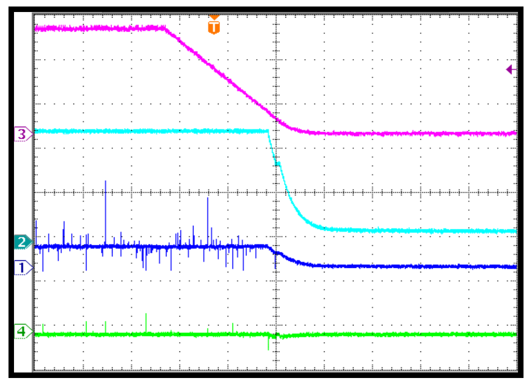
Start-Up through Input Voltage
I_{OUT} = 0A, CCM



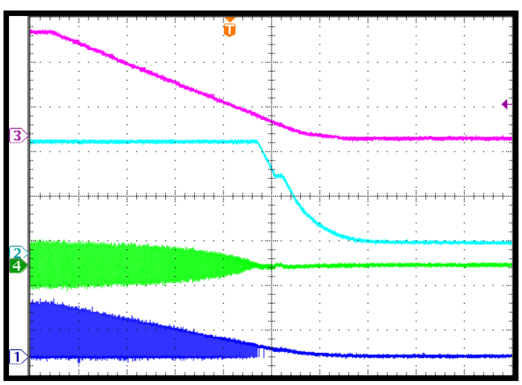
Start-Up through Input Voltage
I_{OUT} = 1A



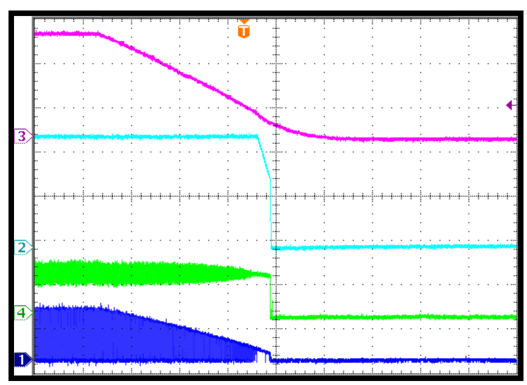
Shutdown through Input Voltage
I_{OUT} = 0A, AAM



Shutdown through Input Voltage
I_{OUT} = 0A, CCM



Shutdown through Input Voltage
I_{OUT} = 1A

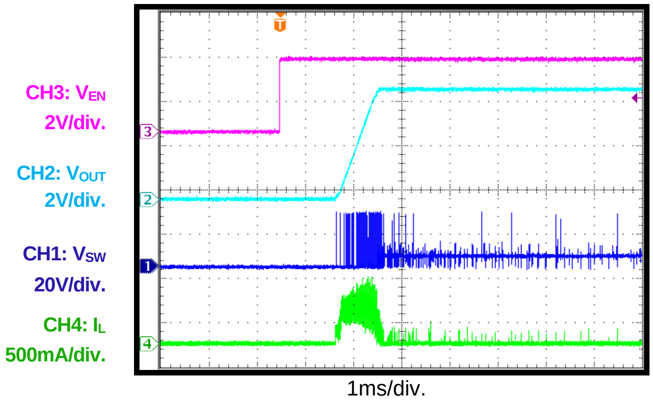


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 15µH, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

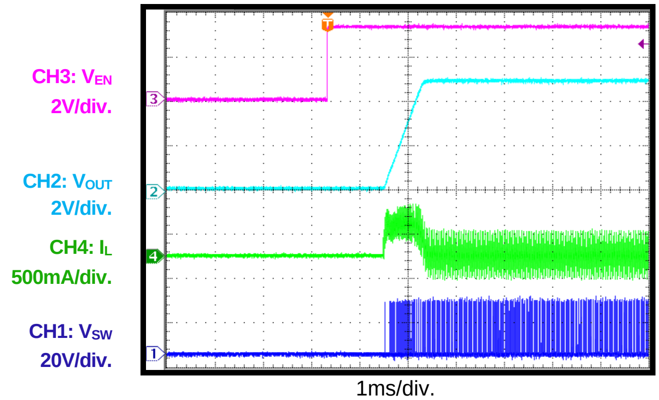
Start-Up through EN

I_{OUT} = 0A, AAM



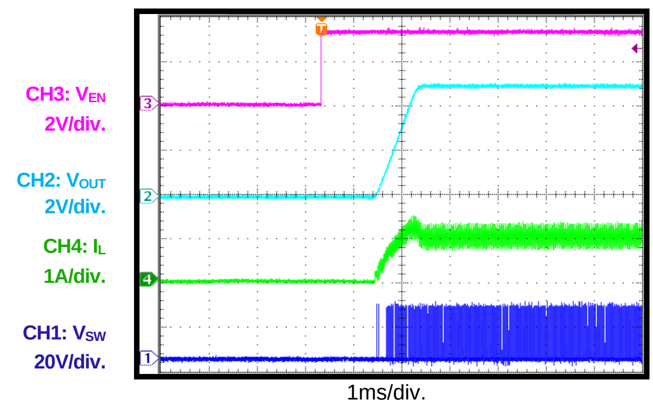
Start-Up through EN

I_{OUT} = 0A, CCM



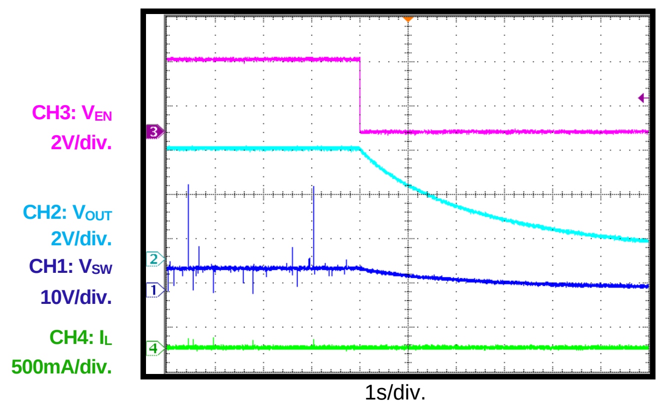
Start-Up through EN

I_{OUT} = 1A



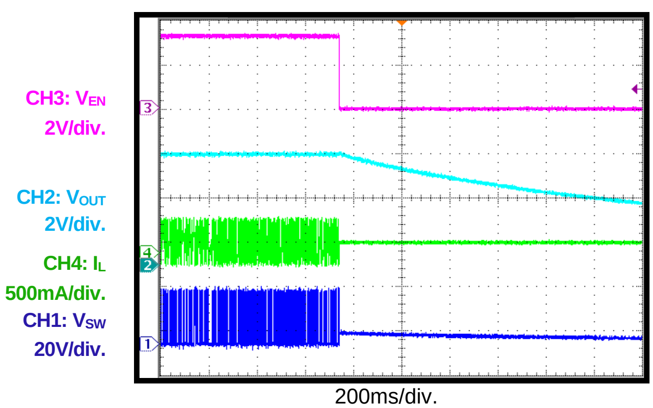
Shutdown through EN

I_{OUT} = 0A, AAM



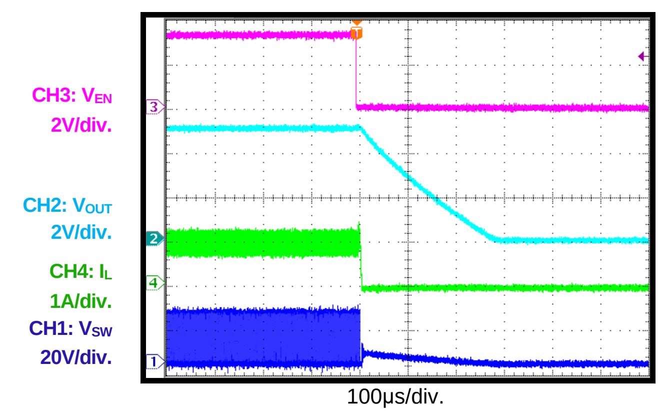
Shutdown through EN

I_{OUT} = 0A, CCM



Shutdown through EN

I_{OUT} = 1A

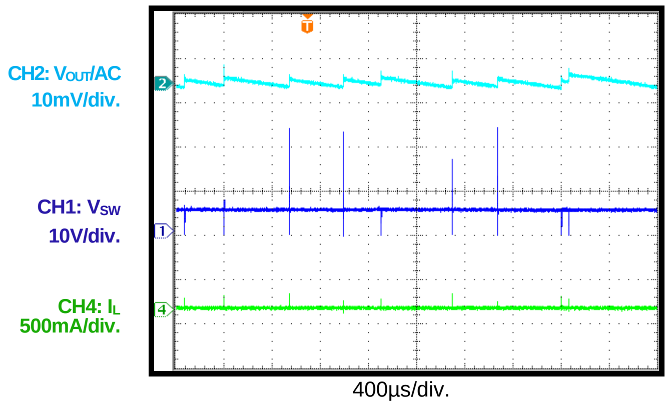


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 15µH, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

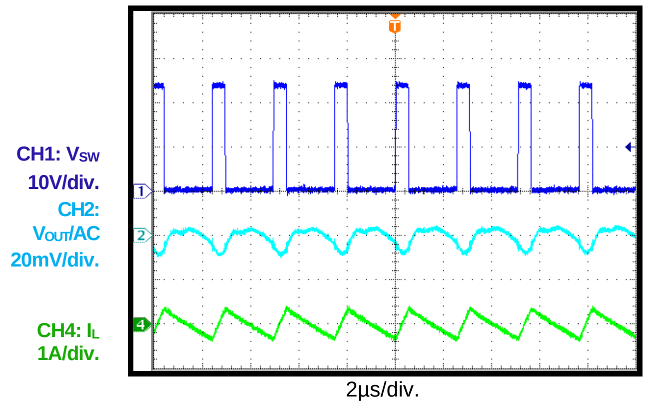
Output Ripple

I_{OUT} = 0A, AAM



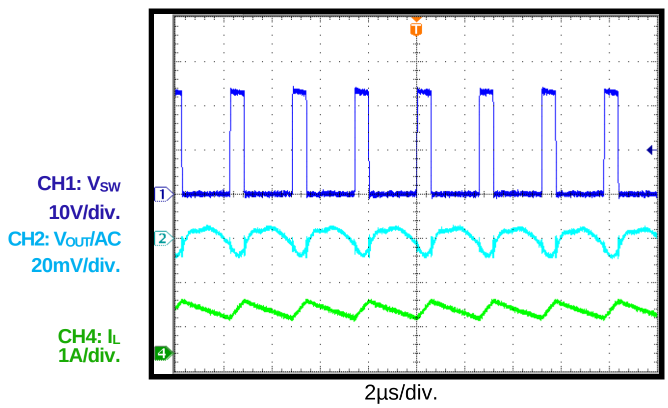
Output Ripple

I_{OUT} = 0A, CCM



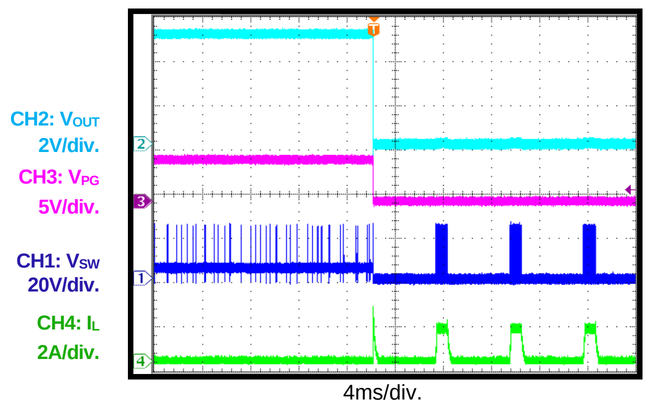
Output Ripple

I_{OUT} = 1A



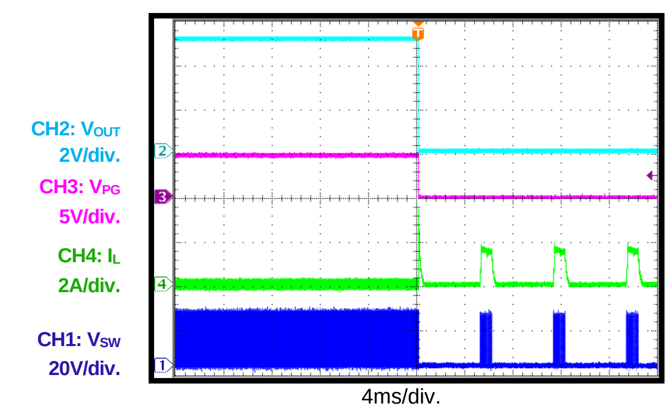
SCP Entry

I_{OUT} = 0A, AAM



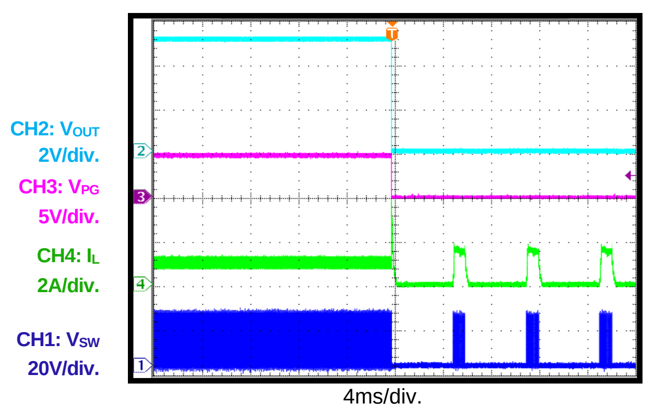
SCP Entry

I_{OUT} = 0A, CCM



SCP Entry

I_{OUT} = 1A

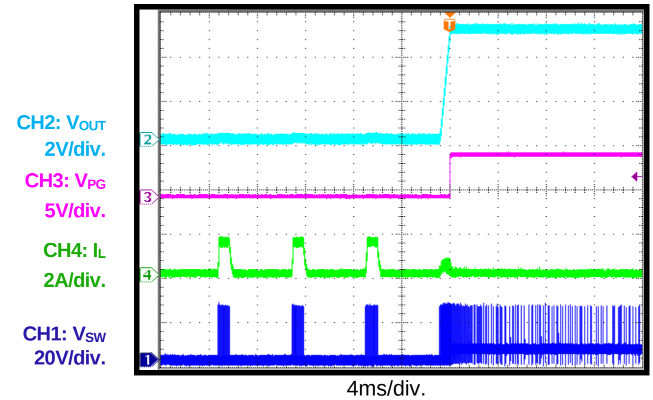


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 15µH, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

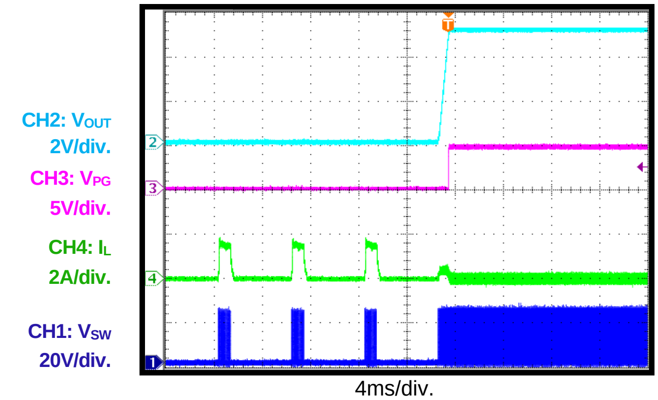
SCP Recovery

I_{OUT} = 0A, AAM



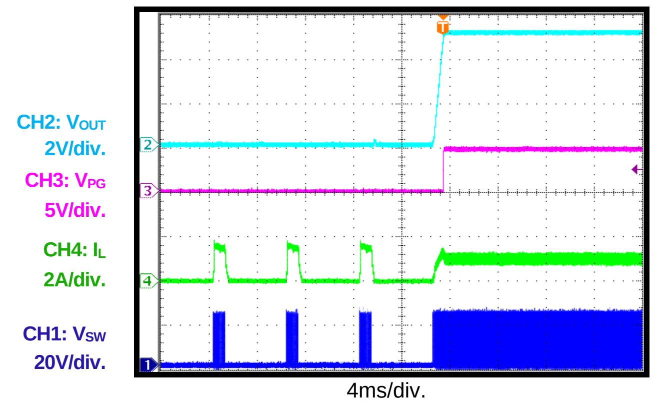
SCP Recovery

I_{OUT} = 0A, CCM

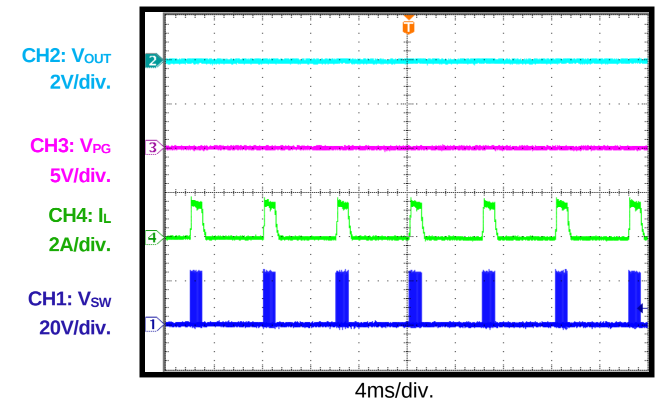


SCP Recovery

I_{OUT} = 1A

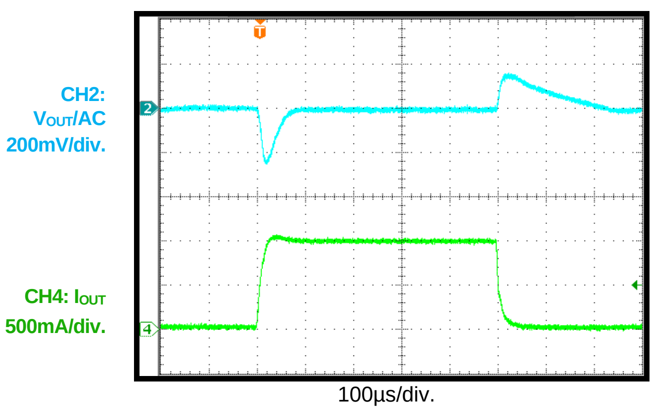


SCP Steady State



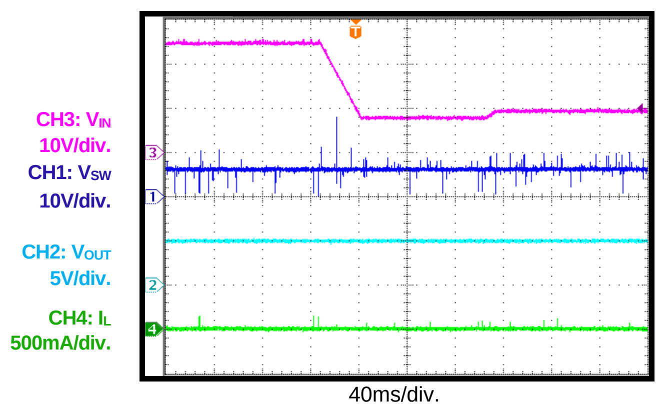
Load Transient

I_{OUT} = 0A to 1A, AAM



Cold Crank

V_{IN} = 24V to 4V to 5V, I_{OUT} = 0A

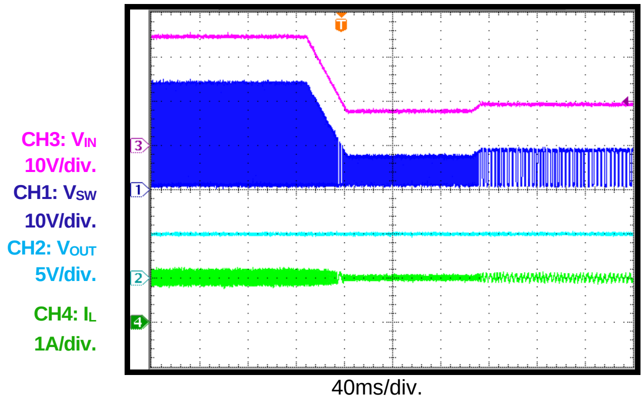


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 15µH, f_{SW} = 400kHz, T_A = 25°C, unless otherwise noted.

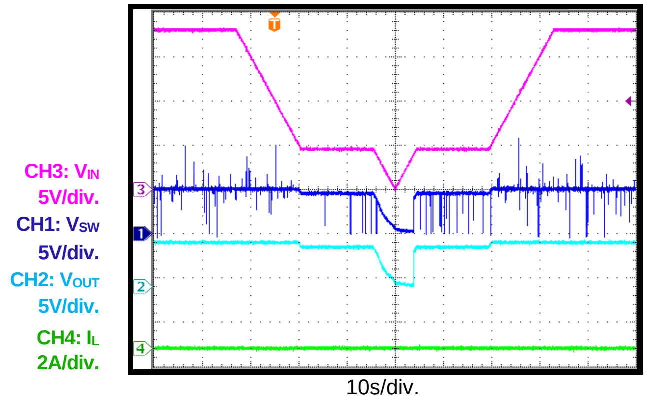
Cold Crank

V_{IN} = 24V to 4V to 5V, I_{OUT} = 1A



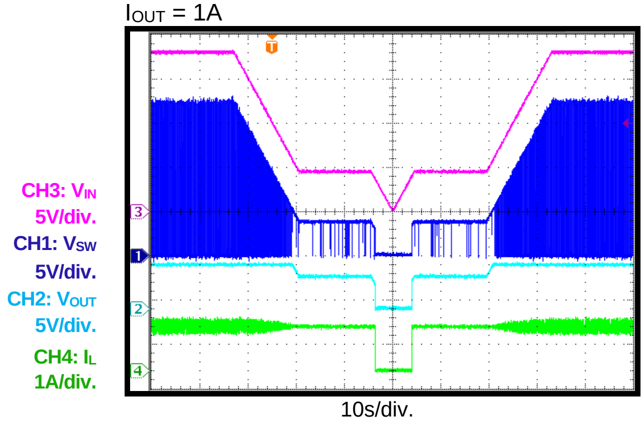
VIN Ramp Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to 18V, I_{OUT} = 0A



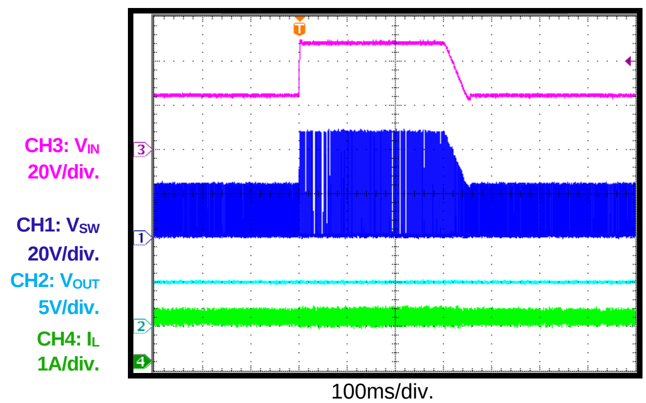
VIN Ramp Down and Up

V_{IN} = 18V to 4.5V to 0V to 4.5V to 18V, I_{OUT} = 1A



Load Dump

V_{IN} = 24V to 48V to 24V, I_{OUT} = 1A



FUNCTIONAL BLOCK DIAGRAM

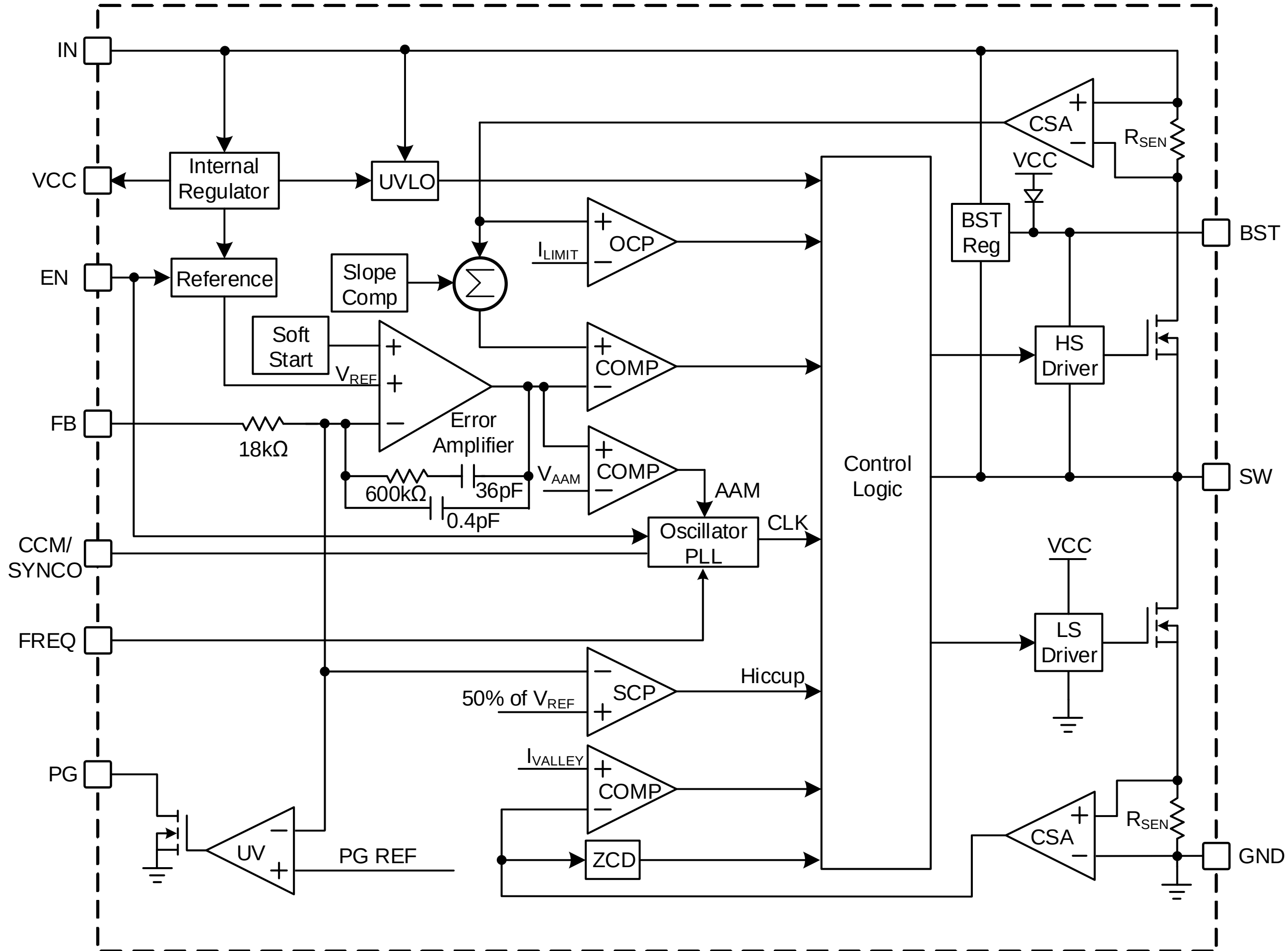


Figure 1: Functional Block Diagram

OPERATION

The MP4571 is a fully integrated, synchronous, rectified, step-down, non-isolated switch-mode converter. It offers a wide 4.5V to 60V input supply range, and can achieve up to 1A of continuous output current with excellent load and line regulation across an ambient temperature range of -40°C to +125°C. Figure 1 shows a block diagram of the device.

PWM Control

At moderate to high output currents, the MP4571 operates in fixed-frequency, peak current control mode to regulate the output voltage.

An internal clock initiates a PWM cycle. At the rising edge of the clock, the high-side switch (HS-FET) turns on, and the inductor current rises linearly to provide energy to the load. The HS-FET remains on until the current reaches the value set by the COMP voltage (V_{COMP}), which is the output of the internal error amplifier. V_{COMP} is based on the difference between the output feedback voltage and internal high-precision reference. V_{COMP} determines how much energy should be transferred to the load. A higher load current creates a higher V_{COMP}. Once the HS-FET is on, it remains on for at least 90ns.

When the HS-FET is off, the low-side switch (LS-FET) turns on immediately, and stays on until the next clock starts. During this time, the inductor current flows through the LS-FET. Once the LS-FET is on, it remains on for at least 100ns before the next cycle starts. To avoid shoot-through, a dead time is inserted to prevent the HS-FET and LS-FET from turning on simultaneously.

If the current in the HS-FET does not reach the COMP set current value within one PWM period, the HS-FET remains on, saving a turn-off operation.

Light-Load Operation

The MP4571 features configurable forced continuous conduction mode (FCCM) and light-load asynchronous advanced mode (AAM), which can be set by the CCM/SYNCO pin. FCCM maintains a constant switching frequency and smaller output ripple. However, FCCM has low efficiency during light-load conditions, while AAM achieves high efficiency (see Figure 2).

To force the device into FCCM, connect the CCM/SYNCO pin to GND using a 10kΩ to 300kΩ resistor. In FCCM, the converter works with a fixed frequency across a no-load to full-load range. Float the CCM/SYNCO pin to force the device into AAM under light-load conditions. The device cannot change modes while it is operating, so the mode must be selected before start-up.

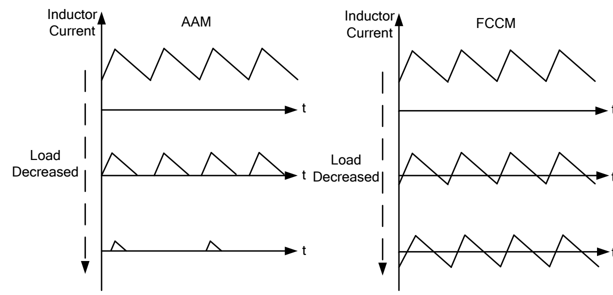


Figure 2: AAM and FCCM

When AAM is enabled, the switching frequency is scaled down according to V_{COMP} during light-load conditions. The MP4571 first enters nonsynchronous operation while the inductor current approaches zero at light-load. If the load further decreases or is at no-load, V_{COMP} drops below the internally set AAM value (V_{AAM}). The MP4571 then enters sleep mode and consumes a low quiescent current to improve light-load efficiency.

In sleep mode, the internal clock is blocked, so the MP4571 skips some pulses. V_{FB} is below V_{REF}, so V_{COMP} ramps up until it exceeds V_{AAM}. Then the internal clock is reset, and the crossover time is used as the benchmark for the next clock. This control scheme helps the device achieve high efficiency by scaling down the frequency to reduce switching and gate driver losses.

As the output current increases from light load, both V_{COMP} and the switching frequency rise. If the output current exceeds the critical level set by V_{COMP}, the MP4571 enters discontinuous conduction operation (DCM) or CCM, which has a constant switching frequency.

Enable (EN) Control

The MP4571 can be enabled or disabled via a remote EN signal that is referenced to ground. The remote EN control operates with a positive logic that is compatible with popular logic devices. Positive logic indicates that when the input voltage exceeds the under-voltage lockout (UVLO) threshold (about 4.0V), the converter is enabled by pulling the EN pin above 1.45V. Drive the EN pin below 1.12V to disable the MP4571. An internal resistor (R_{EN}) from EN to GND allows EN to be floated to shut down the chip (R_{EN} = 2.8MΩ when EN is on; R_{EN} = 1.8MΩ when EN is off).

SYNCO

The MP4571 has a SYNCO pin. During start-up, SYNCO stays low and quickly outputs a 180° phase-shift clock to the internal oscillator once soft start is ready. Note that the falling edge of SYNCO is a 180° phase-shift to the rising edge of the internal oscillator. This function allows two devices to operate in the same frequency, but 180° out of phase, which reduces the total input current ripple. This allows a smaller input bypass capacitor to be used.

Internal Regulator

A 4.9V internal regulator powers most of the internal circuitries. This regulator takes V_{IN} and operates in the full V_{IN} range. When V_{IN} exceeds 4.9V, the output of the regulator is in full regulation. Lower V_{IN} values result in lower output voltages. The regulator is enabled when V_{IN} exceeds its under-voltage lockout (UVLO) threshold and EN is high. In EN shutdown mode, the internal VCC regulator is disabled to reduce power dissipation.

Frequency Programmable and Foldback

The oscillating frequency (f_{SW}) of the MP4571 is configured by an external frequency resistor. The frequency resistor should be located between FREQ pin and GND, as close as possible to the device. Select a proper R_{FREQ}, calculated with Equation (1):

$$R_{FREQ}(M\Omega) = \frac{30}{f_{sw}(kHz)} \qquad (1)$$

The calculated resistance may need fine-tuning with a bench test.

It is not possible to use a high f_{SW} with a high V_{IN}, since the minimum on time required for the HS-FET is limited. The MP4571 control loop automatically sets the maximum possible f_{SW} up to the set frequency, which also reduces excessive power loss in the IC. V_{OUT} is regulated by varying the duration of the switch-off time of the HS-FET, which results in an automatic reduction of f_{SW}.

Compliance with the minimum on time of the HS-FET is guaranteed. An advantage of this method is that the device works at the desired f_{SW} as long as possible, and a correction is only made at high V_{IN}. For the Switching Frequency vs. V_{IN} curve, see the Typical Performance Characteristics section on page 12, where R_{FREQ} equals 12.1kΩ.

Internal Soft Start (SS)

To avoid overshoot during start-up, the MP4571 has built-in soft start (SS) that ramps up the output voltage at a controlled slew rate when the EN pin goes high. When the SS voltage (V_{SS}) is below the internal reference (V_{REF}), V_{SS} overrides V_{REF} as the error amplifier reference. When V_{SS} exceeds V_{REF}, V_{REF} acts as the reference. At this point, soft start finishes and the MP4571 enters steady-state.

The SS time is internally set to 0.45ms. When the output voltage is shorted to GND, the feedback voltage is pulled low and V_{SS} is discharged. The part initiates soft start again when it returns to a normal state.

Pre-Biased Start-Up

If V_{FB} exceeds V_{SS} during start-up, that means the output has a pre-biased voltage. Neither the HS-FET nor LS-FET turns on until V_{SS} exceeds V_{FB}. Note that the pre-biased capability is only available when the device is set to AAM.

Power Good (PG) Indicator

The MP4571 has power good (PG) indication. The PG pin is the open drain of a MOSFET. It should be connected to a voltage source through a resistor (e.g. 100kΩ). In the presence of an input voltage, the MOSFET turns on so that the PG pin is pulled to GND before soft start is ready. PG goes high if the output voltage is between 90% and 108% of the nominal voltage after a 70µs delay. PG goes low when the output voltage is above 116% or below 94% of the nominal voltage after a 25µs delay.

Under-Voltage Lockout Protection (UVLO)

The MP4571 has input under-voltage lockout protection (UVLO) to ensure reliable output power. Assuming EN is active, the MP4571 is powered on when the input voltage exceeds the UVLO rising threshold. The device is powered off when input voltage drops below the UVLO falling threshold. This function prevents the device from operating at an insufficient voltage. It is a non-latch protection.

Over-Current Protection (OCP)

The MP4571 has a 1.95A peak current limit. Once the inductor current reaches the current limit, the HS-FET turns off immediately. Then the LS-FET turns on to discharge the energy, and the inductor current decreases. The HS-FET does not turn on again until the inductor current drops below the current threshold (the valley current limit). This protection prevents the inductor current from running away and damaging the components.

Short-Circuit Protection (SCP)

When a short-circuit condition occurs, the MP4571 immediately reaches its current limit. Meanwhile, the output voltage drops until V_{FB} falls below 50% of V_{REF}. The device considers this an output dead short, and triggers hiccup short-circuit protection (SCP) mode to periodically restart the part.

In hiccup mode, the MP4571 disables its output power stage, slowly discharges the soft-start capacitor, then initiates a soft start. If the short-circuit condition remains after soft start ends, the device repeats this operation until the short circuit disappears and the output returns to the regulation level. This protection mode greatly reduces the average short-circuit current to alleviate thermal issues and protect the regulator.

Negative Current Protection

The MP4571 has a -1.3A negative current limit. Once the inductor current reaches the current limit, the LS-FET immediately turns off and the HS-FET turns on. The current limit prevents the negative current from dropping too low and damaging the components.

Thermal Shutdown

For thermal protection, the MP4571 monitors the IC temperature internally. This function prevents the chip from operating at exceedingly high temperatures. If the junction temperature exceeds the threshold value (about 170°C), it shuts down the whole chip. This is a non-latch protection. There is a 25°C hysteresis. Once the junction temperature drops to about 145°C, the device resumes operation by initiating a soft start.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating HS-FET driver. There are two methods to charge the bootstrap capacitor (see Figure 3).

The first method is through the main charging circuit from V_{CC} through a diode. When the HS-FET is on, V_{SW} is about equal to V_{IN} but exceeds V_{CC}, and the bootstrap capacitor is not charged. The best charging period occurs when the LS-FET is on, and V_{CC} - V_{SW} is at its largest. When there is no current in the inductor, V_{SW} equals V_{OUT}, so V_{CC} can only charge BST when V_{OUT} is very small.

The second method is through the auxiliary charging circuit from V_{IN}. When the voltage difference between BST and SW is below the internal 5V bootstrap regulator, a PMOS pass transistor (M1) turns on to charge the bootstrap capacitor. The charging current is much smaller than that from VCC, but as long as V_{IN} exceeds V_{SW}, BST can be charged. This function is useful in sleep mode, when there is not always a switch.

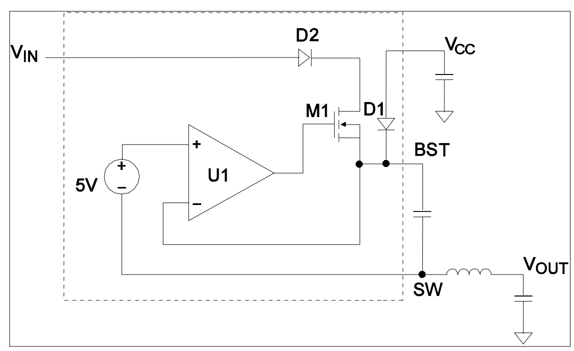


Figure 3: Internal Bootstrap Charging Circuit

Low-Dropout Operation (BST Refresh)

To improve dropout, the MP4571 is designed to operate at close to 100% duty cycle as long as the BST-to-SW voltage exceeds 1.4V. When the BST-to-SW voltage drops below 1.34V, the HS-FET turns off using a UVLO circuit, which allows the LS-FET to conduct and refresh the charge on the BST capacitor. When the input voltage drops, the HS-FET remains on and close to 100% duty cycle to maintain output regulation until the BST-to-SW voltage falls below 1.34V.

Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the capacitor. The means the effective duty cycle of the switching regulator is high.

The effective duty cycle during regulator dropout is mostly influenced by the voltage drops across the power MOSFET, inductor resistance, low-side diode, and PCB resistance.

Start-Up and Shutdown

If both V_{IN} and V_{EN} exceed their respective thresholds, the chip starts. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

While the internal supply rail is up, an internal timer holds the power MOSFET off for about 50µs to blank the start-up glitches. When the soft-start block is enabled, it first holds its SS output low to ensure the circuitries are ready, then slowly ramps up.

Three events can shut down the chip: EN going low, V_{IN} UVLO, and thermal shutdown. In the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command, but its charging path is disable.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider connected to the FB pin sets the output voltage (see the Typical Application Circuits on page 29). The feedback resistor (R1) must account for both stability and dynamic response, so it cannot be too large or too small. Choose an R1 value of about 40kΩ. R2 is then estimated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8} - 1} \tag{2}$$

Figure 4 shows the recommended T-type feedback network.

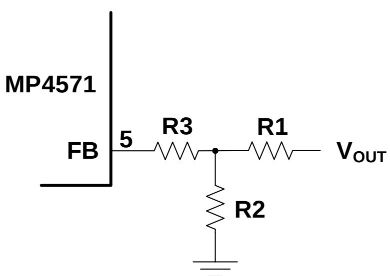


Figure 4: Feedback Network

R3 + R1 is used to set the loop bandwidth. A higher R3 + R1 indicates a lower bandwidth. To ensure loop stability, it is strongly recommended to limit the bandwidth between 1/10 of the switching frequency and 100kHz.

The calculated resistance may need fine-tuning via bench testing. Table 1 lists the recommended feedback divider resistor values for common output voltages. Use check loop analysis before using the device in an application, and change the resistance of R3 for loop stability if necessary.

Table 1: Resistor Values for Typical V_{OUT}

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
3.3	41.2	13
5.0	41.2	7.68

Selecting the Inductor

The inductor must supply constant current to the output load while being driven by the switching input voltage. For the highest efficiency, choose an inductor with a low DC resistance. High inductance will result in less ripple current and lower output ripple voltage. However, a larger inductance value results in a physically larger inductor, higher series resistance, and lower saturation current.

A good rule to determine the ideal inductance value is to make the inductor ripple current about 30% of the maximum load current. Ensure that the peak inductor current is below the device peak current limit. The inductance value can be calculated with Equation (3):

$$L = \frac{V_{OUT}}{f_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{3}$$

Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. Calculate the peak inductor current with Equation (4):

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2f_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{4}$$

Selecting the Input Capacitor

The step-down converter has a discontinuous input current, and requires a capacitor to supply the AC current to the converter while maintaining the DC input voltage. Use low-ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended because of their low ESR and small temperature coefficients. Other capacitors, such as Y5V and Z5U, should not be used since they lose too much capacitance with frequency, temperature, and bias voltage.

Place the input capacitors as close to the IN pin as possible. For most applications, a 22µF capacitor is sufficient. For higher output voltages, use a 47µF capacitor to improve system stability. To maintain a small solution size, choose a properly sized capacitor that has a voltage rating compliant with the input spec.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating that should exceed the converter's maximum input ripple current. The input ripple current can be estimated with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \tag{5}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (6)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, use a small, high-quality ceramic capacitor (0.1µF), placed as close to the IC as possible. The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system design, choose an input capacitor that meets the specification.

The input voltage ripple caused by the capacitance can be estimated with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, estimated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

Selecting the Output Capacitor

The output capacitor maintains the output DC voltage. Ceramic capacitors with low ESR are recommended for their small size and low output voltage ripple. Electrolytic and polymer capacitors may also be used. The output voltage ripple can be estimated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 f_{SW} \times C_{OUT}}) \quad (9)$$

Where R_{ESR} is the equivalent series resistance of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple. For simplification, the output voltage ripple can be calculated with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

Another consideration for the output capacitance is the allowable overshoot in V_{OUT} if the load is suddenly removed. In this case, energy stored in the inductor is transferred to C_{OUT}, causing its voltage to rise. To achieve a desired overshoot relative to the regulated voltage, the output capacitance can be estimated with Equation (12):

$$C_{OUT} = \frac{I_{OUT}^2 \times L}{V_{OUT}^2 \times ((V_{OUTMAX} / V_{OUT})^2 - 1)} \quad (12)$$

Where V_{OUTMAX} / V_{OUT} is the allowable maximum overshoot.

After calculating the capacitance required for both the ripple and overshoot, choose the larger value.

The characteristics of the output capacitor also affect the stability of the regulation system. The MP4571 can be optimized for a wide range of capacitance and ESR values.

V_{IN} Under-Voltage Lockout (UVLO) Setting

The MP4571 has an internal, fixed under-voltage lockout (UVLO) threshold. The rising threshold is 4.0V, while the falling threshold is about 3.5V. For applications that require a higher UVLO point, place an external resistor divider between EN and IN to obtain a higher equivalent UVLO threshold (see Figure 5 and Figure 6). Add a 6V Zener diode between EN to GND if the EN pin is connected to VIN through a resistor.

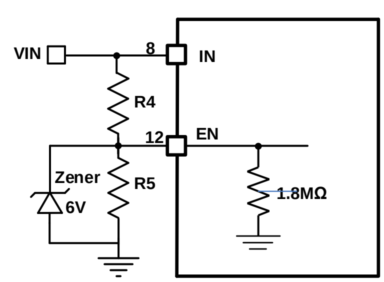


Figure 5: Adjustable UVLO Using EN Divider when EN Rises

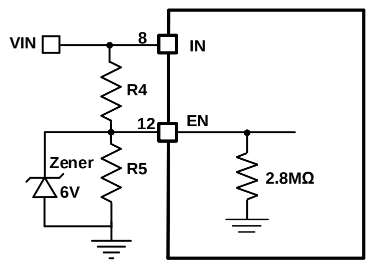


Figure 6: Adjustable UVLO Using EN Divider when EN Falls

The UVLO threshold can be calculated with Equation (13) and Equation (14) when EN is rising or falling, respectively:

$$INUV_{RISING} = (1 + \frac{R4}{1.8M//R5}) \times V_{EN\_RISING} \quad (13)$$

$$INUV_{FALLING} = (1 + \frac{R4}{2.8M//R5}) \times V_{EN\_FALLING} \quad (14)$$

Where V_{EN_RISING} = 1.45V, $V_{EN\_FALLING}$ = 1.12V.

When choosing R4, ensure it is big enough to limit the current flowing into EN pin below 100µA.

BST Resistor and Capacitor

A resistor in series with the BST capacitor (R_{BST}) can reduce the SW rising rate and voltage spikes. This enhances EMI performance and reduces voltage stress at a high V_{IN}. A higher resistance is better for SW spike reduction, but compromises efficiency. To make a tradeoff between EMI and efficiency, it is recommended to keep R_{BST} below 20Ω. It is also recommended for the BST capacitor to be between 0.1µF and 1µF.

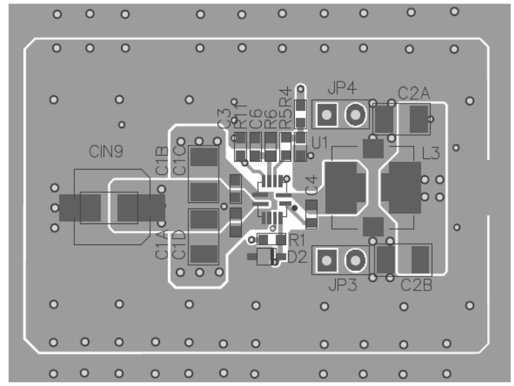
PCB Layout Guidelines [9]

An optimized PCB layout is critical for proper operation. A 4-layer layout is strongly recommended to improve thermal performance. For the best results, refer to Figure 7 and follow the guidelines below:

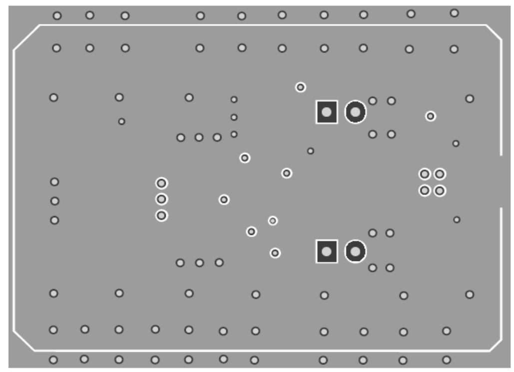
1. Place high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2. Use large copper areas to minimize conduction loss and thermal stress.
3. Place the ceramic input capacitors as close to the IN and GND pins as possible to minimize high frequency noise.
4. Place the T-type feedback resistors as close as possible to the FB pin to ensure the trace connecting to the FB pin is as short as possible.
5. Route SW and BST away from sensitive analog areas, such as FB.
6. Use multiple vias to connect the power planes to the internal layer.

Note:

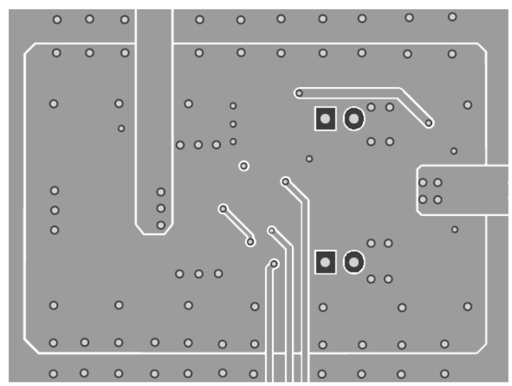
9) The recommended PCB layout is based on the circuit in Figure 8.



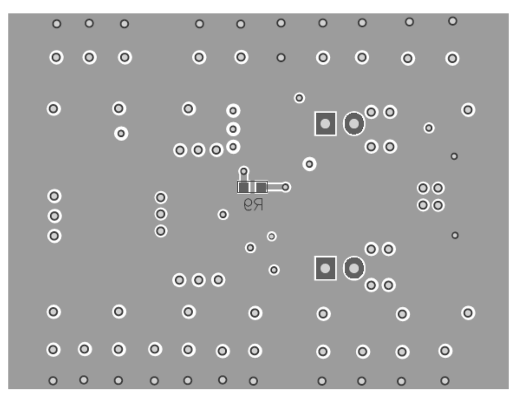
Top Layer and Top Silk



Inner Layer 1



Inner Layer 2



Bottom Layer and Bottom Silk

Figure 7: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

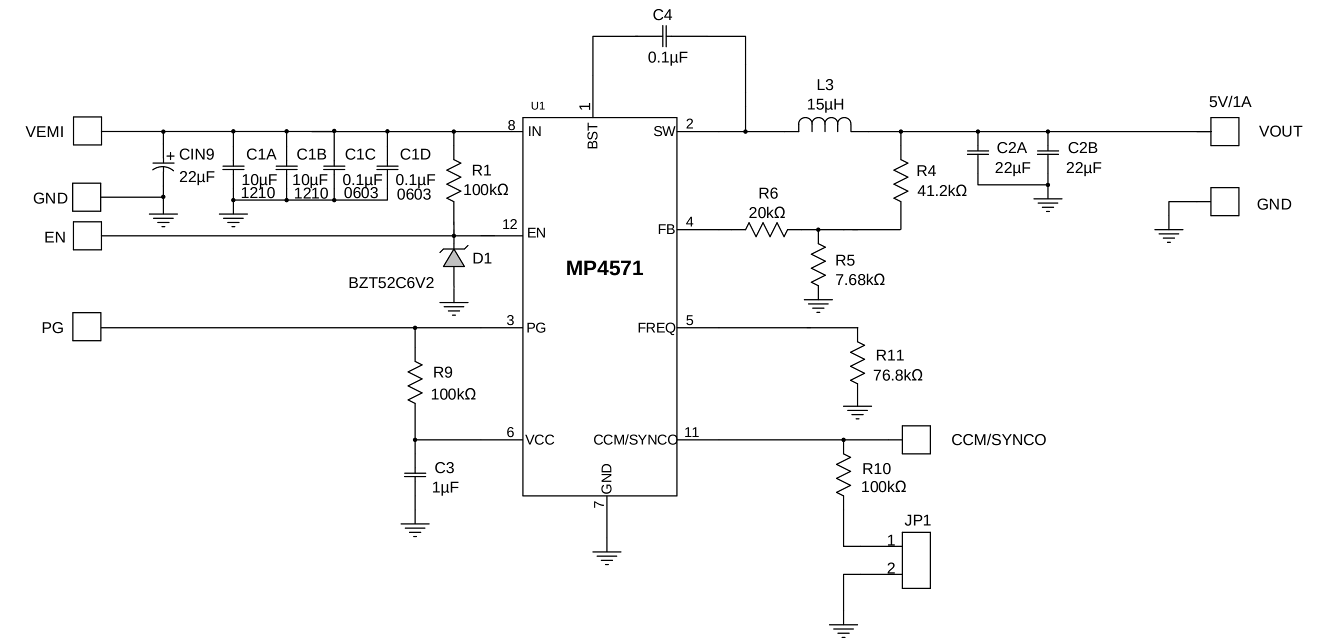


Figure 8: Typical Application Circuit

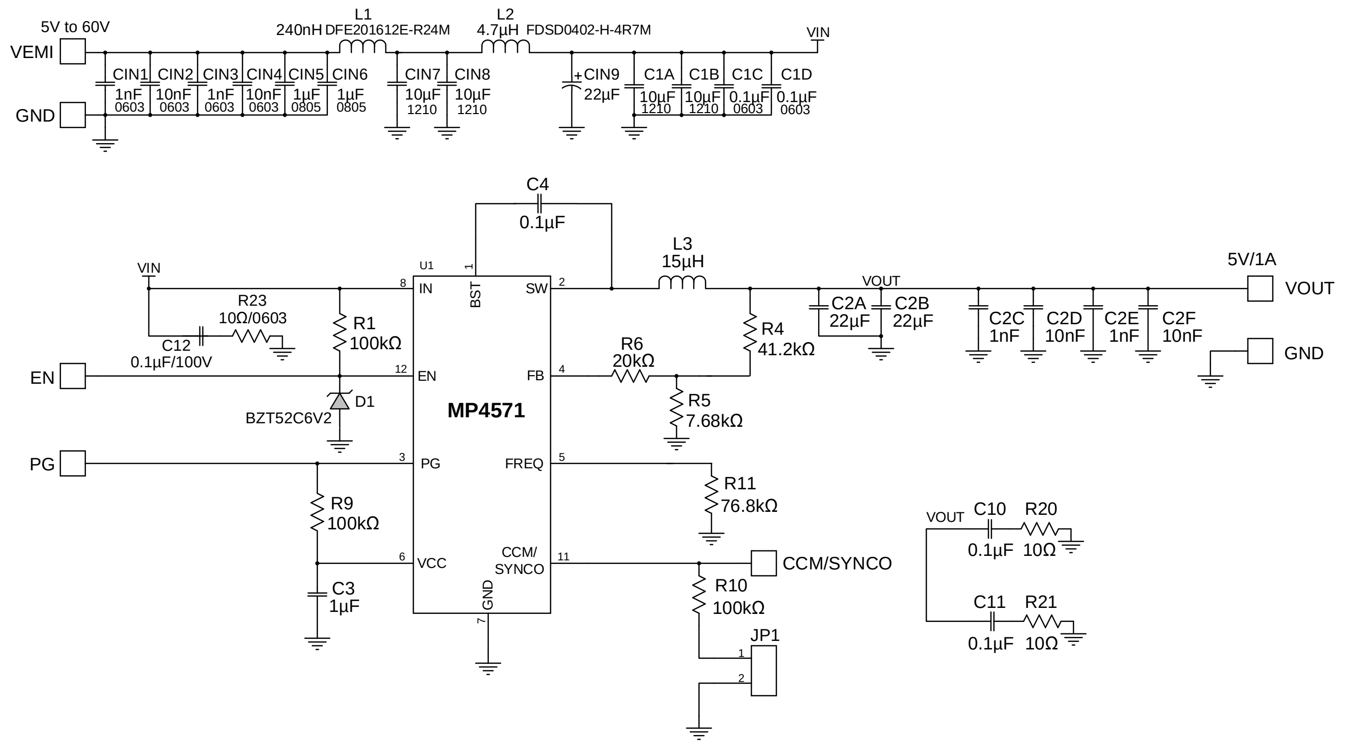
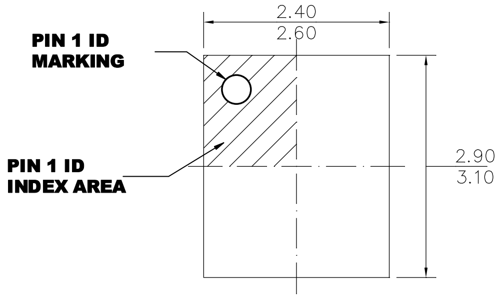


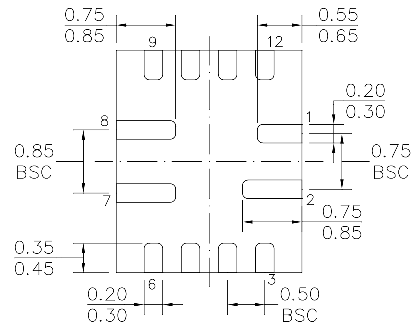
Figure 9: Typical Application Circuit with EMI Filters

PACKAGE INFORMATION

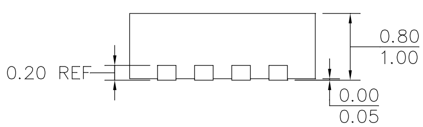
QFN-12 (2.5mmx3mm)
Non-Wettable Flank



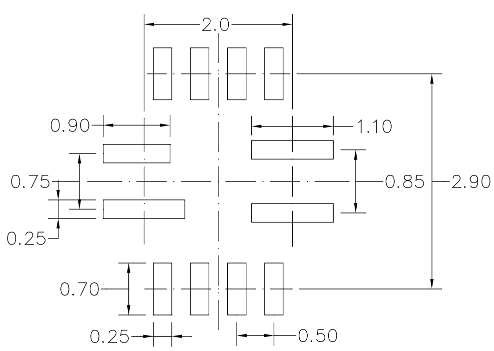
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

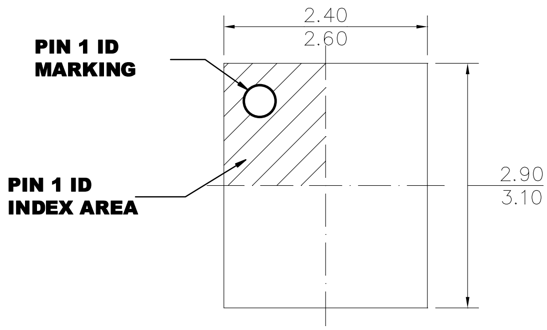
NOTE:

1) LAND PATTERNS OF PINS 2, 7, AND 8 HAVE THE SAME LENGTH AND WIDTH.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

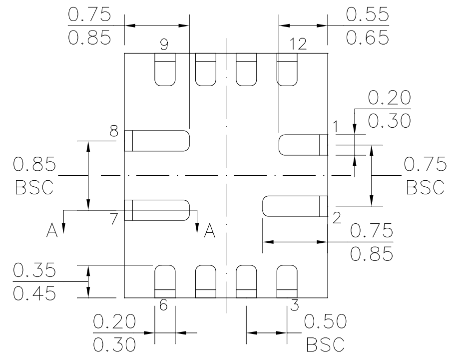
PACKAGE INFORMATION *(continued)*

QFN-12 (2.5mmx3mm)

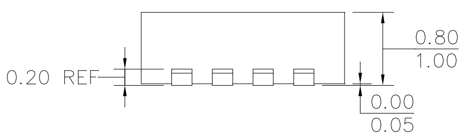
Wettable Flank



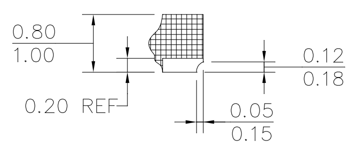
TOP VIEW



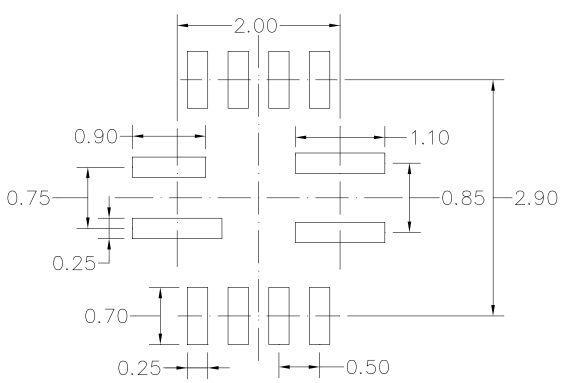
BOTTOM VIEW



SIDE VIEW



SECTION A-A

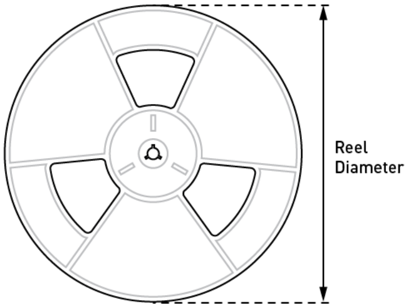


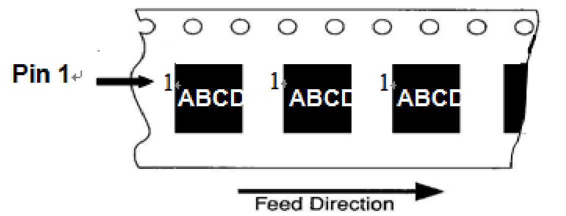
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) LAND PATTERNS OF PIN2,7 AND 8 HAVE THE SAME LENGTH AND WIDTH.
3) ALL DIMENSIONS ARE IN MILLIMETERS.
4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity/ Reel	Reel/ Diameter	Carrier Tape Width	Carrier Tape Pitch
MP4571GQB-Z	QFN-12 (2.5mmx3mm)	5000	13in	12mm	8mm
MP4571GQBE-Z	QFN-12 (2.5mmx3mm)	5000	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	3/9/2020	Initial Release	-
1.1	2/22/2023	Added “Available in a Wettable Flank Package” to the Features section	1
		Added the MP4571GQBE part number and top marking information	3
		Added the POD information for the MPQ4571GQBE	32
		Added the MP4571GQBE part number	33