

PRELIMINARY

July 1995

Subscriber Line Interface Circuit

Features

- DI Monolithic High Voltage Process
- Programmable Current Feed
- Programmable Loop Current Detector Threshold and Battery Feed Characteristics
- Ground Key and Ring trip Detection
- Compatible with Industry Standards Types
- Thermal Shutdown
- On-Hook Transmission
- Wide Battery Voltage Range (-24V to -56V)
- Low Standby Power
- Meets TR-NWT-000057 Transmission Requirements
- -40°C to +85°C Ambient Temperature Range

Applications

- Digital Loop Carrier Systems
- Fiber-In-The-Loop ONUs

Description

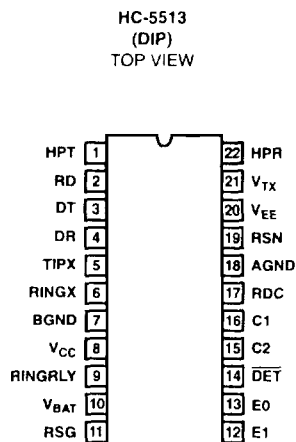
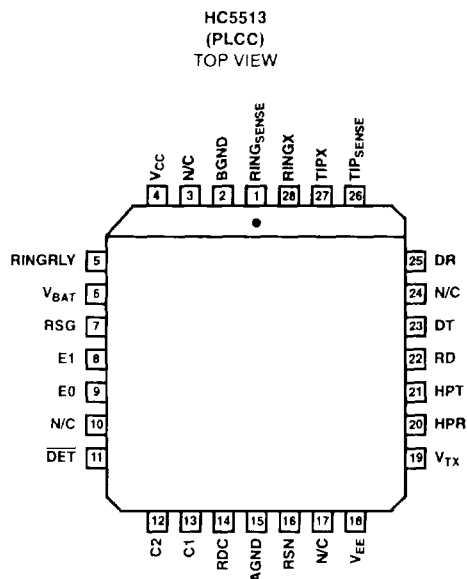
The HC-5513 is a subscriber line interface circuit design to match industry standard PBL3764 for PBX and DLC applications. Enhancements include: lower noise and absence of false signaling in the presence of longitudinal currents.

The HC-5513 is fabricated in a High Voltage Dielectrically Isolated (DI) Bipolar Process that eliminates leakage currents and device latch-up problems normally associated with junction isolated ICs. The elimination of the leakage currents results in improved circuit performance for wide temperature extremes. The latch free benefit of the DI process guarantees operation under adverse transient conditions. This process feature makes the HC-5513 ideally suited for use in harsh outdoor environments.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HC5513IMA02	-40°C to +85°C	28 Lead PLCC
HC5513IPA02	-40°C to +85°C	22 Lead Plastic DIP

Pinouts



Specifications HC-5513

Absolute Maximum Ratings

Temperature	
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +110°C
Operating Junction Temperature Range	-40°C to +150°C
Power Supply (-40°C ≤ T_A ≤ +85°C)	
Supply Voltage V _{CC} to GND	0.5V to 7V
Supply Voltage V _{EE} to GND	-7V to 0.5V
Supply Voltage V _{BAT} to GND	-70V to 0.5V
Ground	
Voltage between AGND and BGND	-0.3V to 0.3V
Relay Driver	
Ring Relay Supply Voltage	0V to V _{BAT} +75V
Ring Relay Current	50mA
Ring Trip Comparator	
Input Voltage	V _{BAT} to 0V
Input Current	-5mA to 5mA
Digital Inputs, Outputs (C1, C2, E0, E1, DET)	
Input Voltage	0V to V _{CC}
Output Voltage (DET not Active)	0V to V _{CC}
Output Current (DET)	5mA

Tipx and Ringx Terminals (-40°C ≤ T_A ≤ +85°C)

Tipx or Ringx Voltage, Continuous (Referenced to GND)	V _{BAT} to +2V
Tipx or Ringx, Pulse <10ms, I _{REP} >10s	V _{BAT} -20V to +5V
Tipx or Ringx, Pulse <10μs, I _{REP} >10s	V _{BAT} -40V to +10V
Tipx or Ringx, Pulse <250ns, I _{REP} >10s	V _{BAT} -70V to +15V
Tipx or Ringx Current	70mA
Gate Count	543 Transistors, 51 Diodes

Thermal Information (Typical)

Thermal Resistance	θ _{JA}
22 Lead Plastic DIP	75°C/W
28 Lead PLCC	65°C/W
Package Power Dissipation at +70°C	
22 Lead Plastic DIP	1.06W
28 Lead PLCC	1.23W
Derate Above +70°C	
Plastic DIP	13.3mW/°C
PLCC	15.4mW/°C
Lead Temperature (Soldering 10s)	+300°C
(PLCC - Lead Tips Only)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Typical Operating Conditions

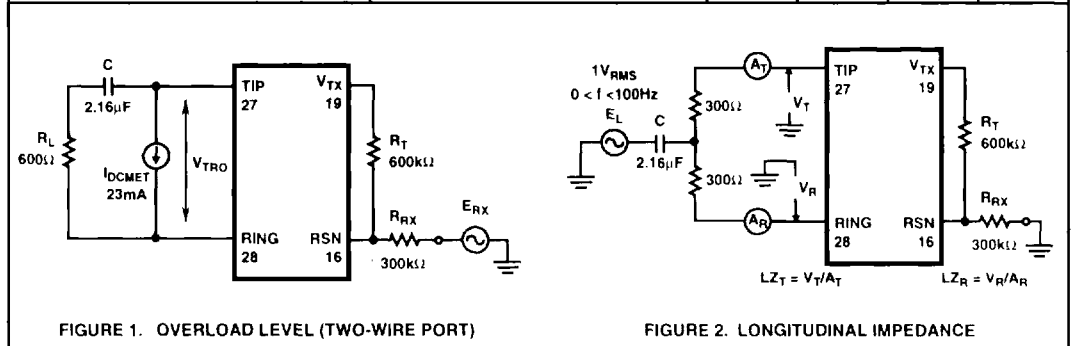
These represent the conditions under which the part was developed and are suggested as guidelines.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Case Temperature		-40	-	100	
V _{CC} with Respect to AGND	-40°C to +85°C	4.75	-	5.25	V
V _{EE} with Respect to AGND	-40°C to +85°C	-5.25	-	-4.75	V
V _{BAT} with Respect to BGND	-40°C to +85°C	-58	-	-24	V

Electrical Specifications

T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = +5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, C_{HP} = 10nF, C_{DC} = 1.5μF, Z_L = 600Ω. Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Overload Level	1% THD, Z _L = 600Ω, 2 16μF (Note 1, Figure 1)	3.1	-	-	V _{PEAK}
Longitudinal Impedance (Tip/Ring)	0 < f < 100Hz (Note 2, Figure 2)	-	20	35	Ω/Wire



TELECOMMUNICATIONS 12

T_A = -40°C to +85°C, V_{CC} = +5V ±5%, V_{EE} = +5V ±5%, V_{BAT} = -28V, AGND = BGND = 0V, R_{DC1} = R_{DC2} = 41.2kΩ, R_D = 39kΩ, R_{SG} = ∞, C_{HP} = 10nF, C_{DC} = 1.5μF, Z_{LC} = 600Ω, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. (Continued)

FIGURE 3A. OFF-HOOK

FIGURE 3B. ON-HOOK

FIGURE 3. LONGITUDINAL CURRENT LIMIT

OFF-HOOK LONGITUDINAL BALANCE					
Longitudinal to Metallic	IEEE 455 - 1985, $R_{LR}, R_{LT} = 368\Omega$ $0.2\text{kHz} < f < 4.0\text{kHz}$ (Note 5, Figure 4)	55	70	-	dB
Longitudinal to Metallic	$R_{LR}, R_{LT} = 300\Omega$, $0.2\text{kHz} < f < 4.0\text{kHz}$ (Note 5, Figure 4)	55	70	-	dB
Metallic to Longitudinal	FCC Part 68, Para 68.310 $0.2\text{kHz} < f < 1.0\text{kHz}$	50	55	-	dB
	$1.0\text{kHz} < f < 4.0\text{kHz}$ (Note 6)	50	55	-	dB
Longitudinal to 4-Wire	$0.2\text{kHz} < f < 4.0\text{kHz}$ (Note 7, Figure 4)	55	70	-	dB
Metallic to Longitudinal	$R_{LR}, R_{LT} = 300\Omega$, $0.2\text{kHz} < f < 4.0\text{kHz}$ (Note 8, Figure 5)	50	55	-	dB
4-Wire to Longitudinal	$0.2\text{kHz} < f < 4.0\text{kHz}$ (Note 9, Figure 5)	50	55	-	dB

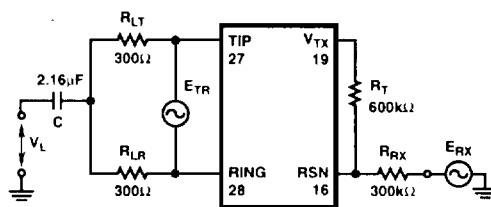


FIGURE 5. METALLIC TO LONGITUDINAL AND 4-WIRE TO LONGITUDINAL BALANCE

Specifications HC-5513

Electrical Specifications

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$, $V_{EE} = +5\text{V} \pm 5\%$, $V_{BAT} = -28\text{V}$, $AGND = BGND = 0\text{V}$, $R_{DC1} = R_{PC2} = 41.2\text{k}\Omega$, $R_D = 39\text{k}\Omega$, $R_{SG} = \infty$, $C_{HP} = 10\text{nF}$, $C_{DC} = 1.5\mu\text{F}$, $Z_L = 600\Omega$. Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
2-Wire Return Loss	0.2kHz to 0.5kHz (Note 10, Figure 8)	25	-	-	dB
	0.5kHz to 1.0kHz (Note 10, Figure 8)	27	-	-	dB
	1.0kHz to 3.4kHz (Note 10, Figure 8)	23	-	-	dB
TIP IDLE VOLTAGE					
Active, $I_I = 0$		-	-4		V
Standby, $I_L = 0$		-	<0		V
RING IDLE VOLTAGE					
Active, $I_L = 0$			-24	-	V
Standby, $I_L = 0$			-28	-	V
4-WIRE TRANSMIT PORT (V_{TX})					
Overload Level	($Z_L > 20\text{k}\Omega$, 1% THD) (Note 11, Figure 9)	3.1	-	-	V_{PEAK}
Output Offset Voltage	$E_G = 0$, $Z_L = \infty$, (Note 12, Figure 9)	-30	-	30	mV
Output Impedance (Guaranteed by Design)	0.2kHz $< f < 0.3$.4kHz	-	5	20	Ω
2- to 4-Wire (Metallic to V_{TX}) Voltage Gain	0.3kHz $< f < 0.3$.4kHz (Note 13, Figure 9)	0.98	1.0	1.02	V/V

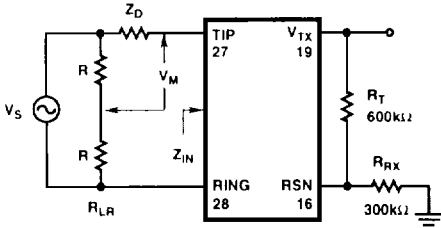


FIGURE 8. TWO-WIRE RETURN LOSS

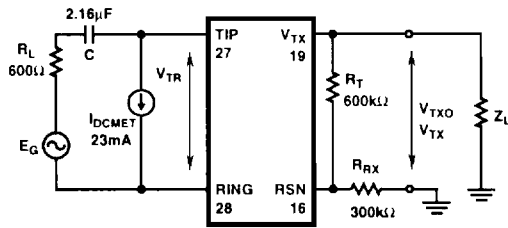


FIGURE 9. OVERLOAD LEVEL (4-WIRE TRANSMIT PORT),
OUTPUT OFFSET VOLTAGE, 2-WIRE TO
4-WIRE VOLTAGE GAIN AND HARMONIC
DISTORTION

4-WIRE RECEIVE PORT (RSN)					
DC Voltage	$I_{RSN} = 0\text{mA}$	-	0	-	V
R_X Sum Node Impedance	0.3kHz $< f < 3.4$ kHz	-	-	20	Ω
Current Gain-RSN to Metallic	0.3kHz $< f < 3.4$ kHz (Note 14, Figure 10)	980	1000	1020	Ratio
FREQUENCY RESPONSE (OFF HOOK)					
2-Wire to 4-Wire	0dBm at 1.0kHz, $E_{RX} = 0\text{V}$ 0.3kHz $< f < 3.4$ kHz (Note 15, Figure 11)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm at 1.0kHz, $E_G = 0\text{V}$ 0.3kHz $< f < 3.4$ kHz (Note 16, Figure 11)	-0.2	-	0.2	dB
4-Wire to 4-Wire	0dBm at 1.0kHz, $E_G = 0\text{V}$ 0.3kHz $< f < 3.4$ kHz (Note 17, Figure 11)	-0.2	-	0.2	dB
INSERTION LOSS					
2-Wire to 4-Wire	0dBm, 1kHz (Note 18, Figure 11)	-0.2	-	0.2	dB
4-Wire to 2-Wire	0dBm, 1kHz (Note 19, Figure 11)	-0.2	-	0.2	dB

Specifications HC-5513

Electrical Specifications $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$, $V_{EE} = +5\text{V} \pm 5\%$, $V_{BAT} = -28\text{V}$, $\text{AGND} = \text{BGND} = 0\text{V}$, $R_{DC1} = R_{DC2} = 41.2\text{k}\Omega$, $R_D = 39\text{k}\Omega$, $R_{SG} = \infty$, $C_{HP} = 10\text{nF}$, $C_{DC} = 1.5\mu\text{F}$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GAIN TRACKING (Ref = -10dBm, at 1.0kHz)					
2-Wire to 4-Wire	-40dBm to +3dBm (Note 20, Figure 11)	-0.1	-	0.1	dB
2-Wire to 4-Wire	-55dBm to -40dBm (Note 20, Figure 11)	-	± 0.03	-	dB
4-Wire to 2-Wire	-40dBm to +3dBm (Note 21, Figure 11)	-0.1	-	0.1	dB
4-Wire to 2-Wire	-55dBm to -40dBm (Note 21, Figure 11)	-	± 0.03	-	dB

$$K = I_M \left(\frac{R_{DC1} + R_{DC2}}{V_{RDC} - V_{RSN}} \right)$$

Where $K \approx 1000$

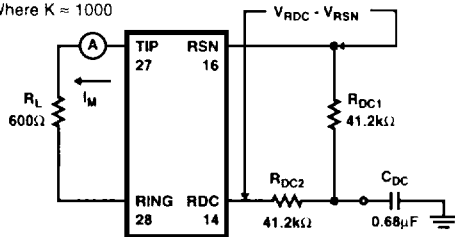


FIGURE 10. CURRENT GAIN -RSN TO METALLIC

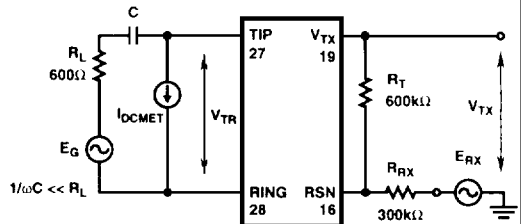


FIGURE 11. FREQUENCY RESPONSE, INSERTION LOSS, GAIN TRACKING AND HARMONIC DISTORTION

NOISE

Idle Channel Noise at 2-Wire	C-Message Weighting (Note 22, Figure 12)	-	7.5	8.9	dBrnC
Idle Channel Noise at 4-Wire	C-Message Weighting (Note 23, Figure 12)	-	-	8.9	dBrnC

HARMONIC DISTORTION

2-Wire to 4-Wire	0dBm, 1kHz (Note 24, Figure 9)	-	-65	-54	dB
4-Wire to 2-Wire	0dBm, 0.3kHz to 3.4kHz (Note 25, Figure 11)	-	-65	-54	dB

BATTERY FEED CHARACTERISTICS

Constant Loop Current Tolerance $R_{DCX} = 41.2\text{k}\Omega$	$I_L = 2500/(R_{DC1} + R_{DC2})$, -40°C to +85°C (Note 26)	$0.9I_L$	I_L	$1.1I_L$	mA
Loop Current Tolerance (Standby)	$I_L = (V_{BAT} - 3)/(R_L + 1800)$, -40°C to +85°C (Note 27)	$0.8I_L$	I_L	$1.2I_L$	mA
Open Circuit Voltage ($V_{TIP} - V_{RING}$)	-40°C to +85°C, (Active)	15	-	19	V

LOOP CURRENT DETECTOR

On Hook to Off Hook	$R_D = 39\text{k}\Omega$ -40°C to +85°C	$372/R_D$	$465/R_D$	$558/R_D$	mA
Off Hook to On Hook	$R_D = 39\text{k}\Omega$ -40°C to +85°C	$325/R_D$	$405/R_D$	$485/R_D$	mA
Loop Current Hysteresis	$R_D = 39\text{k}\Omega$ -40°C to +85°C	$25/R_D$	$60/R_D$	$95/R_D$	mA

Specifications HC-5513

Electrical Specifications

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$, $V_{EE} = +5\text{V} \pm 5\%$, $V_{BAT} = -28\text{V}$, $\text{AGND} = \text{BGND} = 0\text{V}$, $R_{DC1} = R_{DC2} = 41.2\text{k}\Omega$, $R_D = 39\text{k}\Omega$, $R_{SG} = \infty$, $C_{HP} = 10\text{nF}$, $C_{DC} = 1.5\mu\text{F}$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GROUND KEY DETECTOR					
Tip/Ring Current Difference - Trigger	(Note 28, Figure 13)	8	12	17	mA
Tip/Ring Current Difference - Reset	(Note 28, Figure 13)	3	7	12	mA
Hysteresis	(Note 28, Figure 13)	0	5	9	mA

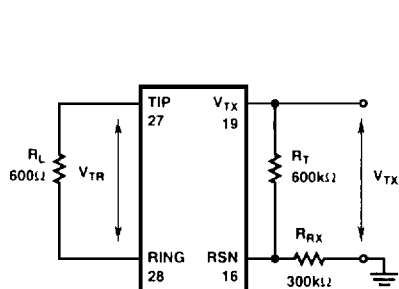


FIGURE 12. IDLE CHANNEL NOISE

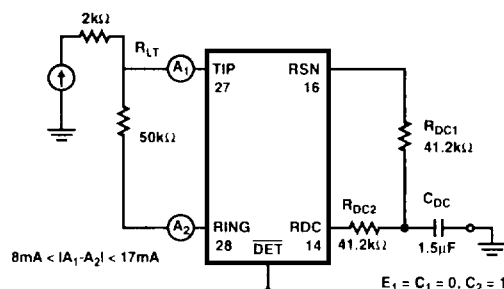


FIGURE 13. GROUND KEY DETECT

RING TRIP DETECTOR (DT, DR)					
Offset Voltage	Source Res = 0	-20	-	20	mV
Input Bias Current	Source Res = 0	-500	-	500	nA
Input Common-Mode Range	Source Res = 0	$V_{BAT} + 1$	-	0	V
Input Resistance	Source Res = 0 Balanced	3	-	-	MΩ
RING RELAY DRIVER					
V_{SAT} at 25mA	$I_{OL} = 25\text{mA}$	-	1.0	1.5	V
Off-State Leakage Current	$V_{OH} = 12\text{V}$	-	-	10	μA
DIGITAL INPUTS (E0, E1, C1, C2)					
Input Low Voltage, V_{IL}		0	-	0.8	V
Input High Voltage, V_{IH}		2	-	V_{CC}	V
Input Low Current, I_{IL} : C1, C2	$V_{IL} = 0.4\text{V}$	-200	-	-	μA
Input Low Current, I_{IL} : E0, E1	$V_{IL} = 0.4\text{V}$	-100	-	-	μA
Input High Current	$V_{IH} = 2.4\text{V}$	-	-	40	μA
DETECTOR OUTPUT (DET)					
Output Low Voltage, V_{OL}	$I_{OL} = 2\text{mA}$	-	-	0.45	V
Output High Voltage, V_{OH}	$I_{OH} = 100\mu\text{A}$	2.7	-	-	V
Internal Pull-up Resistor		10	15	20	kΩ
Power Dissipation					
Open Circuit State	$C1 = C2 = 0$	-	-	23	mW
On Hook, Standby	$C1 = C2 = 1$	-	-	30	mW

Specifications HC-5513

Electrical Specifications

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +5\text{V} \pm 5\%$, $V_{EE} = +5\text{V} \pm 5\%$, $V_{BAT} = -28\text{V}$, $AGND = BGND = 0\text{V}$, $R_{DC1} = R_{DC2} = 41.2\text{k}\Omega$, $R_D = 39\text{k}\Omega$, $R_{SG} = \infty$, $C_{HP} = 10\text{nF}$, $C_{DC} = 1.5\mu\text{F}$, $Z_L = 600\Omega$, Unless Otherwise Specified. All pin number references in the figures refer to the 28 lead PLCC package. (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
On Hook, Active	$C1 = 0$, $C2 = 1$, $R_L = \text{High Impedance}$	-	-	150	mW
Off Hook, Active	$R_L = 0\Omega$	-	-	1.0	W
	$R_L = 300\Omega$	-	-	0.72	W
	$R_L = 600\Omega$	-	-	0.45	W
TEMPERATURE GUARD					
Thermal Shutdown		150	-	180	$^{\circ}\text{C}$
SUPPLY CURRENTS ($V_{BAT} = -28\text{V}$)					
I_{CC} , On Hook	Open Circuit State ($C1, 2 = 0, 0$)	-	-	1.5	mA
	Standby State ($C1, 2 = 1, 1$)	-	-	1.7	mA
	Active State ($C1, 2 = 0, 1$)	-	-	5.5	mA
I_{EE} , On Hook	Open Circuit State ($C1, 2 = 0, 0$)	-	-	0.8	mA
	Standby State ($C1, 2 = 1, 1$)	-	-	0.8	mA
	Active State ($C1, 2 = 0, 1$)	-	-	2.2	mA
I_{BAT} , On Hook	Open Circuit State ($C1, 2 = 0, 0$)	-	-	0.4	mA
	Standby State ($C1, 2 = 1, 1$)	-	-	0.6	mA
	Active State ($C1, 2 = 0, 1$)	-	-	3.9	mA
PSRR					
V_{CC} to 2 or 4-Wire port	(Note 29, Figure 14)	-	50	-	dB
V_{EE} to 2 or 4-Wire port	(Note 29, Figure 14)	-	50	-	dB
V_{BAT} to 2 or 4-Wire port	(Note 29, Figure 14)	-	50	-	dB

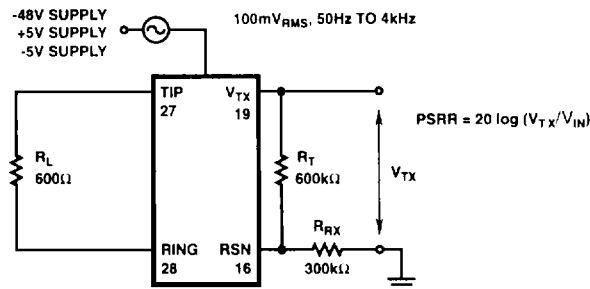


FIGURE 14. POWER SUPPLY REJECTION RATIO

NOTES:

1. **Overload Level (Two-Wire port)** - The overload level is specified at the 2-wire port (V_{TR0}) with the signal source at the 4-wire receive port (E_{RX}). $I_{DCMET} = 23\text{mA}$, increase the amplitude of E_{RX} until 1% THD is measured at V_{TR0} . Reference Figure 1.
2. **Longitudinal Impedance** - The longitudinal impedance is computed using the following equations, where TIP and RING voltages are referenced to ground. L_{ZT} , L_{ZR} , V_T , V_R , A_R and A_T are defined in Figure 2.
 $(TIP) L_{ZT} = V_T/A_T$
 $(RING) L_{ZR} = V_R/A_R$
 where: $E_L = 1V_{RMS}$ (0Hz to 100Hz)
3. **Longitudinal Current Limit (Off Hook Active)** - Off Hook (Active, $C1 = 1$, $C2 = 0$) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3a) until the 2-wire longitudinal balance drops below 45dB. DET pin remains high (no false detection).
4. **Longitudinal Current Limit (On Hook Standby)** - On Hook (Active, $C1 = 1$, $C2 = 1$) longitudinal current limit is determined by increasing the amplitude of E_L (Figure 3b) until the 2-wire longitudinal balance drops below 45dB. DET pin remains high (no false detection).
5. **Longitudinal to Metallic Balance** - The longitudinal to metallic balance is computed using the following equation.
 $BLME = 20 \cdot \log (E_L/V_{TR})$, where: E_L and V_{TR} are defined in Figure 4.
6. **Metallic to Longitudinal FCC Part 68, Para 68.310** - The metallic to longitudinal balance is defined in the above mentioned spec.
7. **Longitudinal to Four-Wire Balance** - The longitudinal to 4-wire balance is computed using the following equation.
 $BLFE = 20 \cdot \log (E_L/V_{TX})$, E_L and V_{TX} are defined in Figure 4.
8. **Metallic to Longitudinal Balance** - The metallic to longitudinal balance is computed using the following equation.
 $BMLE = 20 \cdot \log (E_{TR}/V_L)$, $E_{RX} = 0$
 where: E_{TR} , V_L and E_{RX} are defined in Figure 5.
9. **Four-Wire to Longitudinal Balance** - The 4-wire to longitudinal balance is computed using the following equation.
 $BFLE = 20 \cdot \log (E_{RX}/V_L)$, $E_{TR} = \text{source is removed}$.
 where: E_{RX} , V_L and E_{TR} are defined in Figure 5.
10. **Two-Wire Return Loss** - The 2-wire return loss is computed using the following equation.
 $r = -20 \cdot \log (2V_M/V_S)$
 where: Z_D = The desired impedance, e.g., the characteristic impedance of the line, nominally 600 Ω . (Reference Figure 8).
11. **Overload Level (4-Wire port)** - The overload level is specified at the 4-wire transmit port (V_{TX0}) with the signal source (E_G) at the 2-wire port, $I_{DCMET} = 23\text{mA}$, $Z_L = 20k\Omega$ (Reference Figure 9). Increase the amplitude of E_G until 1% THD is measured at V_{TX0} . Note that the gain from the 2-wire port to the 4-wire port is equal to 1.
12. **Output Offset Voltage** - The output offset voltage is specified with the following conditions: $E_G = 0$, $I_{DCMET} = 23\text{mA}$, $Z_L = \infty$ and is measured at V_{TX} . E_G , I_{DCMET} , V_{TX} and Z_L are defined in Figure 9.
13. **Two-Wire to Four-Wire (Metallic to V_{TX}) Voltage Gain** - The 2-wire to 4-wire (metallic to V_{TX}) voltage gain is computed using the following equation.
 $G_{2,4} = V_{TX}/V_{TR}$, $E_G = 0\text{dBm0}$, V_{TX} , V_{TR} , and E_G are defined in Figure 9.
14. **Current Gain RSN to Metallic** - The current gain RSN to Metallic is computed using the following equation.
 $K = I_M [(R_{DC1} + R_{DC2})/(V_{RDC} - V_{RSN})]$ K , I_M , R_{DC1} , R_{DC2} , V_{RDC} and V_{RSN} are defined in Figure 10.
15. **Two-Wire to Four-Wire Frequency Response** - The 2-wire to 4-wire frequency response is measured with respect to $E_G = 0\text{dBm}$ at 1.0kHz, $E_{RX} = 0\text{V}$, $I_{DCMET} = 23\text{mA}$. The frequency response is computed using the following equation.
 $F_{2,4} = 20 \cdot \log (V_{TX}/V_{TR})$, vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.
 V_{TX} , V_{TR} , and E_G are defined in Figure 11.
16. **Four-Wire to Two-Wire Frequency Response** - The 4-wire to 2-wire frequency response is measured with respect to $E_{RX} = 0\text{dBm}$ at 1.0kHz, $E_G = 0\text{V}$, $I_{DCMET} = 23\text{mA}$. The frequency response is computed using the following equation.
 $F_{4,2} = 20 \cdot \log (V_{TR}/E_{RX})$, vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.
 V_{TR} and E_{RX} are defined in Figure 11.
17. **Four-Wire to Four-Wire Frequency Response** - The 4-wire to 4-wire frequency response is measured with respect to $E_{RX} = 0\text{dBm}$ at 1.0kHz, $E_G = 0\text{V}$, $I_{DCMET} = 23\text{mA}$. The frequency response is computed using the following equation.
 $F_{4,4} = 20 \cdot \log (V_{TX}/E_{RX})$, vary frequency from 300Hz to 3.4kHz and compare to 1kHz reading.
 V_{TX} and E_{RX} are defined in Figure 11.

- 18. Two-Wire to Four-Wire Insertion Loss** - The 2-wire to 4-wire Insertion loss is measured with respect to $E_G = 0\text{dBm}$ at 1.0kHz input signal, $E_{RX} = 0$, $I_{DCMET} = 23\text{mA}$ and is computed using the following equation.

$$L_{2,4} = 20 \cdot \log (V_{TX}/V_{TR})$$
 where: V_{TX} , V_{TR} , and E_G are defined in Figure 11. (Note: The fuse resistors, R_F , impact the insertion loss. The specified insertion loss is for $R_F = 0$).
- 19. Four-Wire to Two-Wire Insertion Loss** - The 4-wire to 2-wire Insertion loss is measured based upon $E_{RX} = 0\text{dBm}$, 1.0kHz input signal, $E_G = 0$, $I_{DCMET} = 23\text{mA}$ and is computed using the following equation.

$$L_{4,2} = 20 \cdot \log (V_{TR}/E_{RX})$$
 where: V_{TR} and E_{RX} are defined in Figure 11.
- 20. Two-Wire to Four-Wire Gain Tracking** - The 2-wire to 4-wire gain tracking is referenced to measurements taken for $E_G = -10\text{dBm}$, 1.0kHz signal, $E_{RX} = 0$, $I_{DCMET} = 23\text{mA}$ and is computed using the following equation.

$$G_{2,4} = 20 \cdot \log (V_{TX}/V_{TR})$$
 vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.
 V_{TX} and V_{TR} are defined in Figure 11.
- 21. Four-Wire to Two-Wire Gain Tracking** - The 4-wire to 2-wire gain tracking is referenced to measurements taken for $E_{RX} = -10\text{dBm}$, 1.0kHz signal, $E_G = 0$, $I_{DCMET} = 23\text{mA}$ and is computed using the following equation.

$$G_{4,2} = 20 \cdot \log (V_{TR}/E_{RX})$$
 vary amplitude -40dBm to +3dBm, or -55dBm to -40dBm and compare to -10dBm reading.
 V_{TR} and E_{RX} are defined in Figure 11. The level is specified at the 4-wire receive port and referenced to a 600Ω impedance level.
- 22. Two-Wire Idle Channel Noise** - The 2-wire idle channel noise at V_{TR} is specified with the 2-wire port terminated in 600Ω (R_L) and with the 4-wire receive port grounded (Reference Figure 12).
- 23. Four-Wire Idle Channel Noise** - The 4-wire idle channel noise at V_{TX} is specified with the 2-wire port terminated in 600Ω (R_L). The noise specification is with respect to a 600Ω impedance level at V_{TX} . The 4-wire receive port is grounded (Reference Figure 12).
- 24. Harmonic Distortion (2-Wire to 4-Wire)** - The harmonic distortion is measured with the following conditions. $E_G = 0\text{dBm}$ at 1kHz, $I_{DCMET} = 23\text{mA}$. Measurement taken at V_{TX} . (Reference Figure 9).
- 25. Harmonic Distortion (4-Wire to 2-Wire)** - The harmonic distortion is measured with the following conditions. $E_{RX} = 0\text{dBm}$. Vary frequency between 300Hz and 3.4kHz, $I_{DCMET} = 23\text{mA}$. Measurement taken at V_{TR} . (Reference Figure 11).
- 26. Constant Loop Current** - The constant loop current is calculated using the following equation.

$$I_L = 2500 / (R_{DC1} + R_{DC2})$$
- 27. Standby State Loop Current** - The Standby state loop current is calculated using the following equation.

$$I_L = (|V_{BAT}| - 3) / (R_L + 1800)$$
 $T_{amb} = 25^\circ\text{C}$
- 28. Ground Key Detector** - (TRIGGER) Increase the input current to verify that if $A_1 - A_2 > 8\text{mA}$ then $\overline{\text{DET}}$ goes Low. A_1 and A_2 are defined in Figure 13.
 (RESET) Decrease the input current to verify that if $A_1 - A_2 < 3\text{mA}$ then $\overline{\text{DET}}$ goes high. A_1 and A_2 are defined in Figure 13
 (Hysteresis) Compare difference between trigger and reset.
- 29. Power Supply Rejection Ratio** - Inject a 100mV_{RMS} signal (50Hz to 4kHz) on V_{BAT} , V_{CC} and V_{EE} supplies. PSRR is computed using the following equation.

$$\text{PSRR} = 20 \cdot \log (V_{TX}/V_{IN})$$
 V_{TX} and V_{IN} are defined in Figure 14.

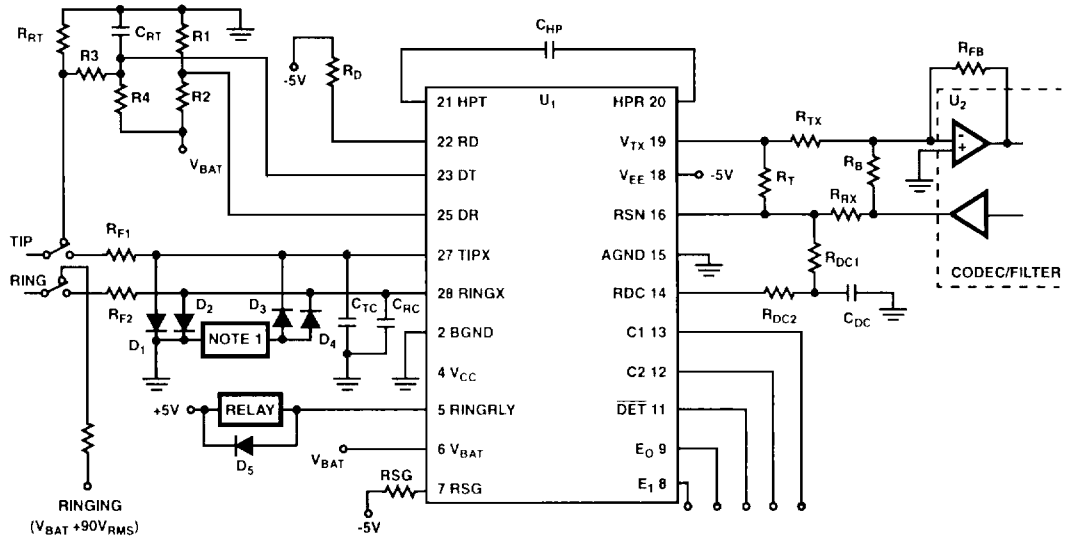
Pin Descriptions

PLCC	PDIP	SYMBOL	DESCRIPTION
1		RINGSENSE	Internally connected to output of RING power amplifier.
2	7	$\overline{\text{BGND}}$	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND
4	8	V_{CC}	+5V power supply.
5	9	RINGRLY	Ring relay driver output.
6	10	V_{BAT}	Battery supply voltage. -48V to -56V
7	11	RSG	Saturation guard programming resistor pin.

Pin Descriptions (Continued)

PLCC	PDIP	SYMBOL	DESCRIPTION
8	12	E1	TTL compatible logic input. The logic state of E1 in conjunction with the logic state of C1 determines which detector is gated to the $\overline{\text{DET}}$ (pin 11) output.
9	13	E0	TTL compatible logic input. Enables the $\overline{\text{DET}}$ (pin 11) output when set to logic level zero and disables $\overline{\text{DET}}$ output when set to a logic level one.
11	14	DET	Detector output. TTL compatible logic output. A zero logic level indicates that the selected detector was triggered (see truth table for selection of Ground Key detector, Loop Current detector or the Ring Trip detector). The $\overline{\text{DET}}$ output is an open collector with an internal pull-up of approximately 15k Ω to V_{CC} .
12	15	C2	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
13	16	C1	TTL compatible logic input. The logic states of C1 and C2 determine the operating states (Open Circuit, Active, Ringing or Standby) of the SLIC.
14	17	RDC	DC feed current programming resistor pin. Constant current feed is programmed by resistors R_{DC1} and R_{DC2} connected in series from this pin to the receive summing node (RSN, pin16). The resistor junction point is decoupled to AGND to isolate the AC signal components.
15	18	AGND	Analog ground.
16	19	RSN	Receive Summing Node. The AC and DC current flowing into this pin establishes the metallic loop current that flows between TIP (pin 27) and RING (pin 28). The magnitude of the metallic loop current is 1000 times greater than the current into the RSN pin. The constant current programming resistors and the networks for program receive gain and 2-wire impedance all connect to this pin.
18	20	V_{EE}	-5V power supply.
19	21	V_{TX}	Transmit audio output. This output is equivalent to the TIP to RING metallic Voltage. The network for programming the 2-wire input impedance connects between this pin and RSN (pin 16).
20	22	HPR	RING side of AC/DC separation capacitor C_{HP} . C_{HP} is required to properly separate the RING AC current from the DC loop current. The other end of C_{HP} is connected to pin 21 HPT.
21	1	HPT	TIP side of AC/DC separation capacitor C_{HP} . C_{HP} is required to properly separate the TIP AC current from the DC loop current. The other end of C_{HP} is connected to pin 20 HPR.
22	2	RD	Loop current programming resistor. Resistor R_D sets the trigger level for the loop current detect circuit. A filter capacitor C_{TJ} is also connected between this pin and V_{EE} (pin 18).
23	3	DT	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT (pin 23) and DR (pin 25).
25	4	DR	Input to ring trip comparator. Ring trip detection is accomplished by connecting an external network to a comparator in the SLIC with inputs DT (pin 23) and DR (pin 25).
26		TIP_{SENSE}	Internally connected to output of TIP power amplifier.
27	5	TIPX	Output of TIP power amplifier.
28	6	RINGX	Output of RING power amplifier.
3, 10, 17, 24		$\overline{N/C}$	No internal connection.

Applications Diagram



- | | | | |
|-----------------------------------|---|-------------------------------------|------------------------------|
| U1 | SLIC (SUBSCRIBER LINE INTERFACE CIRCUIT)
HC-5513 | R _{F1} , R _{F2} | LINE RESISTOR, 20Ω, 1% MATCH |
| U2 | COMBINATION CODEC/FILTER E.G.
CD22354A OR PROGRAMMABLE CODEC/
FILTER, E.G. SLAC | R ₁ , R ₃ | 200kΩ, 5%, 1/4W |
| C _{DC} | 1.5μF, 20%, 10V | R ₂ | 910kΩ, 5%, 1/4W |
| C _{HP} | 10nF, 20%, 100V | R ₄ | 1.2MΩ, 5%, 1/4W |
| C _{RT} | 0.39μF, 20%, 100V | R _B | 75.5kΩ, 1%, 1/4W |
| C _{TC} , C _{RC} | 2200pF, 20%, 10V | R _D | 39kΩ, 5%, 1/4W |
| RELAY | RELAY, 2C CONTACTS, 12V COIL | R _{DC1} , R _{DC2} | 41.2kΩ, 5%, 1/4W |
| D ₁ - D ₄ | DIODE, 100V, 3A | R _{FB} | 20.0kΩ, 1%, 1/4W |
| D ₅ | DIODE 1N4454 | R _{RX} | 300kΩ, 1%, 1/4W |
| | | R _T | 600kΩ, 1%, 1/4W |
| | | R _{TX} | 20kΩ, 1%, 1/4W |
| | | R _{RT} | 150Ω, 5%, 2W |
| | | R _{SG} | Open Circuit |

NOTE:

- The anodes of D₃ and D₄ may be connected directly to the V_{BAT} supply if the application is exposed to only low energy transients. For harsher environments it is recommended that the anodes of D₃ and D₄ be shorted to ground through a transient voltage suppressor or surge protector.

SLIC Operating States

STATE	E0	E1	C1	C2	SLIC OPERATING STATE	ACTIVE DETECTOR	DET OUTPUT
1	0	0	0	0	Open Circuit	No Active Detector	Logic Level High
2	0	0	0	1	Active	Ground Key Detector	Ground Key Status
3	0	0	1	0	Ringing	No Active Detector	Logic Level High
4	0	0	1	1	Standby	Ground Key Detector	Ground Key Status
5	0	1	0	0	Open Circuit	No Active Detector	Logic Level High
6	0	1	0	1	Active	Loop Current Detector	Loop Current Status
7	0	1	1	0	Ringing	Ring Trip Detector	Ring Trip Status
8	0	1	1	1	Standby	Loop Current Detector	Loop Current Status
9	1	0	0	0	Open Circuit	No Active Detector	Logic Level High
10	1	0	0	1	Active	Ground Key Detector	
11	1	0	1	0	Ringing	No Active Detector	
12	1	0	1	1	Standby	Ground Key Detector	
13	1	1	0	0	Open Circuit	No Active Detector	
14	1	1	0	1	Active	Loop Current Detector	
15	1	1	1	0	Ringing	Ring Trip Detector	
16	1	1	1	1	Standby	Loop Current Detector	