# MP3924

## Quad-Port, IEEE 802.3af/at PSE Controller for Power over Ethernet

## DESCRIPTION

The MP3924 is a quad-port power source equipment (PSE) power controller for IEEE 802.3af/at compliant power over Ethernet (PoE) applications.

The device has all the functions of IEEE 802.3af/at, including detection, single-event and two-event classification, current limiting, and disconnected load detection. All of the functions can be configured to work in automatic operation mode or software program mode via the I²C.

The MP3924 features a 9-bit analog-to-digital converter (ADC) to monitor the current and voltage, a special I²C interface for isolated controller communication, adjustable current limits, and configurable system functions. These features provide flexibility for PoE applications.

The MP3924 is available in a QFN-32 (5mmx5mm) package.

## FEATURES

- IEEE802.3af/at Compliant
- Quad-Port and 4-Bit Configurable I²C Address
- 0.25Ω Current-Sense Resistor
- Automatic Mode and I²C Command Control Mode
- Automatic Input Over-Power Shutdown
- Internal VCC Power Supply
- Three-Wire I²C Interface for Isolated Applications
- Two INT Pins for Interrupt Priority Selection
- Disconnected DC Load Detection
- Instantaneous Current/Voltage Readout
- Thermal Protection
- Available in a QFN-32 (5mmx5mm) Package

## APPLICATIONS

- PSE Switches/Routers
- PSE Midspan Power Injectors
- Surveillance NVR and DVRs

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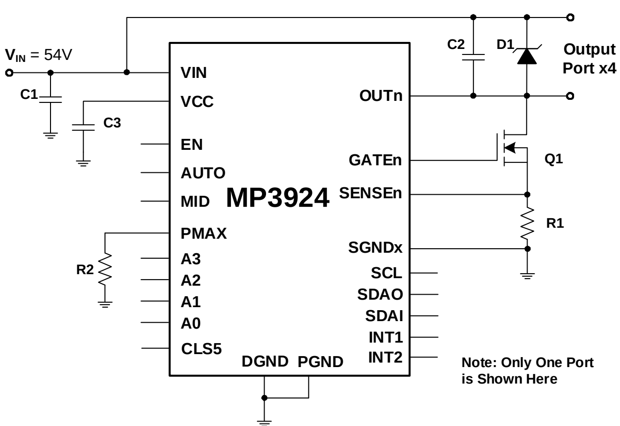
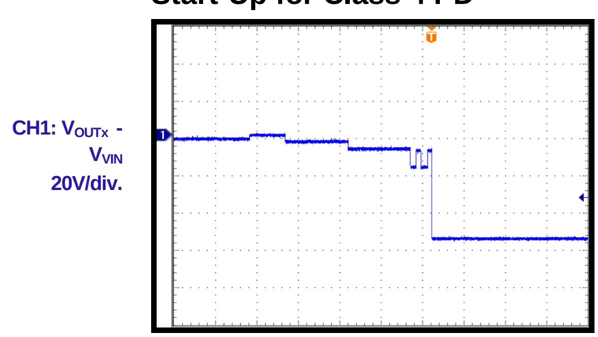
## TYPICAL APPLICATION




**Start-Up for Class 4 PD**





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## ORDERING INFORMATION

| Part Number | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MP3924GU* | QFN-32 (5mmx5mm) | *See Below* | 2 |
| EVKT-MP3924 | Evaluation kit | - | |

* For Tape & Reel, add suffix -Z (e.g. MP3924GU-Z).

## TOP MARKING

MPSYYWW
MP3924
LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP3924: Part number
LLLLLLL: Lot number

## EVALUATION KIT EVKT-MP3924

EVKT-MP3924 kit contents (items listed below can be ordered separately, and the GUI installation file and supplemental documents can be downloaded from the MPS website):

| # | Part Number | Item | Quantity |
|---|---|---|---|
| 1 | EV3924-U-00A | MP3924 evaluation board | 1 |
| 2 | EVKT-USBI2C-02 | Includes one USB to I²C communication interface device, one USB cable, and one ribbon cable | 1 |
| 3 | MP3924GU | MP3924 controller IC | 2 |

**Order directly from MonolithicPower.com or our distributors.**

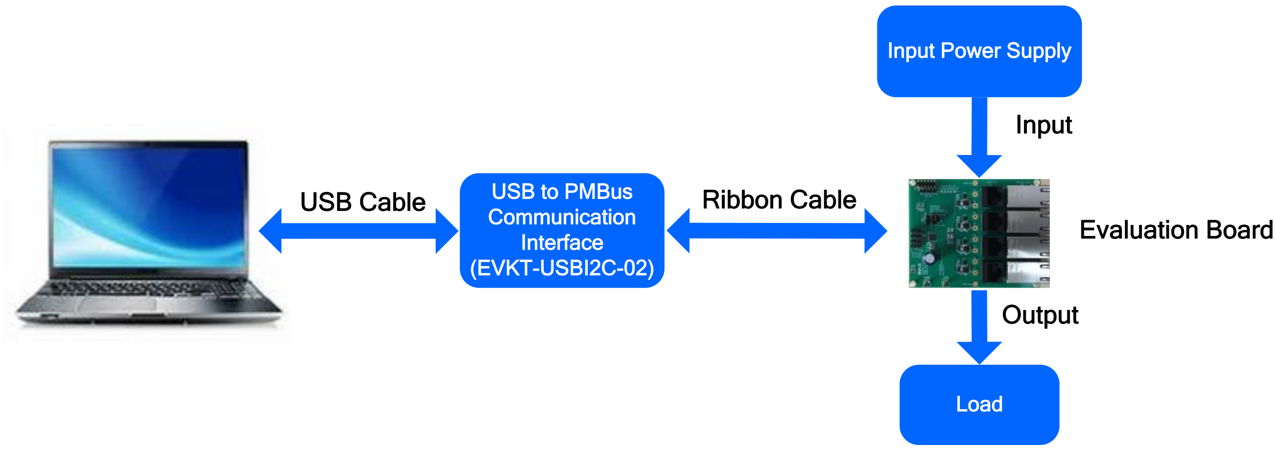


**Figure 1: EVKT-MP3924 Evaluation Kit Set-Up**


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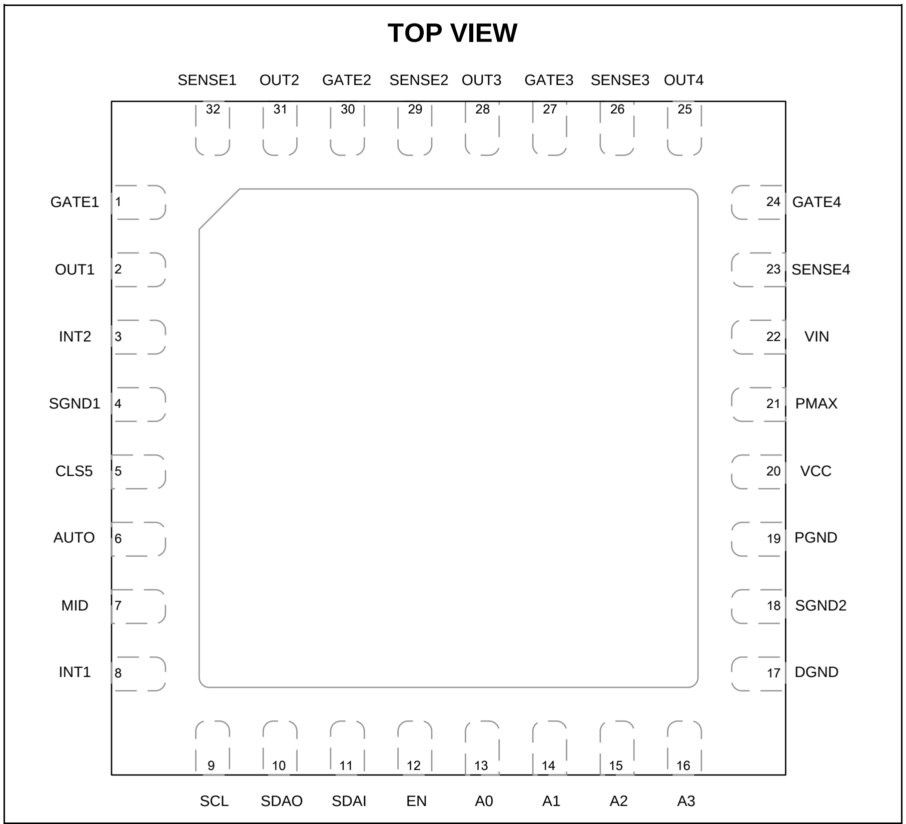
# PACKAGE REFERENCE




**QFN-32 (5mmx5mm)**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## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | GATE1 | **MOSFET gate driver for port 1.** Float the GATE1 pin if not used. |
| 2 | OUT1 | **Output voltage sense pin for port 1.** Connect OUT1 to the output interface return for detecting, classifying, voltage sensing, and current limit foldback control. Float the OUT1 pin if not used. |
| 3 | INT2 | **High-priority interrupt request pin.** INT2 pulls low when the selected high-priority interrupt source register is set and the interrupt is enabled. INT2 is an open-drain output. Connect INT2 to DGND if the interrupt function is not used. |
| 4 | SGND1 | **Current sense negative input for port 1 and port 2.** Connect SGND1 to the low-side terminal of the sense resistor. For an accurate current sense, use a Kelvin connection when connecting SGND1 to the PCB. Connect SGND1 to DGND if not used. |
| 5 | CLS5 | **Class 5 enable input.** CLS5 is internally pulled down to DGND through a 50kΩ resistor. Leave CLS5 disconnected to disable the classification for Class 5 devices (IEEE 802.3at-compliant mode). Connect CLS5 to VCC to enable the classification of Class 5 devices. CLS5's status is latched when the device starts up, or after a reset condition. If CLS5's status changes after start-up, there is no effect. |
| 6 | AUTO | **Automatic mode setting pin.** AUTO is internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can be added). Float the AUTO pin to make automatic mode the default. Connect the AUTO pin to DGND to make shutdown mode the default. AUTO's status is latched when the device starts up, or after a reset condition. If AUTO's status changes after start-up, there is no effect. |
| 7 | MID | **Midspan mode setting.** MID is internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can be added). Float the MID pin for midspan mode, then wait 2.8s to reinitiate detection. Connect the MID pin to DGND to disable midspan mode. MID's status is latched when the device starts up, or after a reset condition. If MID's status changes after start-up, there is no effect. |
| 8 | INT1 | **Interrupt request pin for all interrupt source events.** INT1 pulls low when the interrupt register is set and the interrupt function is enabled. INT1 is an open-drain output. Connect INT1 to DGND if the interrupt function is not used. |
| 9 | SCL | **I$^2$C clock input pin.** Connect SCL to VCC using an external pull-up resistor (typically 4.7kΩ). Connect SCL to VCC if the I$^2$C interface is not used. |
| 10 | SDAO | **I$^2$C serial data output pin.** SDAO is an open-drain output. Connect SDAO to VCC using an external pull-up resistor (typically 4.7kΩ). Connect SDAO to SDAI for non-isolated applications. Connect SDAO to DGND if the I$^2$C interface is not used. |
| 11 | SDAI | **I$^2$C serial data input pin.** Connect SDAI to VCC using an external pull-up resistor (typically 4.7kΩ). Connect SDAI to SDAO for non-isolated applications. Connect SDAI to DGND if the I$^2$C interface is not used. |
| 12 | EN | **Enable input.** EN turns all internal circuits and four ports (except the VCC regulator) on and off. To turn on the device automatically, externally connect EN to VCC. |
| 13 | A0 | **MP3924 address setting pin.** Connect A0 to VCC or DGND to set the lower 4-bit address bits (address = 010 A3 A2 A1 A0). The address signal is latched when the device starts up or is reset. A0 is internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added). |
| 14 | A1 | **MP3924 address setting pin.** Connect A1 to VCC or DGND to set the lower 4-bit address bits (Address = 010 A3 A2 A1 A0). The address signal is latched when the device starts up or is reset A1 is internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added). |


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## PIN FUNCTIONS *(continued)*

| Pin # | Name | Description |
|---|---|---|
| 15 | A2 | **MP3924 address setting pin.** Connect A2 to VCC or DGND to set the lower 4-bit address bits (Address = 010 A3 A2 A1 A0). The address signal is latched when the device starts up or is reset. A2 is internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can be added). |
| 16 | A3 | **MP3924 address setting pin.** Connect A3 to VCC or DGND to set the lower 4-bit address bits (Address = 010 A3 A2 A1 A0). The address signal is latched when the device starts up or is reset. A3 is internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added). |
| 17 | DGND | **Ground of the internal digital and analog circuit.** |
| 18 | SGND2 | **Current sense negative input for port 3 and port 4.** Connect SGND2 to the low-side terminal of the sense resistor. For an accurate current sense, use a Kelvin connection when connecting SGND2 to the PCB. Connect SGND2 to DGND if not used. |
| 19 | PGND | **Ground of input power supply.** |
| 20 | VCC | **3.3V internal regulator output for analog and digital circuit supply.** A minimum 1µF ceramic capacitor must be placed between VCC and DGND. |
| 21 | PMAX | **Maximum loading power setting pin.** Connect one resistor from the PMAX pin to DGND to set the total power capability on all four output ports. The MP3924 limits the total power on all four ports below this set limit. The PMAX setting signal is latched when the device starts up or is reset. |
| 22 | VIN | **Power supply input for both VCC and output ports.** Bypass VIN with at least one 0.1µF/100V ceramic capacitor, placed between VIN and PGND. |
| 23 | SENSE4 | **Current-sense pin from the high-side sense resistor terminal for port 4.** It is recommended to use a 0.25Ω sense resistor for all applications. For an accurate current sense, use a Kelvin connection when connecting SENSE4 during PCB layout. Connect SENSE4 to DGND if not used. |
| 24 | GATE4 | **MOSFET gate driver for port 4.** Float the GATE4 pin if not used. |
| 25 | OUT4 | **Output voltage sense pin for port 4.** Connect OUT4 to the return of the output interface for detecting, classifying, voltage sensing, and current limit foldback control. Float the OUT4 pin if not used. |
| 26 | SENSE3 | **Current-sense pin from the high-side sense resistor terminal for port 3.** It is recommended to use a 0.25Ω sense resistor for all applications. For an accurate current sense, use a Kelvin connection when connecting SENSE3 during PCB layout. Connect SENSE3 to DGND if not used. |
| 27 | GATE3 | **MOSFET gate driver for port 3.** Float the GATE3 pin if not used. |
| 28 | OUT3 | **Output voltage sense pin for port 3.** Connect OUT3 to the return of the output interface for detecting, classifying, voltage sensing, and current limit foldback control. Float the OUT3 pin if it is not used. |
| 29 | SENSE2 | **Current-sense pin from the high-side sense resistor terminal for port 2.** It is recommended to use a 0.25Ω sense resistor for all applications. For an accurate current sense, use a Kelvin connection when connecting SENSE1 during PCB layout. Connect SENSE1 to DGND if not used. |
| 30 | GATE2 | **MOSFET gate driver for port 2.** Float the GATE2 pin if not used. |
| 31 | OUT2 | **Output voltage sense pin for port 2.** Connect OUT2 to the return of the output interface for detecting, classifying, voltage sensing, and current limit foldback control. Float the OUT2 pin if it is not used. |
| 32 | SENSE1 | **Current-sense pin from the high-side sense resistor terminal for port 1.** It is recommended to use a 0.25Ω sense resistor for all applications. For an accurate current sense, use a Kelvin connection when connecting SENSE1 during PCB layout. Connect SENSE1 to DGND if not used. |


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## ABSOLUTE MAXIMUM RATINGS [1]

$V_{IN}$ ............................................ -0.3V to +80V
OUT1~4................................-0.3V to $V_{IN}$ + 0.3V
GATE1~4, SENSE1~4................. -0.3V to +22V
DGND, SGND1, SGND2............. -0.3V to +0.3V
All other pins............................... -0.3V to +6.5V
INT1, INT2, SDAO maximum sink current……...
……………………………………………..20mA
Continuous power dissipation ($T_A$ = 25°C)
…………………………………………...3.9W [2] [4]
Junction temperature ............................... 150°C
Lead temperature .................................... 260°C
Storage temperature................ -65°C to +150°C

### *Recommended Operating Conditions* [3]

Supply voltage ($V_{IN}$) ......................... 44V to 57V
INT1, INT2, SDAO maximum sink current……...
…………………………………………………5mA
Operating junction temp ($T_J$). ... -40°C to +125°C

| *Thermal Resistance* | $\theta_{JA}$ | $\theta_{JC}$ | |
|---|---|---|---|
| EV3924-U-00A [4] | 32 | 2 | °C/W |
| JESD51-7 [5] | 36 | 8 | °C/W |

**Notes:**

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can cause excessive die temperature, and the regulator may go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EV3924-U-00A, 2-layer, 88mmx106mm PCB.
5) The value of $\theta_{JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.


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## ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 54V, PGND, DGND, SGND1, and SGND2 are connected together, $R_{SENSE}$ = 0.25Ω, $T_J$ = -40°C to +125°C (6), typical value is tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Power Supply** | | | | | | |
| Input under-voltage lockout (UVLO) | $V_{IN\_UVLO}$ | $V_{IN}$ rising | 28 | 29.5 | 31 | V |
| Input UVLO hysteresis | $V_{IN\_UVLO\_HYS}$ | | | 2.7 | | V |
| Input over-voltage lockout (OVLO) | $V_{IN\_OVP}$ | $V_{IN}$ rising | 62 | 65 | 68 | V |
| Input OVLO hysteresis | $V_{IN\_OVP\_HYS}$ | | | 2.8 | | V |
| Input OVP lockout delay (7) | | | | 100 | | µs |
| Input power okay threshold | $V_{IN\_OK}$ | $V_{IN}$ rising | 38 | 40 | 42 | V |
| Input power okay hysteresis | $V_{IN\_OK\_HYS}$ | | | 0.7 | | V |
| EN logic high voltage | $V_{HI}$ | | 2.5 | | | V |
| EN logic low voltage | $V_{LI}$ | | | | 0.4 | V |
| EN input current | | Pull EN to 0V, 3.3V | | 0 | | µA |
| EN turn on/off delay | $t_{EN\_ON}$ | EN pin high pulse duration for start-up or low-pulse duration for shutdown | | 150 | | µs |
| | $t_{EN\_OFF}$ | | | 120 | | |
| Supply current | $I_{IN}$ | Logic pin is floating, no connection for all output ports, AUTO = low | | 2 | 4 | mA |
| Shutdown current | $I_{SD}$ | EN = 0V | | 150 | | µA |
| VCC regulation | $V_{CC}$ | Load = 0mA | | 3.3 | | V |
| | | Load = 15mA | | 3.2 | | |
| VCC UVLO | $V_{CC\_UVLO}$ | $V_{CC}$ rising | 2.3 | 2.5 | 2.7 | V |
| VCC UVLO hysteresis | $V_{CC\_UV\_HYS}$ | | | 170 | | mV |
| VCC current limit | | VCC = DGND | | 17 | | mA |
| Power-on reset (POR) delay | $t_{POR}$ | From VCC on to detection | | 0.5 | | ms |
| **Detection** | | | | | | |
| First detection voltage | $V_{DET1}$ | Test the VIN to OUTx pins | 3.6 | 4 | | V |
| Second detection voltage | $V_{DET2}$ | Test the VIN to OUTx pins | 7.2 | 8 | | V |
| Detection voltage slew rate | $V_{SLEW}$ | $C_{DET}$ = 0.1µF | | | 0.02 | V/µs |
| Detection current limit | $I_{DET\_LIMIT}$ | Short VIN to OUTx | 1 | 1.2 | 1.5 | mA |
| Short-circuit detection threshold | $V_{SC}$ | First detection voltage | 1 | 1.5 | 1.8 | V |
| Open-circuit current threshold | $I_{OPEN}$ | | 10 | 15 | 25 | µA |


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## ELECTRICAL CHARACTERISTICS *(continued)*

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| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Minimum valid detection resistance | $R_{GOODL}$ | | 15 | 17 | 19 | kΩ |
| Maximum valid detection resistance | $R_{GOODH}$ | | 26.5 | 30 | 33 | kΩ |
| Maximum valid capacitance | $C_{GOOD\_MAX}$ | | 1 | | 9 | µF |
| Detection time | $t_{DET}$ | Second detection phase | | 280 | 310 | ms |
| Detection reset time | $t_{RESET}$ | Port reset by internal discharge between VIN and OUTx before detection starts | | 80 | 100 | ms |
| Midspan mode detection delay | $t_{MIDDLY}$ | Re-detection interval, MID = 1 | | 2.8 | | sec |
| Power removal detection delay | $t_{REMDLY}$ | Re-detection after one power removal event due to error condition (ICUT, ILIM, INRUSH), fault timer = 60ms MID = 0, automatic and semi-automatic mode | 0.8 | 0.96 | 1.12 | sec |
| **Classification** | | | | | | |
| Classification output voltage | $V_{CLS}$ | Test VIN to OUTx pins during classification, load < 60mA | 16 | 18 | 20 | V |
| Classification current limit | $I_{CLS\_ILIM}$ | Short VIN to OUTx | | 70 | | mA |
| Class event time | $t_{CLE}$ | | 8 | 15 | 22 | ms |
| Mark event voltage | $V_{MARK}$ | Test VIN to OUTx pins | 7.6 | 8.8 | 9.8 | V |
| Mark event current limit | $I_{MARK\_ILIM}$ | Short VIN to OUTx | 6 | 10 | 14 | mA |
| Mark event time | $t_{ME}$ | | 6.5 | 9 | 11 | ms |
| Classification current threshold | $I_{CLS}$ | Class 0 to 1 | 5.5 | 6.5 | 7.5 | mA |
| | | Class 1 to 2 | 13.5 | 14.5 | 15.5 | mA |
| | | Class 2 to 3 | 21.5 | 23 | 24.5 | mA |
| | | Class 3 to 4 | 31.5 | 33 | 34.5 | mA |
| | | Class 4 to over-current (OC) condition (or Class 5 (8)) | 45.5 | 48 | 50.5 | mA |
| Port start-up delay | $t_{PON}$ | Automatic mode from detection ending to power port above 21V | | | 100 | ms |
| | | Manual mode, from command to output port above 21V | | | 3 | ms |
| Port shutdown delay | | From command off to gate < 1V | | | 0.5 | ms |
| Start-up sequence delay (9) | | From one channel detection to the next channel detection if the first channel powers up in automatic mode | | 0.5 | | sec |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 54V, PGND, DGND, SGND1, and SGND2 are connected together, $R_{SENSE}$ = 0.25Ω, $T_J$ = -40°C to +125°C (6), typical value is tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Gate Driver** | | | | | | |
| GATE source capability | $I_{SOURCE}$ | Port start-up, $V_{GATE}$ = GND | | -43 | | µA |
| GATE sink capability | $I_{SINK}$ | Port shutdown, $V_{GATE}$ = 10V | | 60 | | µA |
| | | Port shutdown, $V_{GATE}$ < 1V | | 9 | | mA |
| | | Trigger SCP, $V_{SENSE}$ = 450mV, $V_{GATE}$ = 5V (7) | | 100 | | mA |
| GATE clamp voltage | $V_{GS\_MAX}$ | Float GATE pin | | 10 | | V |
| **OUT Pin** | | | | | | |
| OUT pin resistance | $R_{OUT}$ | Between VIN and OUTx, pull OUTx high in idle state (detection/classification off, port shutdown) | | 0.2 | | MΩ |
| OUT pin bias current | $I_{OUT}$ | OUTx = 0V, port start-up | | -270 | | µA |
| | | OUTx = 54V, port shutdown | | | 1 | µA |
| **Protection** | | | | | | |
| Output power good (PG) rising threshold | $V_{PG}$ | OUTx pin voltage decrease | 1.5 | 2 | 2.5 | V |
| Output PG hysteresis | $V_{PG\_HYS}$ | | | 400 | | mV |
| PG delay | | Low to high deglitch | | 3 | | ms |
| | | High to low deglitch | | 10 | | µs |
| Current limit threshold | $V_{ILIM}$ | Class 0~3, ILIMx bit = 0 | 101 | 106.25 | 111.5 | mV |
| | | Class 4, ILIMx bit = 1 | 201 | 212.5 | 224 | mV |
| | | Class 5, ILIMx bit = 1 | 251.75 | 265 | 278.25 | mV |
| Over-current (OC) detection threshold | $V_{CUT}$ | Class 0~3 (ICUTx = 000) | 89.06 | 93.75 | 98.44 | mV |
| | | Class 4 (ICUTx = 100) | 154.38 | 162.5 | 170.63 | mV |
| | | Class 5 (ICUTx = 101) | 218.5 | 230 | 241.5 | mV |
| Current limit timer | $t_{ILIM}$ | TILIM = 11 | 50 | 60 | 70 | ms |
| OC timer | $t_{ICUT}$ | TCUT = 10 | 50 | 60 | 70 | ms |
| Start inrush current limit timer | $t_{INRUSH}$ | TINRUSH = 10 | 50 | 60 | 70 | ms |
| Foldback initial voltage | $V_{FOLD\_ST}$ | OUTx pin voltage when ILIM decreases, ILIMx bit = 0 | | 32 | | V |
| | | OUTx pin voltage when ILIM decreases, ILIMx bit = 1 | | 18 | | V |
| Foldback end voltage | $V_{FOLD\_END}$ | OUTx pin voltage when ILIM decreases to minimum value | | 46 | | V |
| Foldback minimum current limit | $V_{LIM\_MIN}$ | Short VIN to OUTx, FBLIMT bit = 1, Class 4 | | 40 | | mV |
| | | Short VIN to OUTx, FBLIMT bit = 0, Class 4 | | 22 | | mV |


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## ELECTRICAL CHARACTERISTICS *(continued)*

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| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Short circuit fast-off threshold | $V_{SCP}$ | ILIMx bit = 0 | | 212 | | mV |
| | | ILIMx bit = 1 | | 425 | | mV |
| Sense pin bias current | | | -1 | | +1 | µA |
| Thermal shutdown (7) | | | | 150 | | °C |
| Thermal shutdown hysteresis (7) | | | | 25 | | °C |
| **Total Load Power Limit** | | | | | | |
| Load power limit on all four ports | $P_{MAX}$ | $R_{MAX}$ = 49.9kΩ | | 49.9 | | W |
| | | $R_{MAX}$ = 120kΩ | | 120 | | W |
| Maximum load capability on all four ports | $P_{MAX\_LIMT}$ | Float the PMAX pin | | 204.8 | | W |
| Maximum load power protection delay | $t_{MAX\_DLY}$ | TPMAX bit = 10<br>100% x $P_{MAX}$ < load < 150% x $P_{MAX}$ | | 60 | | ms |
| | | Load > 150% x $P_{MAX}$ | | 2 | | ms |
| **DC Load Disconnection** | | | | | | |
| DC disconnect hold threshold | $V_{DCHOLD}$ | Decrease output load until output port power off | 1.25 | 1.875 | 2.5 | mV |
| DC connect power time | $t_{DCON}$ | Load time to reset $t_{DCOFF}$ timer | 37.5 | 43.75 | 50 | ms |
| DC disconnect power remove time | $t_{DCOFF}$ | Time from load < $V_{DCHOLD}$ to gate off | 300 | 350 | 400 | ms |
| **Analog-to-Digital Converter (ADC)** | | | | | | |
| ADC resolution | | | | 9 | | bits |
| Max ADC current range | | ADC results = 1 1111 1111 (2.4mA/count) | | 1.216 | | A |
| Max ADC voltage range | | ADC results = 1 1111 1111 (0.15V/count) | | 76.65 | | V |
| ADC junction temperature range | | ADC results = 0 0000 0000 to 1 1111 1111 (0.4°C/count) | -40 | | +164.4 | °C |
| Max ADC PMAX setting range | | ADC results = 1 1111 1111 (0.4W/count) | | 204.8 | | W |
| Current conversion | | I = 600mA | | 254 | | count |
| Voltage conversion | | V = 44V | | 293 | | count |
| | | V = 57V | | 380 | | count |
| Temperature conversion (7) | | $T_J$ = 25°C | | 163 | | count |
| | | $T_J$ = 125°C | | 413 | | count |
| PMAX setting conversion | | $R_{MAX}$ = 49.9kΩ | | 125 | | count |
| | | $R_{MAX}$ = 120kΩ | | 300 | | count |


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## ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 54V, PGND, DGND, SGND1, and SGND2 are connected together, $R_{SENSE}$ = 0.25Ω, $T_J$ = -40°C to +125°C (6), typical value is tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Logic Interface (SCL, SDAI, SDAO, INT1, INT2, MID, A0, A1, A2, A3, AUTO, CLS5)** | | | | | | |
| Input logic low voltage | $V_{LI}$ | | | | 0.4 | V |
| Input logic high voltage | $V_{HI}$ | | 2 | | | V |
| Logic input current | | For SCL, SDAI | -1 | | +1 | µA |
| Open-drain output logic low voltage | $V_{LO}$ | Sink current = 3mA, SDAO, INT1, INT2 | | | 0.4 | V |
| Open-drain output logic high leakage | | Open drain to 3.3V | | | 1 | µA |
| Internal pull-up/down Resistance | $R_{UP}$ | A0, A1, A2, A3, AUTO, MID to VCC, CLS5 to DGND | | 50 | | kΩ |

**Notes:**

6) Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.
8) If CLS5 is enabled, the MP3924 treats the classification current range from the upper of class 4 to the classification current limit as class 5.
9) Guaranteed by detection time, classification time, and start-up delay time.


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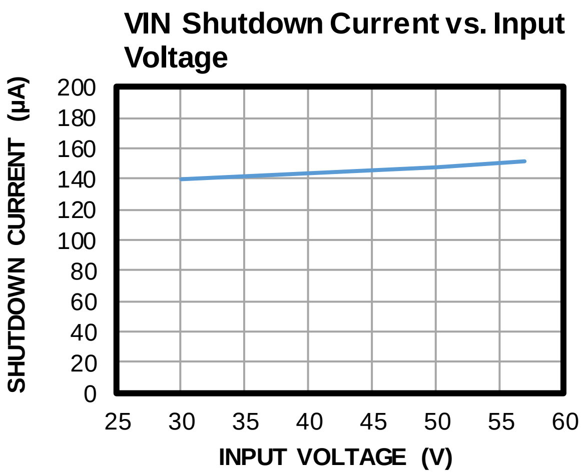
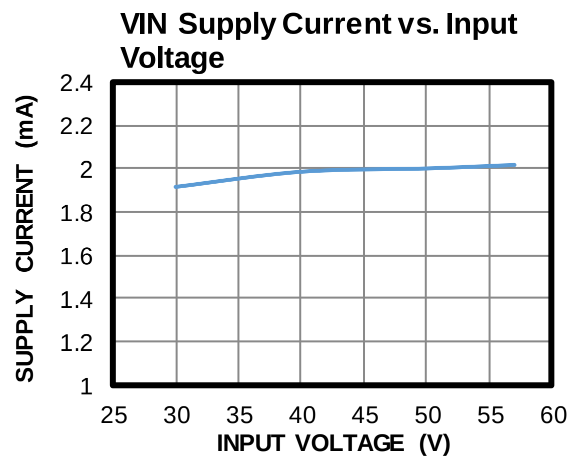
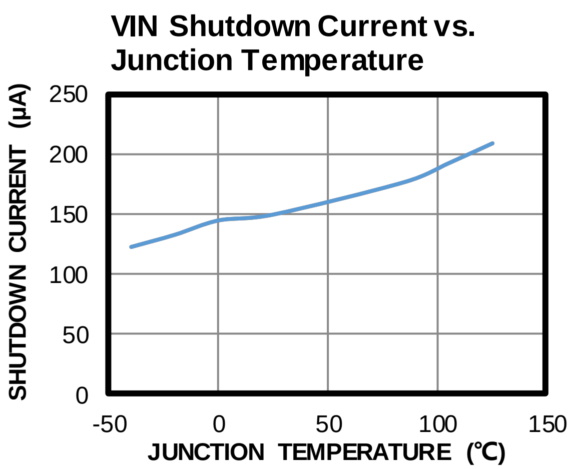
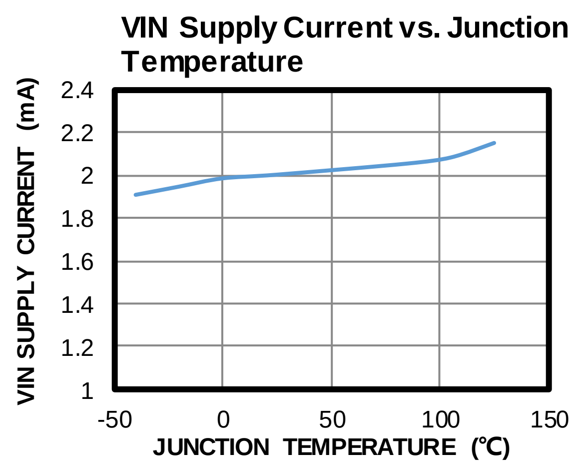
## TYPICAL CHARACTERISTICS

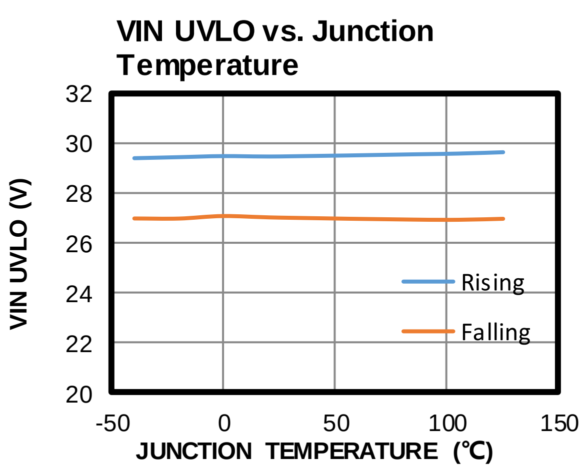
**$V_{IN}$ = 54V, $T_A$ = 25°C, unless otherwise noted.**

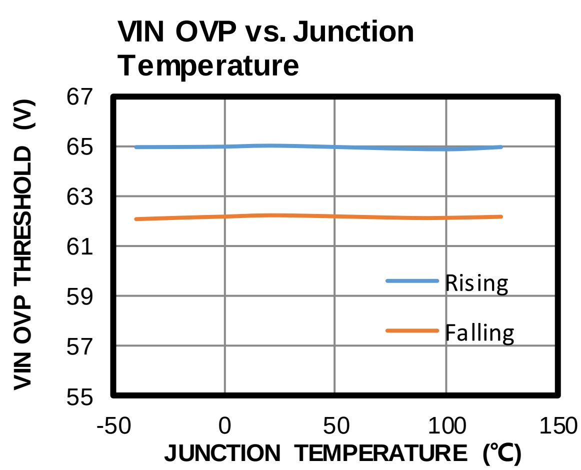




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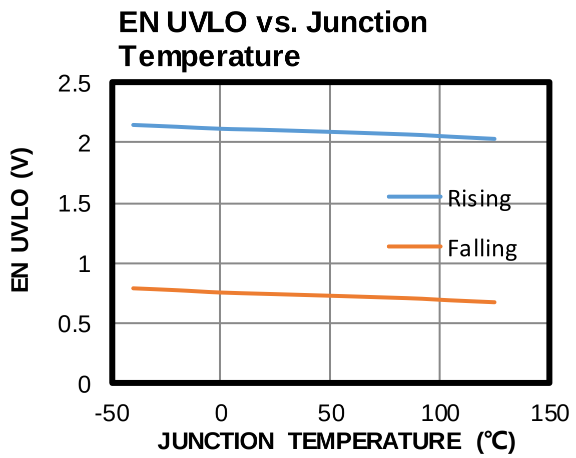
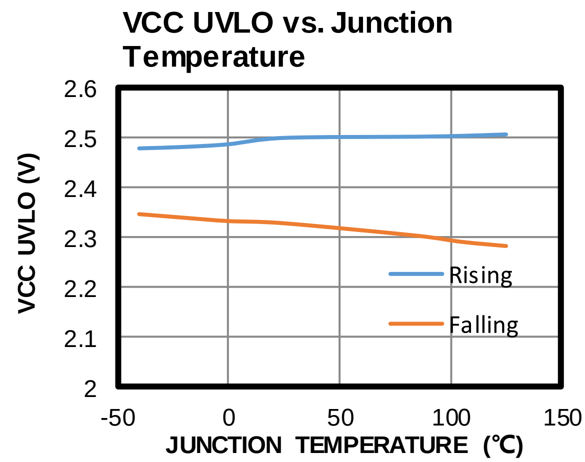
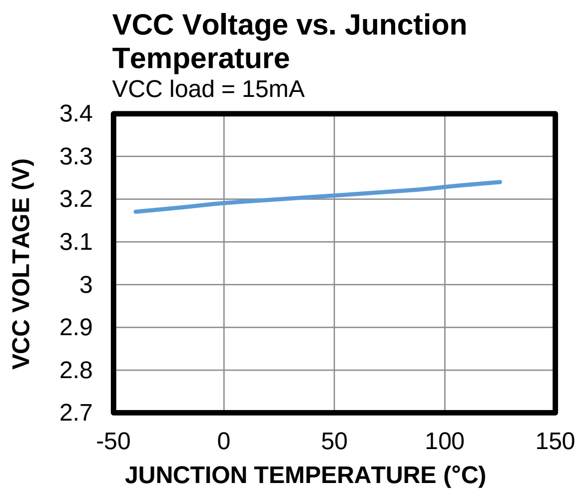
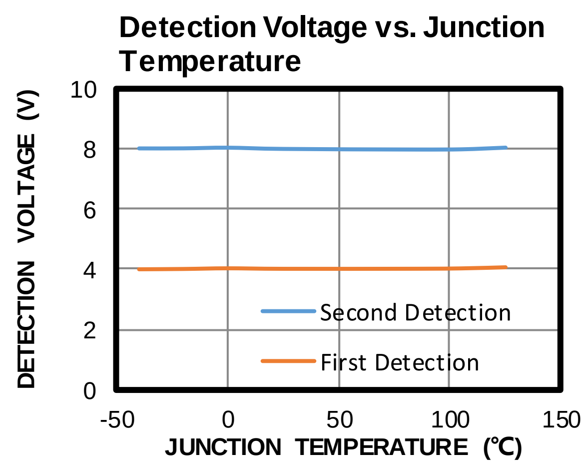
## TYPICAL CHARACTERISTICS *(continued)*

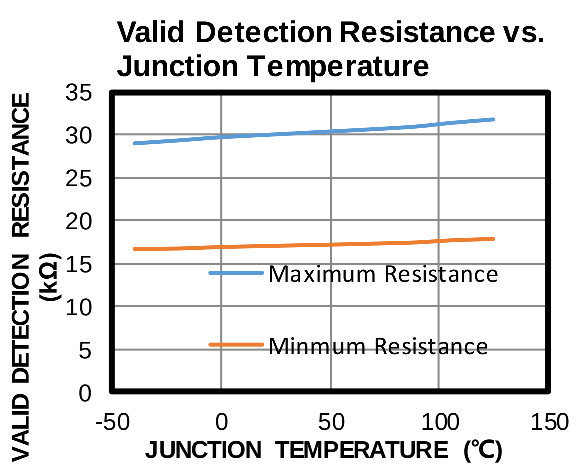
**$V_{IN}$ = 54V, $T_A$ = 25°C, unless otherwise noted.**

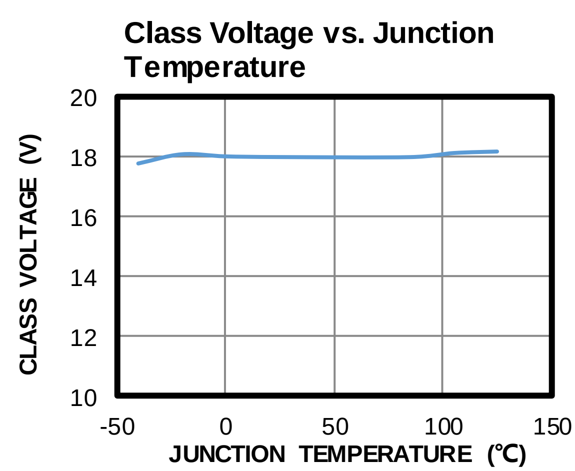




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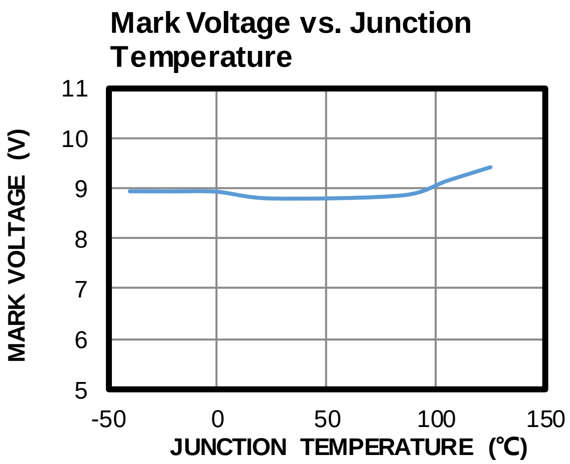


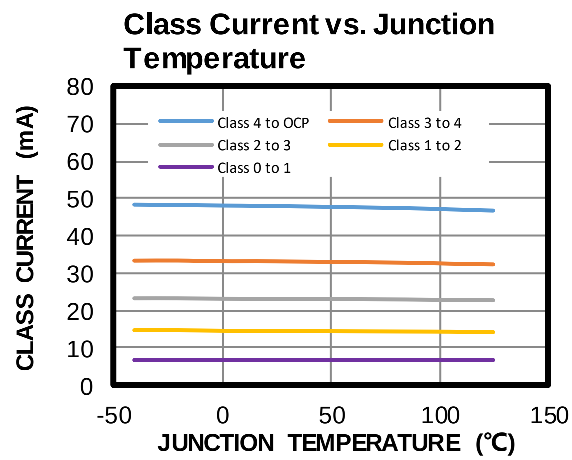


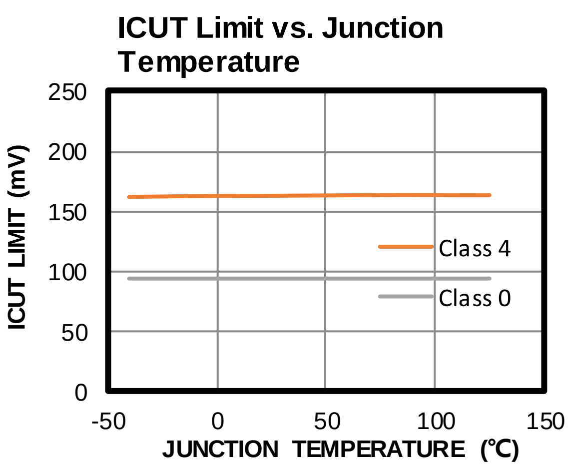


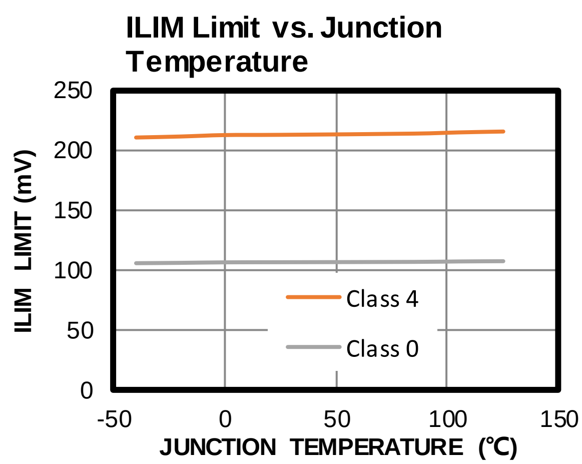


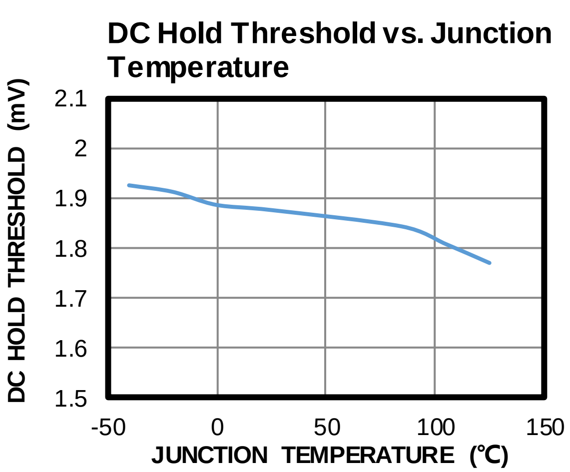


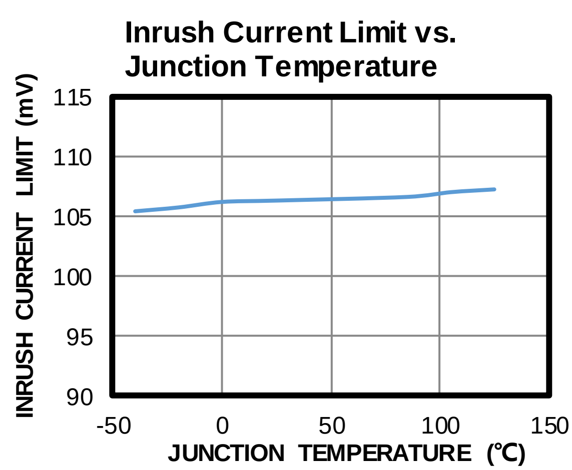



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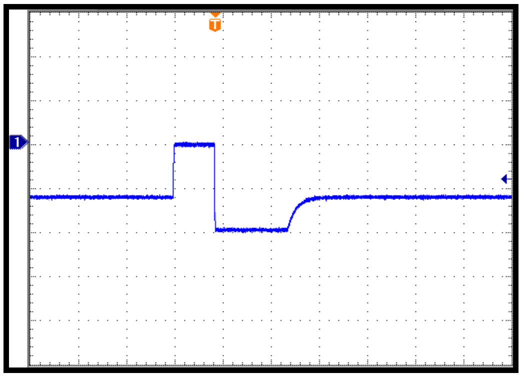
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 54V, set with a Class 4 PD load, $T_A$ = 25°C, unless otherwise noted.**

### No PD Connection

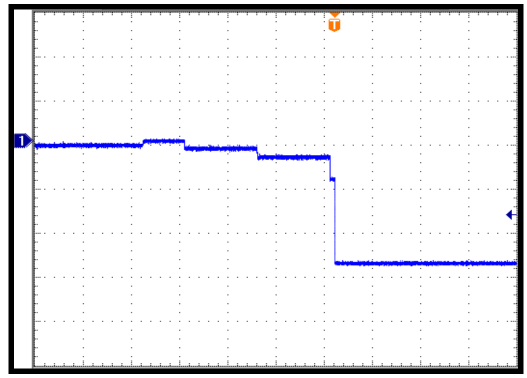
CH1: $V_{OUTx}$ - $V_{VIN}$ 2V/div.



100ms/div.

### Class 0~3 PD Connection

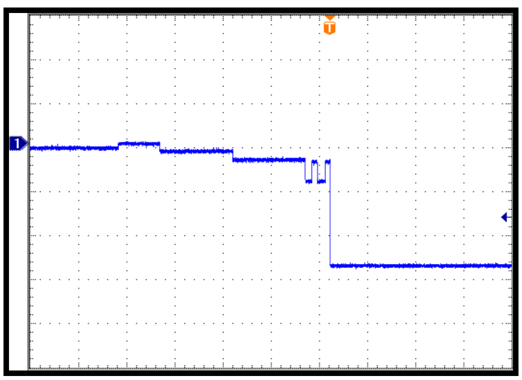
CH1: $V_{OUTx}$ - $V_{VIN}$ 20V/div.



100ms/div.

### Class 4 PD Connection

CH1: $V_{OUTx}$ - $V_{VIN}$ 20V/div.

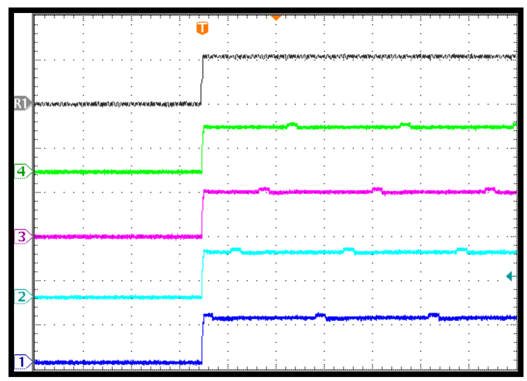


100ms/div.

### Start-Up through VIN

No PD connection

R1: $V_{IN}$ 50V/div.
CH4: OUT4 50V/div.
CH3: OUT3 50V/div.
CH2: OUT2 50V/div.
CH1: OUT1 50V/div.

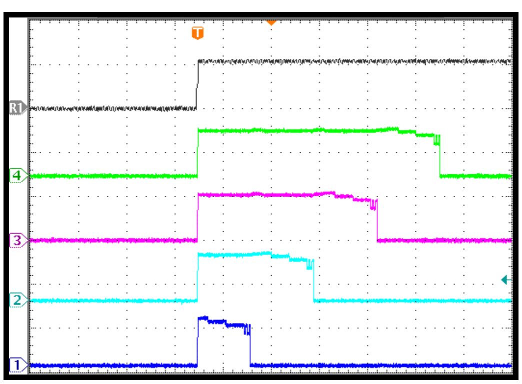


400ms/div.

### Start-Up through VIN

Class 4 PD connection

R1: $V_{IN}$ 50V/div.
CH4: OUT4 50V/div.
CH3: OUT3 50V/div.
CH2: OUT2 50V/div.
CH1: OUT1 50V/div.

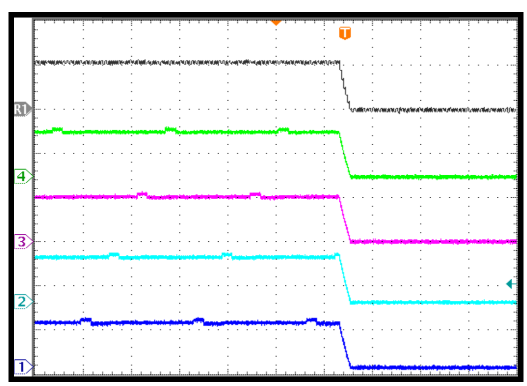


400ms/div.

### Shutdown through VIN

No PD connection

R1: $V_{IN}$ 50V/div.
CH4: OUT4 50V/div.
CH3: OUT3 50V/div.
CH2: OUT2 50V/div.
CH1: OUT1 50V/div.



400ms/div.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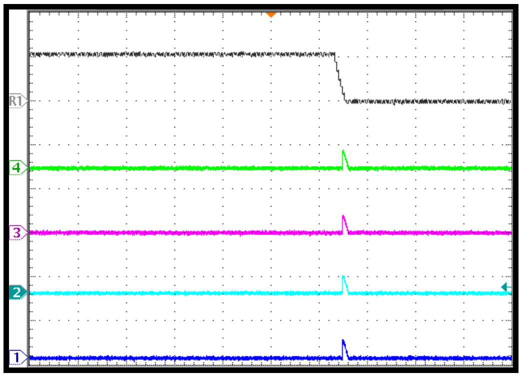
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 54V, set with a Class 4 PD load, $T_A$ = 25°C, unless otherwise noted.**

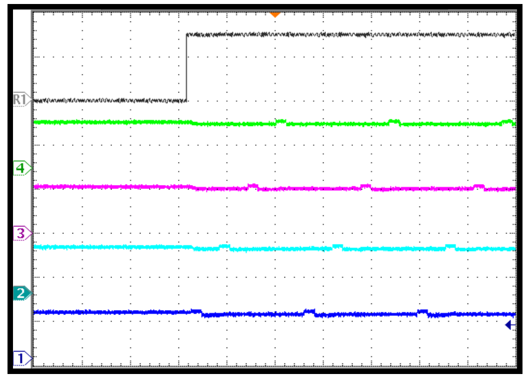
### Shutdown through VIN

Class 4 PD connection



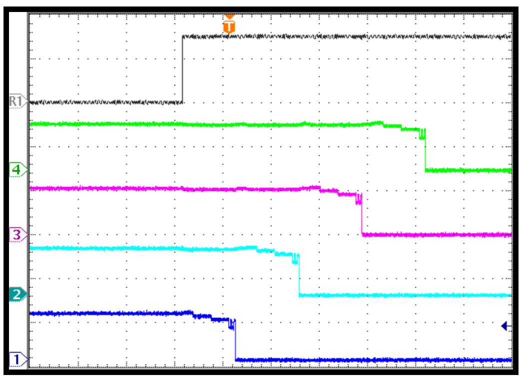

### Start-Up through EN

No PD connection



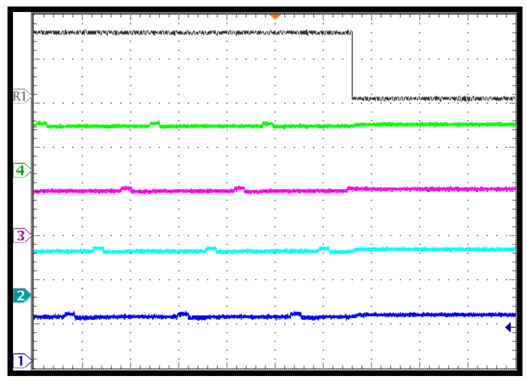

### Start-Up through EN

Class 4 PD connection



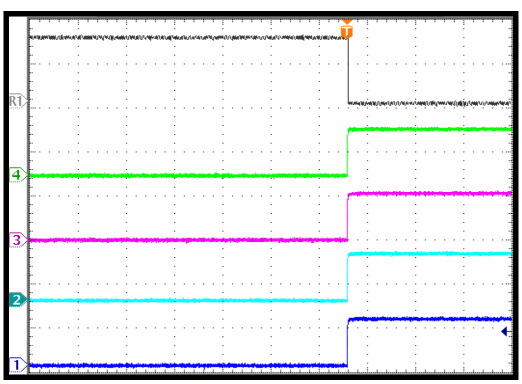

### Shutdown through EN

No PD connection

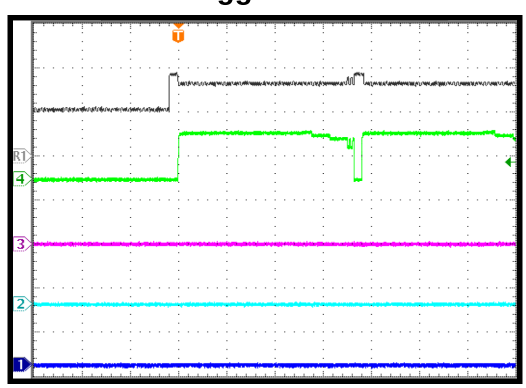



### Shutdown through EN

Class 4 PD connection




### PMAX Limit Triggered (10)




**Note:**

10) The maximum power ($P_{MAX}$) is set to 50W. If the load's power exceeds 50W, port 4 shuts down with default priority.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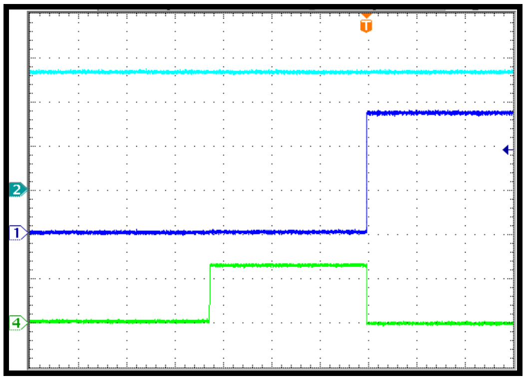
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 54V, set with a Class 4 PD load, $T_A$ = 25°C, unless otherwise noted.**

### ICUT Triggered

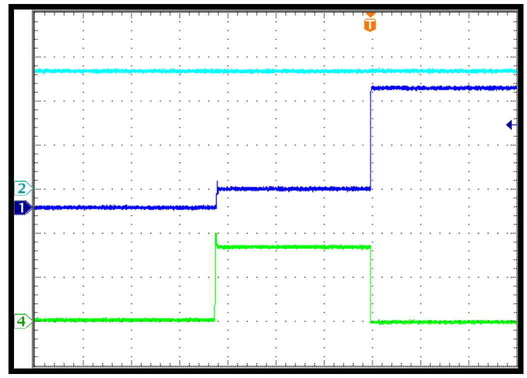
CH2: $V_{IN}$ 20V/div.
CH1: OUT1 20V/div.
CH4: $I_{OUT1}$ 500mA/div.



20ms/div.

### ILIM Triggered

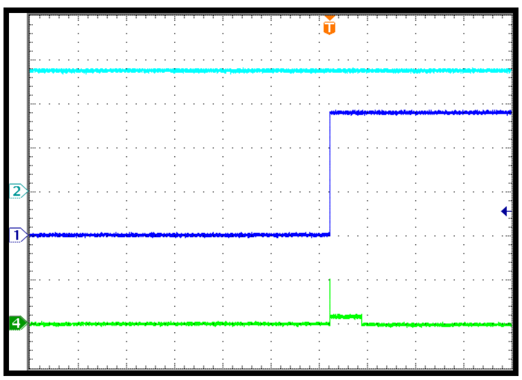
CH2: $V_{IN}$ 20V/div.
CH1: OUT1 20V/div.
CH4: $I_{OUT1}$ 500mA/div.



20ms/div.

### Output SCP Triggered

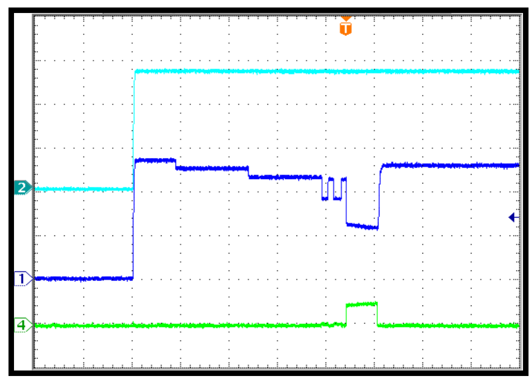
CH2: $V_{IN}$ 20V/div.
CH1: OUT1 20V/div.
CH4: $I_{OUT1}$ 1A/div.



100ms/div.

### Inrush Current Limit Triggered

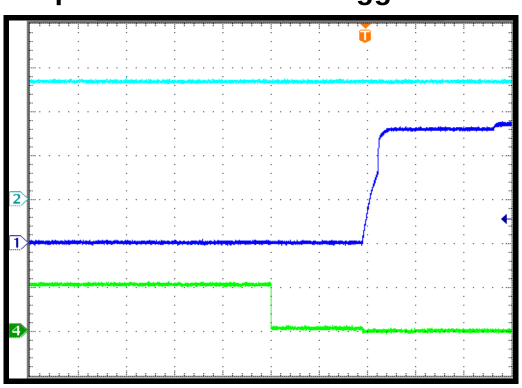
CH2: $V_{IN}$ 20V/div.
CH1: OUT1 20V/div.
CH4: $I_{OUT1}$ 1A/div.



100ms/div.

### Output Disconnection Triggered

CH2: $V_{IN}$ 20V/div.
CH1: OUT1 20V/div.
CH4: $I_{OUT1}$ 100mA/div.



200ms/div.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# FUNCTIONAL BLOCK DIAGRAM

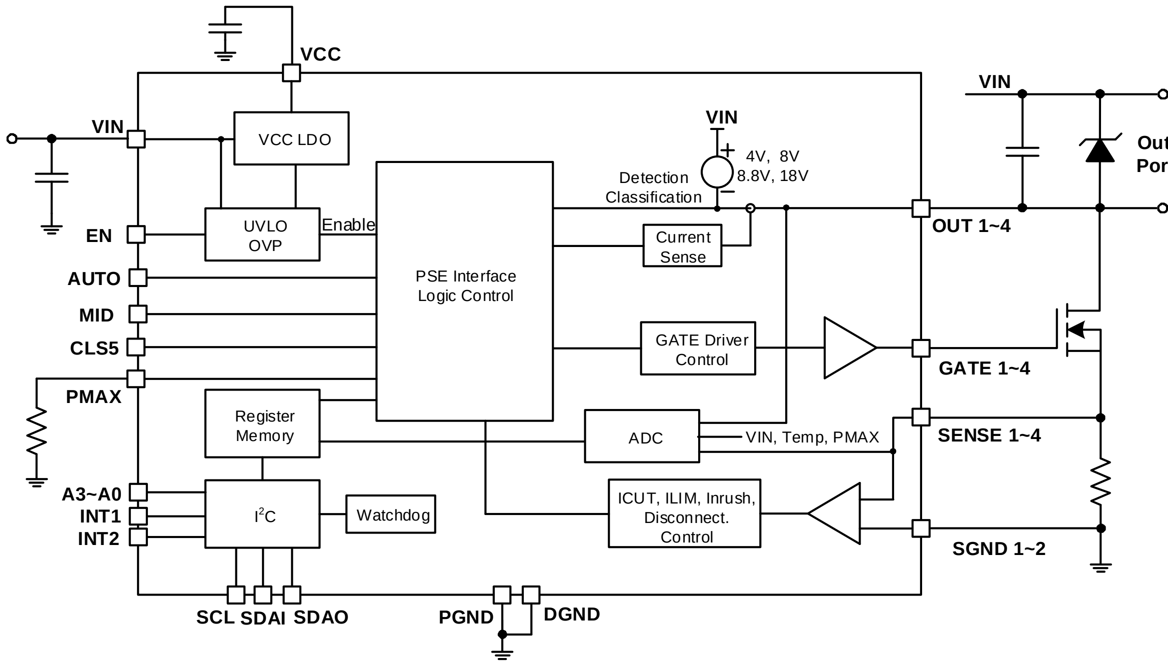


**Figure 2: Functional Block Diagram**


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# OPERATION

The MP3924 is a quad-output power source equipment (PSE) power controller for IEEE 802.3af/at power over Ethernet (PoE) applications. The device establishes a method of communication between the powered device (PD) and PSE with detection, classification, and marked events. The MP3924 also provides functions for current and voltage protections in automatic mode as well as $I^2C$ command control mode.

## Power Supply

The MP3924 is designed for PoE applications that require a 44V to 57V input. The MP3924 powers the output port from this input source, then generates an internal 3.3V for the digital and analog circuits. The VCC regulator is enabled after VIN powers on. When $V_{IN}$ exceeds $V_{IN\_UVLO}$, the part is enabled after a delay ($t_{POR}$). All functions can be enabled or disabled by both VCC and EN going above or below the under-voltage lockout (UVLO) value, respectively.

The MP3924 uses the PORT_ENABLE register to disable functions related to all ports, as well as functions related to individual ports. The PORT_ENABLE register does not include VIN, VCC, or EN UVLO.

The device can be reset by any of the below conditions:

- VIN or VCC UVLO
- EN turning off
- Writing 0 to the ENAL bit

After the MP3924 resets, all internal register are set to their default values. The following pins are read and latched into the internal registers:

- AUTO
- MID
- CLS5
- PMAX
- A3~A0

During normal operation, changes to these pins do not affect the registers.

The MP3924 includes one $V_{IN}$ over-voltage protection (OVP) threshold at about 65V. All ports shut down if input OVP is triggered. The MP3924 outputs can restart with a new detection cycle after OVP recovery.

## PD Detection

In normal idle operation, the MP3924 detects the output port for a valid PD connection, which typically has a 24.9kΩ resistance (see Figure 3).

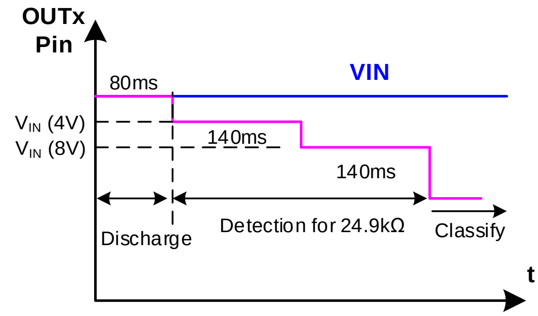


**Figure 3: PD Detection Process**

During this detection process, the MP3924 generates a two-phase voltage (4V/8V) through the OUTx pin. Meanwhile, the external MOSFET is off (see Figure 4).

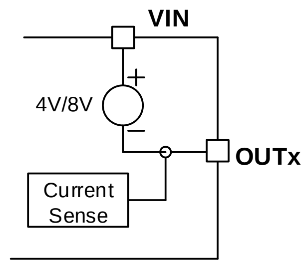


**Figure 4: PD Detection Block Diagram**

The OUTx pin sinking current capability is limited to about 1.2mA. The current and voltage through the OUTx pin are measured. If the effective resistance with the two-point test is valid, this means that one PD device is connected to the PSE port. The MP3924 integrates a filter to avoid 50Hz/60Hz power line noise.

After the detection cycle, the DETCx bit is set, and an interrupt signal is generated to report that detection has completed. The host can read each port's DET/CLS_RESULT register to obtain the detection results. After one detection cycle, the MP3924 enters classification mode if the PD connection is valid.

If the output port is shorted or the detected capacitance is too high, the OUTx pin limits the


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sink current to about 1.2mA. Then the detection cycle ends.

If the output port has an open circuit in the first phase detection period, the MP3924 ends the detection cycle. If the OUTx pin has a low impedance to PGND, detection ends immediately.

For other invalid resistance signatures, the MP3924 ends detection after two-phase detection. After one invalid detection result, the MP3924 stays in idle mode and re-enables detection within an 80ms port reset time. In midspan mode, there is one delay time (about 2.8s) before the 80ms reset time.

### Midspan Mode

If a port is set to midspan mode, the device waits about 2.8s before attempting to detect a PD connection. This can avoid detection collision. Midspan mode can be set or reset by the MID pin before the MP3924 starts up. Midspan mode can also be configured via the MIDx bits via the $I^2C$ interface during normal operation. If the detection is valid, the device exits midspan mode.

### PD Classification

If the PD detection resistance is valid, the device enters classification mode to measure the power level of the connected PD. Different classifications support 4W, 7W, 15.4W, or 30W of power to the port. Based on the IEEE802.3af/at standard, the MP3924 provides one additional class: Class 5 (see Figure 5).

Class 5 classification has a 40W load capability, which is valid when the CLS5_EN bit is enabled and the classification current exceeds the Class 4 upper current threshold. If Class 5 is not enabled, a classification current that exceeds 50.5mA results in an over-current (OC) condition and a classification failure. If Class 5 is enabled, a classification current that exceeds 50.5mA results in a Class 5 classification level. In this scenario, an OC condition refers to when the current has triggered the current limit threshold. OC conditions can occur with all classes.

The CLS5 pin is internally pulled down to DGND to disable Class 5 classification. Pull the CLS5 pin high during a power-on reset (POR) to enable Class 5 classification. Another method to enable Class 5 is to use the enable the CLS5_ENx bits on a port.

During classification, the MP3924 outputs a 18V voltage on the OUTx pin (see Figure 5). The device then measures the current though the OUTx pin to determine the classification level. After classification is complete, the status bits (CLSCx) and interrupt are set. The classification result is stored in the DET/CLS Result register.

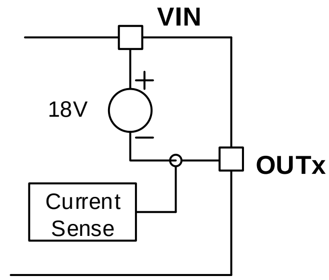


**Figure 5: Classification Block Diagram**

Classification is based on the IEEE802.3at standards. If a classification result is in Class 0~3, the MP3924 only performs one-time classification in accordance with IEEE 802.3af. If Class 4 or Class 5 is detected in the first classification event, the MP3924 performs a second classification event when the voltages on VIN and OUTx are the same. 2-event classification can be enabled by 2EVNTENx (see Figure 6).

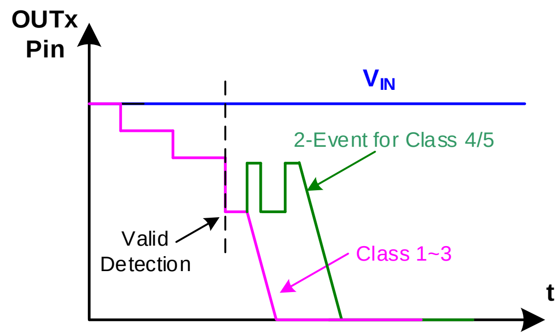


**Figure 6: 1-Event and 2-Event Classification**

Between the two classifications, the MP3924 performs two time mark events between VIN and OUTx with an 8.8V mark voltage. The second classification result must be equal to the first classification result, or the classification is considered invalid.

After each 2-event classification, the output port generates an 8.8V voltage to perform the mark


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event. During a classification mark event, the OUTx pins have sink and source current capability. This means that the output port voltage can use a 0.1µF capacitor to follow the OUTx pin's regulated voltage.

The classification circuit is disabled when the classification result is valid and the port output is powered up.

### Start-Up

If the detection and classification results are valid, the MP3924 ramps up the port's output power. This power is delivered to the PD circuit. The PENx and PECx bits are then set to indicate the port status. When the power supply ($V_{IN}$) is between 44V and 57V, the MP3924 can operate from 31V and report over-voltage (OV) conditions at 65V. If the OUTx pin voltage drops below 2V, the PGx and PGCx bits are set to indicate the power good (PG) result.

If the detection is valid but the port does not start up within 400ms in automatic or semi-automatic mode, then the port initializes a new detection cycle.

### Four-Channel Sequence

The MP3924 detects, classifies, and starts up the ports one at a time. Port one is first, followed by the second, third, and fourth ports.

If no PD is plugged in, the detection process goes one by one (see Figure 7).

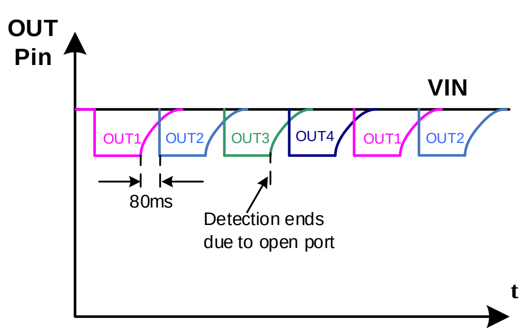


**Figure 7: No PD on an Output Port**

The next port starts detecting within the 80ms discharge time after the previous port's detection cycle ends. Within this 80ms delay, the port can be discharged below 4V before detection starts (see Figure 8).

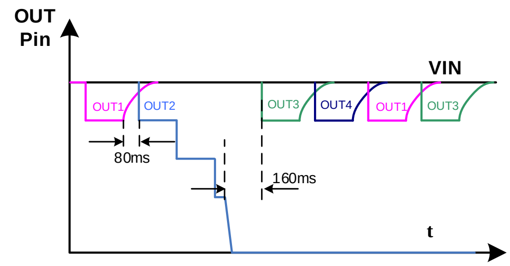


**Figure 8: PD Plug into Port 2**

If one of the ports has a PD load and the port starts up, then the other ports repeat the detection cycle, from channel one to channel four. After one channel shuts down, it returns to its place in the queue (see Figure 9).

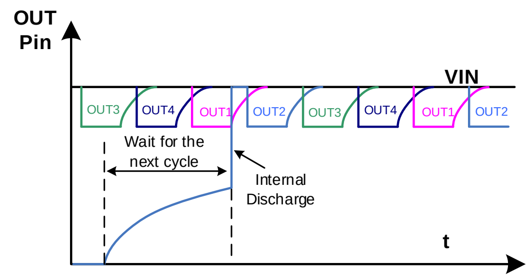


**Figure 9: PD Plug Out from Port 2**

### Over-Current Protection (OCP)

When the port is powered up, the MP3924 controls the inrush current. As a result, the output port voltage ramps up smoothly until the connected PD capacitor charges up to the power source voltage. In this scenario, the GATE pin voltage is controlled to limit the input current ($I_{IN}$) below 106.25mV / $R_{SENSE}$.

If the PD capacitor value is too large or the output port is shorted, the inrush current lasts for a set time ($t_{INRUSH}$). After $t_{INRUSH}$, the port output power turns off. $t_{INRUSH}$ can be configured via the TINRUSH bit.

If 106.25mV / $R_{SENSE}$ exceeds $I_{CUT}$ during the inrush period, the $I_{CUT}$ timer ($t_{ICUT}$) begins counting. After $t_{ICUT}$, the output turns off. It is recommended for $R_{SENSE}$ to be 0.25Ω for all applications. If one port shuts down due to the start-up inrush current, then the STFx bits are set to indicate a start failure event.

After start-up, the PGx bits are set to high to indicate the port's output power status. If the load current exceeds $V_{CUT}$ / $R_{SENSE}$ ($V_{CUT}$ is


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controlled by the ICUTx bits), then a timer ($t_{ICUT}$) is enabled to record the OC condition.

8The port turns once this timer finishes counting. If the load current exceeds $V_{CUT}$ and triggers $V_{ILIM}$ / $R_{SENSE}$, then the GATE pin regulates the load at the current limit level. An additional timer ($t_{ILIM}$) is enabled to record the current limit event. $t_{ILIM}$ is counted even if the MP3924 is in current foldback mode.

$V_{CUT}$ detects the OC threshold, which is below the $V_{ILIM}$ threshold. $t_{ICUT}$ starts counting when the OC condition begins. If the load current drops below $V_{CUT}$, $t_{ICUT}$ does not reset immediately. Instead, $t_{ICUT}$ counts down at a rate that is 1/16 of how quickly is counts up. The $t_{ICUT}$ timer records for a total of 60ms for every 0.96s + 0.06s detection window.

If the port shuts down due to an OC condition, the port can be re-enabled only after $t_{ICUT}$ counts down to 0. This logic can detect a short or repeated OC condition. The logic also protects the external MOSFET from overheating. $t_{ILIM}$ and $t_{NRUSH}$ operate with the same logic.

The over-current protection (OCP) timer does not reset even if the device shuts down or the EN bit turns off. This means that the port cannot be re-enabled until the timer counts to 0 again. In manual mode, the host should read the Read and Clear register address continuously until the register is reset to 0. Then the port is re-enabled. In automatic mode, the MP3924 automatically restarts after the timer counts down to 0.

When $t_{ICUT}$ is completed, the related OUT port shuts down (see Figure 10). At the same time, the POWER_STATUS and OVER_LOAD_STATUS registers are set to indicate the power condition.

The default $V_{CUT}$ is different for Classes 0~3 than Class 4 and Class 5. $V_{CUT}$ can also be configured. $V_{ILIM}$ has three fixed values for Classes 0~3, Class 4, and Class 5.

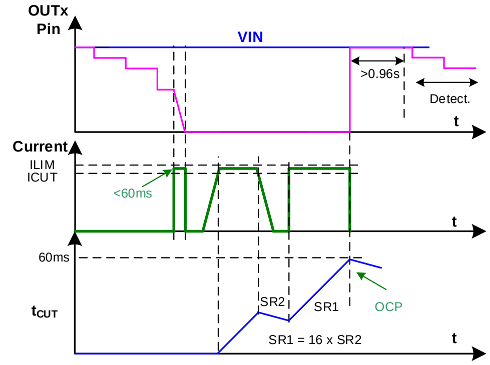


**Figure 10: $I_{CUT}$ Over-Current Detection**

The GATE pin typically has a 43µA source current capability for current limit regulation, which means that the output voltage maximum start-up slew rate can be controlled by $I_{GATE}$ / $C_{GD}$ ($C_{GD}$ is the capacitance between the external MOSFET's gate and drain). When the GATE pin's voltage is pulled down to 1V by a weak discharge current, the voltage is latched to 0V with a strong pull-down current until the next start-up event. If the load current ramps up quickly and triggers the $V_{SCP}$ fast-off voltage threshold, the MP3924 shuts down port power quickly to protect the MOSFET. The load at the current limit level is regulated until the timer ($t_{ILIM}$) counts down.

The MP3924 shuts down the corresponding output port if an $I_{CUT}$ or $I_{LIM}$ event occurs, and the related fault bits are set. The following registers are also affected:

- The PGx and PENx bits in the POWER_STATUS register are cleared.
- The DET/CLS_RESULTx register and PORTx_VOLTAGE/CURRENT register are cleared.
- The PGCx and PECx bits in the POWER_STATUS_CHANGE register are set.
- The ICUTx and ILIMx bits are cleared.

### Current Foldback

During an overload or short-circuit condition, the MP3924 limits the current through the sense resistor by controlling the external MOSFET. The MOSFET loses power due to the rising drain voltage. To reduce power loss and protect the MOSFET, reduce the current limit when the drain voltage rises.


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For Class 0~3 applications, the current limit drops when the OUTx pin's voltage ($V_{OUTx}$) exceeds 32V. Meanwhile, the current limit threshold linearly falls to 40mV when $V_{OUTx}$ rises to 46V. For Class 4 and Class 5 applications, the current limit drops when $V_{OUTx}$ exceeds 18V. The current limit eventually falls to 40mV when $V_{OUTx}$ rises to 46V.

Figure 11 shows current limit foldback. The current limit is calculated using a 0.25Ω sense resistor.

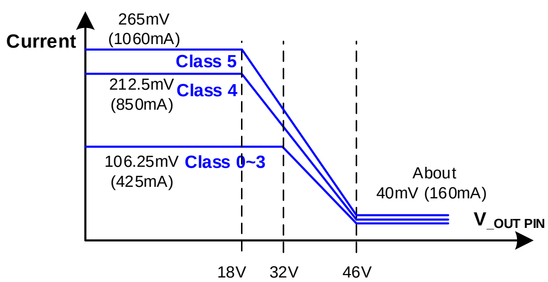


**Figure 11: Current Limit Foldback**

### Automatic Maximum Power Protection

The MP3924 has the classification ability to allocate power to each port based on IEEE802.3at. The MP3924 can monitor the total loading power and automatically shut down the lower priority port if the total load power exceeds the expected power rating. Set the PMAXEN bit high to enable this function. Then the MP3924 compares the total load power with the power reference set by the PMAX pin.

If the total load exceeds the configured power level for longer than the overload time ($t_{PMAX}$), the MP3924 shuts down the lowest priority port among the powered ports. If the total load power exceeds 50% of the configured limit, the lowest priority port shuts down after a 2ms delay. Port priority is arranged via the PRTYx bits. By default, port 1 has the highest priority and port 4 has the lowest priority.

If the AUTO pin is high after start-up or after the device resets, then the PMAXEN bit is set to 1 by default. If the AUTO pin is low after start-up or after the device resets, then the PMAXEN bit is set to 0 by default. Maximum power protection is enabled when the PMAXEN bit is high. If the total load power is below the configured PMAX level, the maximum power on each port does not exceed the classified current limit. The PMAX cooling time before recovery is 16 times the value set by the TPMAX register (see Figure 12).

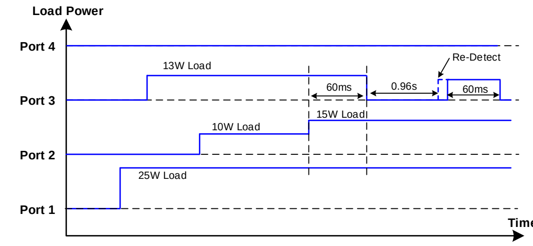


**Figure 12: PMAX Power Management at 50W**

### DC Disconnect Detection

The MP3924 monitors the load current after the port is powered up. If the port load current drops below 7.5mA (assuming $R_{SENSE}$ = 0.25Ω) for longer than 350ms, then the MP3924 considers the load disconnected and turns off the port's output power. The MP3924 considers the load connected to the port if the current exceeds 7.5mA (assuming $R_{SENSE}$ = 0.25Ω), or exceeds the current load from the PSE output, for longer than 43.75ms in every 393.75ms window.

The DC disconnect detection function is enabled by default after the device starts up in automatic mode. If the AUTO pin is low during start-up or after the IC resets, the DC disconnect detection function is disabled by default. Each port can enable/disable the DC disconnect detection function via the DISENx bits. After a shut down due to DC disconnect detection, one DCDISx bit is set to indicate the status. The following registers are also affected:

- The PGx and PENx bits in the POWER_STATUS register are cleared.
- The DET/CLS_RESULTx register and PORTx_VOLTAGE/CURRENT register are cleared.
- The PGCx and PECx bits in the POWER_STATUS_CHANGE register are set.
- the ICUTx and ILIMx bits are cleared.

### Interrupt Control

The MP3924 features two interrupt pins that can be used for different priority interrupt sources. The priority can be configured via the Interrupt Priority register. INT2 responds to the


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selected interrupt sources, while INT1 responds to all interrupt sources. By default, INT2 responds to $V_{IN}$ power failures and OC events.

The MP3924 pulls the INT1 and INT2 pins low if a fault condition occurs in the Interrupt Priority register while the interrupt is not masked. The interrupt signal is asserted to notify the host controller that certain fault conditions have been detected. If the interrupt source is masked, the interrupt event bits are set, but the INT1 and INT2 pins do not respond to the fault event.

INT1 and INT2 go low if a fault occurs. If a second fault occurs before the host resets the interrupt signal, the MP3924 keeps the INT1 and INT2 pins low until the host controller resets the fault condition (see Figure 13).

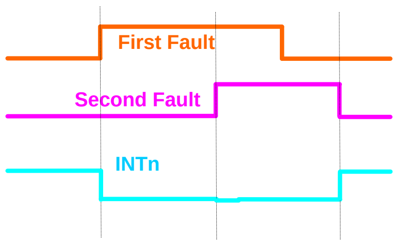


**Figure 13: Interrupt Sequence**

After the host controller receives the interrupt signal, it can check the status register to diagnose the issues. The host can read the read and clear address to reset the interrupt event register, as well as the INT1 and INT2 pins. If the host controller reads the status register through the read-only address, neither the interrupt event register nor the INT1 and INT2 pins are reset. For more details, see the Register Map section on page 29.

The INT1 and INT2 pins can be reset by the CLRAINT bit or the interrupt disable bit (INTEN) (see Figure 14).

The INTx pin should be triggered at the edge of the fault event. If two fault events occur simultaneously, then the INTx pin does not reset until all fault events are cleared.

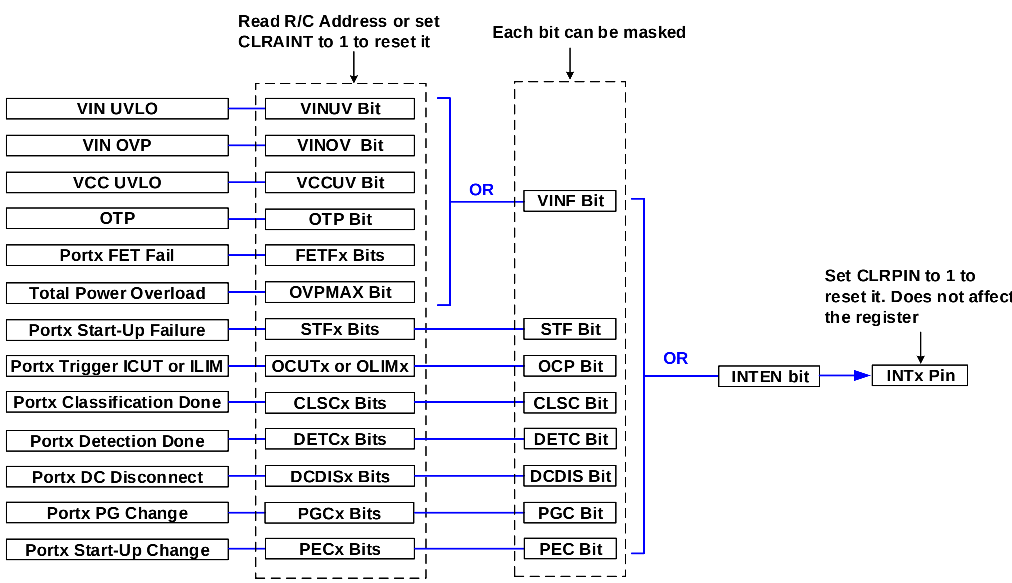


**Figure 14: Interrupt Logic Diagram**

## Legacy Detection

The DET/CLS_RESULTx registers return to 010 (if $C_{DET}$ > 5µF) if the cable is connected to a legacy PD with a high input capacitor. The LEGENx bits enable legacy detection mode. By default, the LEGENx bits are set to 00 to disable legacy detection. Table 1 on page 25 lists the detection parameters. Legacy detection returns the results of the LEGACY_DETECT_RESULTx registers.

The MP3924 starts legacy detection after the PD input voltage is discharged below 2.4V. If


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the PD input voltage is high, a 250ms discharge timer works with a 100kΩ load between the OUTx pin and VIN. If the PD input exceeds 2.4V, a secondary 500ms discharge timer begins. If the PD input voltage does not fall below 2.4V after the two discharge times, then the MP3924 is set to 0010 in the LEGACY_DETECT_RESULTx registers.

After legacy detection starts, a fixed current is charged to the PD input. The voltage difference between two points is used to calculate the effective capacitance.

If the capacitance is too great and the measured voltage difference is below 0.5V, then the MP3924 reports 0110. If the capacitance is too low and the measured voltage reaches 18.5V, then the MP3924 reports 0100 or 0101. All of these results are invalid in legacy detection.

**Table 1: Legacy Detection Measurements**

| Parameter | Value | Units |
|---|---|---|
| Minimum measurable capacitance | 5 | µF |
| Maximum measurable capacitance | 100 | µF |
| Capacitance test charge current | 500 | µA |
| Nominal measurement time | 150 | ms |
| Maximum voltage before start measurement | 2.4 | V |
| Duration of first port discharge period | 250 | ms |
| Duration of second port discharge period | 500 | ms |
| Maximum voltage during measurement | 18.5 | V |

If legacy detection is enabled and a legacy device is detected in automatic mode, then the detection status is reported in the LEGACY_DETECT_RESULTx registers. However, the device does not start up immediately, as it requires a host command through the $I^2C$.

If LEGENx is set to 01 or 10 in automatic or semi-automatic mode, there is initially one standard detecting cycle. If the standard resistance detection result is valid, then the MP3924 does not continue legacy detection and the classification process begins instead. If the standard resistance detection result is not valid and legacy detection is valid, the MP3924 does not start the classification process, even if the CLSENx bit is set. In this scenario, a software command is required to trigger the classification process.

If the following conditions are met, then PON automatically powers the port (even if the classification result does not match, or there is an OC condition):

- PON is enabled by the software after the legacy detection is determined to be valid.
- The MP3924 is in automatic or semi-automatic mode.

If the LEGENx bit is enabled in automatic or semi-automatic mode, the legacy detection result repeats and refreshes the LEGACY_DETECT_RESULTx registers. This process repeats until the LEGENx bit is disabled. In manual mode, legacy detection occurs once, then the LEGENx bits resets automatically. It is recommended to use manual mode.

### Operation Modes

The MP3924 provides four operation modes to flexibly control PoE communication and start-up: automatic mode, semi-automatic mode, manual mode, and shutdown mode. The AUTO pin and the MODEx bits set the different modes, which are described below in greater detail.

#### *Automatic Mode*

In automatic mode, the MP3924 automatically controls and responds to all detection, classification, and start-up functions. The MP3924 handles these processes for each port independently and without external $I^2C$ control. Float the AUTO pin to force the MP3924 to work in automatic mode.

In automatic mode, the MODEx bits are set to 11 when device turns on. The AUTO pin status is only read once when the device turns on or the MP3924 is reset. If a master is connected to the MP3924 via the $I^2C$, then the master can change the MODEx bits to change the operation mode. If there is no valid PD on the port in automatic mode, then the MP3924


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repeats the detection cycle until a valid PD is connected.

If the MP3924 runs in automatic mode after start-up or reset, the DETENx and CLSENx bits are set high based on the AUTO pin. If a port is set to automatic mode via the I²C, the DETENx and CLSENx bits do not change.

### *Semi-Automatic Mode*

In semi-automatic mode, the MP3924 automatically detects and classifies the connected PD. However, the port does not start up until an I²C command is issued. Set the MODEx bits to 10 to force the MP3924 to operate in semi-automatic mode.

When the port is set to semi-automatic mode, the DETENx and CLSENx bits to not change. If the DETENx and CLSENx bits are high in semi-automatic mode, the port repeats the detection (and classification if the PD detection result is valid) continuously. However, the port does not start up until an I²C command is issued. If the detection and classification are valid, the port power can be turned on by a PONx bit. If the port is powered off in semiautomatic mode, the DETENx and CLSENx bits are reset to 0.

If the detection is valid and the port does not turn on within 400ms in automatic or semi-automatic mode, then the port initiates a new detection sequence. If the final detection and classification sequences are determined to be invalid before the start-up command is received, the device fails to turn on. At the same time, the STFx bit is set and the MP3924 resets the command. If the detection and classification sequences are valid but a start-up command is not issued after 400ms, then the STFx bit is set.

### *Manual Mode*

In manual mode, all functions are controlled via the I²C interface. Manual mode is recommended for system diagnostics. Set the MODEx bits to 01 to force the ports to operate in manual mode.

In manual mode, the DETENx and CLSENx bits are set to 0. Set these bits to 1 to enable one-time detection or classification. These bits reset to 0 automatically.

The PONx bits power the port in manual mode. The port turns on any time the PONx bit is set. If the DETENx, CLSENx, and PONx bits are set simultaneously, then the MP3924 executes a detection cycle first. If the DETENx and CLSENx bits are set after the port starts up, the MPM3924 ignores the DETENx and CLSENx commands. The RDETx and RCLSx bits follow the same logic.

If a PONx command is received while the device recovers from a protection, then the MP3924 does not turn on and the failure is reported to the STFx bit.

### *Shutdown Mode*

In shutdown mode, all detection, classification, and port power output functions are off. To force the MP3924 to operate in shutdown mode, pull the AUTO pin to DGND before the device starts up or resets. Set the MODEx bits to 00 to set a port to shutdown mode.

Once a port is in shutdown mode, the power is turned off and the corresponding port event/status registers are cleared, except for the PECx and PGCx bits. The I²C interface still operates in shutdown mode, but the ports do not respond to any detection, classification, or port start-up commands.

In certain AUTO pin configurations, the MODE bits are set to 00 or 11 after start-up (or after a reset). After start-up, all ports can switch between the four modes. The registers and port states are not changed by these bits unless shutdown mode is selected.

## 9-Bit ADC

The MP3924 integrates a 9-bit analog-to-digital converter (ADC) to continuously measure the input voltage, output voltage, load current, and junction temperature. The ADC also measures PMAX once following start-up, or if the device is reset. When any ADC information is required, the host controller can read the corresponding data registers. ADC conversion only works when the port is enabled and if there is no data update for the corresponding port when the port is shut down. The register cannot be updated while it is read, even if ADC conversion is complete for that segment of data.

## I²C Interface

The MP3924 features an I²C interface. The 7-bit device address is defined as 010 xxxx, where


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the lower 4 bits are set by A3~A0 pins. When the master sends an 8-bit address value, the 7-bit $I^2C$ address should be followed by a 0 or 1 to indicate a write or read operation, respectively. The MP3924 works as a slave and supports standard mode (100kbps) and fast mode (400kbps) communication.

The $I^2C$ is a two-wire, bidirectional serial interface consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are idle. When connecting to the line, a master device generates the SCL signal and device address, then arranges the communication sequence. To support communication with an isolated host controller, the data interface is split into two ports: SDAI and SDAO. For non-isolated applications, SDAI and SDAO can be connected to on another.

The MP3924 includes one alert response address for MP3924 devices that are connected through the address 0x0C (000 1100). If the bus master controller sends the alert response address when INT1 is low during an interrupt event, then the MP3924 with the interrupt request responds with its device address on the SDAI line before releasing the INT1 line.

If two MP3924 devices respond simultaneously, then the device with the lower address succeeds in transmitting to the master via the SDAI and SDAO lines. The device that attempts to send a 1 but detects a 0 on the SDAI line does not respond. After this, the MP3924 with the higher address finishes responding. Its INT1 pin remains low until it receives the host controller’s next alert response address read.

The MP3924 has one global address: 0110000. This means that the host controller can write to multiple MP3924 devices through the address 0x60 (01100000). If the host controller reads multiple MP3924 through the address 0x61 (01100001), it works as an alert response address.

While reading or writing, the MP3924 register address is determined by the host command. After each read/write data byte operation, the register address automatically increases by 1 byte, and the host can read/write the next byte without the new address command information. If the system works with several host controllers, the address set by host 1 can respond to host 2, if host 1 does not have data to read/write in that address. If different registers must be read or written, one address information is required to set the correct register address.

### *$I^2C$ Data Validity*

One clock pulse is generated for each transferred data bit. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCL line is low (see Figure 15).

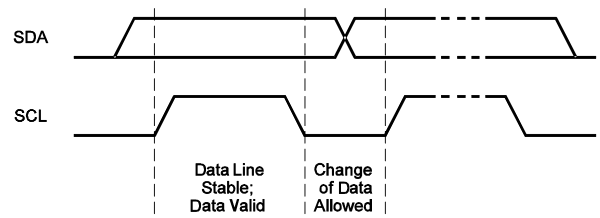


**Figure 15: Bit Transfer on the $I^2C$ Bus**

The start (S) and stop (P) commands are signaled by the master device, which signifies the beginning and the end of the $I^2C$ transfer. A start command is defined as the SDA signal transitioning from high to low while the SCL signal is high. A stop command is defined as the SDA signal transitioning from low to high while the SCL signal is high (see Figure 16).

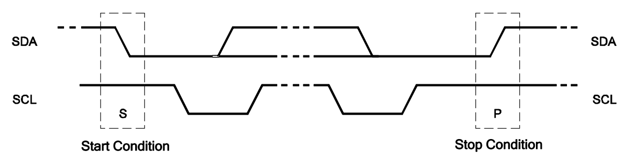


**Figure 16: Start and Stop Conditions**

Start and stop commands are always generated by the master. The bus is considered to be busy after a start command. The bus is considered to be free again a minimum of 4.7μs after the stop condition. The bus remains busy if a repeated start (Sr) command is generated instead of a stop command. The start (S) and repeated start (Sr) commands are functionally identical.

### *$I^2C$ Transfer Data*

Every byte put on the SDA line must be 8 bits long. Each byte has to be followed by an acknowledge (ACK) bit. The acknowledge clock pulse is generated by the master. The transmitter releases the SDA line (high) during


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the acknowledgement clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains low during the high period of this clock pulse.

Figure 17 shows the data transfer sequence. After the start condition (S), a slave address is sent. This address is 7 bits long followed by an 8th data direction bit (R/W). A 0 indicates a transmission (write), while a 1 indicates a request for data (read). A data transfer is always terminated by a stop condition (P) generated by the master. However, if a master must communicate on the bus, it can generate a repeated start condition (Sr) and address another slave without first generating a stop condition.

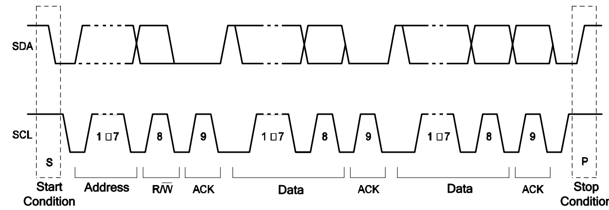


**Figure 17: Complete Data Transfer**

The MP3924 includes a full I²C slave controller. The I²C slave fully complies with I²C specification requirements. It requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. The MP3924 acknowledges that it has received each byte by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP3924. The MP3924 performs an update on the falling edge of the LSB byte.

Figure 18 shows an I²C write example.

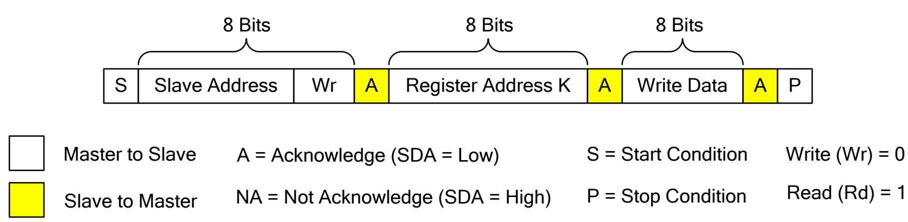


**Figure 18: I²C Write Example**

Figure 19 shows an I²C write example.

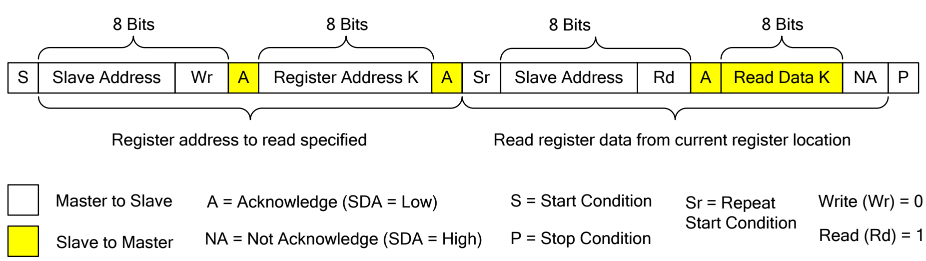


**Figure 19: I²C Read Example**

Figure 20 shows that the 0x00C address has a different read command from the standard I²C.

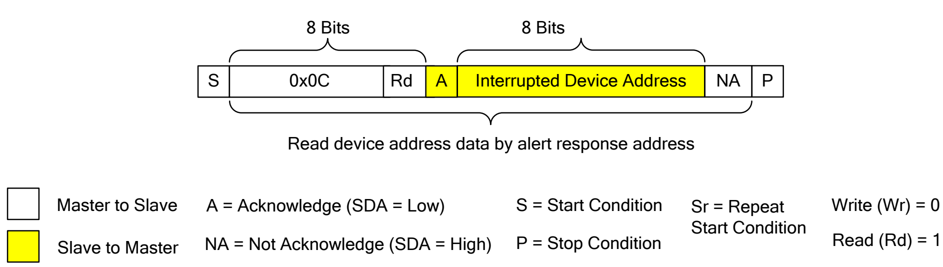


**Figure 20: 0x0C Read Example**


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### Watchdog

The MP3924 implements a watchdog to monitor the SCL line for $I^2C$ activity. If there is no transition on the SCL line for about 2.5s during $I^2C$ communication, then the $I^2C$ port and all power output ports shut down. The WDS bit is set to 1 to indicate the error condition. WDS must be reset before any port can be re-enabled. After watchdog protection is triggered, the port shuts down until the host re-enables the ENx bits.

By default, the watchdog is off after start-up. To enable the watchdog function, set the WDEN bit to 1.

### Over-Temperature Protection (OTP)

Over-temperature protection (OTP) is implemented to prevent the chip from thermal runaway. When the junction temperature exceeds its upper threshold, the MP3924 shuts down all ports (the $I^2C$ and registers still work). Once the temperature drops below its recovery threshold, the ports are enabled again with a new detection cycle. The OTP bit is set to 1 after OTP recovery.


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# REGISTER DESCRIPTION

## Register Map

| Addr | Register | Type | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Interrupt Register** | | | | | | | | | | | |
| 00h | INTERRUPT | R | VINF | STF | OCP | CLSC | DETC | DCDIS | PGC | PEC | 1000 0000 |
| 01h | INTERRUPT_MASK | R/W | VINF_M | STF_M | OCP_M | CLSC_M | DETC_M | DCDIS_M | PGC_M | PEC_M | 1A A0 0A00 (11) |
| 02h | INTERRUPT_PRIORITY | R/W | VINF_P | STF_P | OCP_P | CLSC_P | DETC_P | DCDIS_P | PGC_P | PEC_P | 1010 0000 |
| **Configuration Register** | | | | | | | | | | | |
| 03h | MODE_SETTING | R/W | MODE4 | | MODE3 | | MODE2 | | MODE1 | | AAAA AAAA (11) |
| 04h | MIDSPAN_SETTING | R/W | - | - | - | - | MID4 | MID3 | MID2 | MID1 | 0000 MMMM (11) |
| 05h | PORT_ENABLE | R/W | - | - | - | ENAL | EN4 | EN3 | EN2 | EN1 | 0001 1111 |
| 06h | DET/CLS_ENABLE | R/W | CLSEN4 | LCSEN3 | CLSEN2 | CLSEN1 | DETEN4 | DETEN3 | DETEN2 | DETEN1 | AAAA AAAA (11) |
| 07h | DISCONNECT_ENABLE | R/W | - | - | - | - | DISEN4 | DISEN3 | DISEN2 | DISEN1 | 0000 AAAA (11) |
| 08h | FAULT_TIMER | R/W | TPMAX | | TINRUSH | | TILIM | | TCUT | | 1010 1110 |
| 09h | RESERVED | - | - | - | - | - | - | - | - | - | 0000 0000 |
| 0Ah | RESERVED | - | | | - | - | - | - | - | - | 0000 0000 |
| 0Bh | FOLDBACK_ILIM | R/W | - | - | - | - | - | - | - | FBLIMT | 0000 0001 |
| 0Ch | 2-EVENT_CLASS_5_ENABLE | R/W | CLS5_EN4 | CLS5_EN3 | CLS5_EN2 | CLS5_EN1 | 2EVNT EN4 | 2EVNTEN3 | 2EVNT EN2 | 2EVNT EN1 | CCCC AAAA (11) |
| 0Dh | PMAX_SHUTDOWN_PRIORITY | R/W | PRTY4 | | PRTY3 | | PRTY3 | | PRTY1 | | 1110 0100 |
| 0Eh | INTERRUPT_ENABLE | R/W | - | - | - | - | - | CLRPIN | CLRAINT | INTEN | 0000 0001 |
| 0Fh | GENERAL_CONTROL | R/W | - | - | - | - | - | PMAXEN | ADCEN | WDEN | 0000 0A 10 (11) |
| **Manual Control Register** | | | | | | | | | | | |
| 10h | DET/CLS_TRIGGER | R/W | RCLS4 | RCLS3 | RCLS2 | RCLS1 | RDET4 | RDET3 | RDET2 | RDET1 | 0000 0000 |
| 11h | POWER_ON/OFF_TRIGGER | R/W | POFF4 | POFF3 | POFF2 | POFF1 | PON4 | PON3 | PON2 | PON1 | 0000 0000 |
| 12h | LEGACY_ENABLE | R/W | LEGEN4 | | LEGEN3 | | LEGEN2 | | LEGEN1 | | 0000 0000 |
| **Current Limit Configuration Register** | | | | | | | | | | | |
| 13h | ICUT1_THRESHOLD | R/W | - | - | - | - | - | ICUT1 | | | 0000 0000 |
| 14h | ICUT2_THRESHOLD | R/W | - | - | - | - | - | ICUT2 | | | 0000 0000 |
| 15h | ICUT3_THRESHOLD | R/W | - | - | - | - | - | ICUT3 | | | 0000 0000 |
| 16h | ICUT4_THRESHOLD | R/W | - | - | - | - | - | ICUT4 | | | 0000 0000 |
| 17h | ILIM1_THRESHOLD | R/W | - | - | - | - | - | - | - | ILIM1 | 0000 0000 |
| 18h | ILIM2_THRESHOLD | R/W | - | - | - | - | - | - | - | ILIM2 | 0000 0000 |
| 19h | ILIM3_THRESHOLD | R/W | - | - | - | - | - | - | - | ILIM3 | 0000 0000 |
| 1Ah | ILIM4_THRESHOLD | R/W | - | - | - | - | - | - | - | ILIM4 | 0000 0000 |
| **Status Register** | | | | | | | | | | | |
| 20h | POWER_SOURCE_STATUS1 | R | FETF4 | FETF3 | FETF2 | FETF1 | VCCUV | OTP | VINOV | VINUV | 0000 1001 |
| 21h | | R/C (12) | | | | | | | | | |
| 22h | POWER_SOURCE_STATUS2 | R | - | - | - | - | - | - | VINOK | OVP MAX | 0000 0000 |
| 23h | | R/C (12) | | | | | | | | | |
| 24h | DET/CLS_COMPLETE_STATUS | R | CLSC4 | CLSC3 | CLSC2 | CLSC1 | DETC4 | DETC3 | DETC2 | DETC1 | 0000 0000 |
| 25h | | R/C (12) | | | | | | | | | |
| 26h | DET/CLS_RESULT_1 | R | CLSR1 | | | | 2EVNT C1 | DETR1 | | | 0000 0000 |
| 27h | DET/CLS_RESULT_2 | R | CLSR2 | | | | 2EVNT C2 | DETR2 | | | 0000 0000 |
| 28h | DET/CLS_RESULT_3 | R | CLSR3 | | | | 2EVNT C3 | DETR3 | | | 0000 0000 |
| 29h | DET/CLS_RESULT_4 | R | CLSR4 | | | | 2EVNT C4 | DETR4 | | | 0000 0000 |
| 2Ah | POWER_STATUS | R | PG4 | PG3 | PG2 | PG1 | PEN4 | PEN3 | PEN2 | PEN1 | 0000 0000 |
| 2Bh | POWER_STATUS_CHANGE | R | PGC4 | PGC3 | PGC2 | PGC1 | PEC4 | PEC3 | PEC2 | PEC1 | 0000 0000 |
| 2Ch | | R/C (12) | | | | | | | | | |


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| Addr | Register | Type | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Reset State |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2Dh | OVER_LOAD_STATUS | R | OCUT4 | OCUT3 | OCUT2 | OCUT1 | STF4 | STF3 | STF2 | STF1 | 0000 0000 |
| 2Eh | | R/C (12) | | | | | | | | | |
| 2Fh | CURRENT_LIMIT_STATUS | R | - | - | - | - | OLIM4 | OLIM3 | OLIM2 | OLIM1 | 0000 0000 |
| 30h | | R/C (12) | | | | | | | | | |
| 31h | DISCONNECT_STATUS | R | - | - | - | - | DCDIS4 | DCDIS3 | DCDIS2 | DCDIS1 | 0000 0000 |
| 32h | | R/C (12) | | | | | | | | | |
| 33h | WATCHDOG_STATUS | R | - | - | - | - | - | - | - | WDS | 0000 0000 |
| 34h | PIN_STATUS | R | - | - | - | AUTO | A3 | A2 | A1 | A0 | 000A DDDD (11) |
| 35h | LEGACY_DETECT_RESULT1 | R | LEGDET2 | | | | LEGDET1 | | | | 0000 0000 |
| 36h | LEGACY_DETECT_RESULT2 | R | LEGDET4 | | | | LEGDET3 | | | | 0000 0000 |
| **ADC Results Register** | | | | | | | | | | | |
| 40h | PORT_1_CURRENT | R | - | - | - | - | - | - | - | Bit [0] | 0000 0000 |
| 41h | | R | Bit[8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | 0000 0000 |
| 42h | OUT1_PIN_VOLTAGE | R | - | - | - | - | - | - | - | Bit [0] | 0000 0000 |
| 43h | | R | Bit[8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | 0000 0000 |
| 44h | PORT_2_CURRENT | R | - | - | - | - | - | - | - | Bit [0] | 0000 0000 |
| 45h | | R | Bit[8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | 0000 0000 |
| 46h | OUT2_PIN_VOLTAGE | R | - | - | - | - | - | - | - | Bit [0] | 0000 0000 |
| 47h | | R | Bit[8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | 0000 0000 |
| 48h | PORT_3_CURRENT | R | - | - | - | - | - | - | - | Bit [0] | 0000 0000 |
| 49h | | R | Bit[8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | 0000 0000 |
| 4Ah | OUT3_PIN_VOLTAGE | R | - | - | - | - | - | - | - | Bit [0] | 0000 0000 |
| 4Bh | | R | Bit [8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | 0000 0000 |
| 4Ch | PORT_4_CURRENT | R | - | - | - | - | - | - | - | Bit [0] | 0000 0000 |
| 4Dh | | R | Bit [8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | 0000 0000 |
| 4Eh | OUT4_PIN_VOLTAGE | R | - | - | - | - | - | - | - | Bit [0] | 0000 0000 |
| 4Fh | | R | Bit [8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | 0000 0000 |
| 50h | INPUT_VOLTAGE | R | - | - | - | - | - | - | - | Bit [0] | 0000 0000 |
| 51h | | R | Bit [8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | 0000 0000 |
| 52h | JUNCTION_TEMPERATURE | R | - | - | - | - | - | - | - | Bit [0] | 0000 0000 |
| 53h | | R | Bit [8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | 0000 0000 |
| 54h | PMAX_POWER_SETTING | R/W | - | - | - | - | - | - | - | Bit [0] | 0000 000P |
| 55h | | R/W | Bit [8] | Bit [7] | Bit [6] | Bit [5] | Bit [4] | Bit [3] | Bit [2] | Bit [1] | PPPP PPPP (11) |
| 60h | DIE_ID | R | FAB | MAJOR_REV | MINOR_REV | VENDOR_ID | 0000 0000 | - | - | - | - |

**Notes:**

11) "A" represents the AUTO pin's status during start-up. "M" represents the MID pin's status during start-up. "C" represents CLS5 pin's status during start-up. "D" represents the A3~A0 address pin statuses during start-up. "P" represents the PMAX pin setting ADC results during start-up.
12) R/C is read and clear address. Reading R/C clears the bit status after reading is complete.


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# INTERRUPT REGISTERS

## INTERRUPT (00h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | VINF | 1 | Interrupt signal for VIN power failure. If this bit is set to 1, one of the following scenarios has occurred:<br>• The power on VIN is below 29.5V<br>• VIN over-voltage protection (OVP)<br>• VCC is under the under-voltage lockout (UVLO) threshold<br>• Thermal shutdown<br>• A power MOSFET failure<br>• A PMAX event |
| D[6] | STF | 0 | Interrupt signal for a start-up failure. If this bit is set to 1, at least one of the ports has experienced a start-up failure, or if a port shuts down due to the start-up inrush current. |
| D[5] | OCP | 0 | Interrupt signal for over-current (OC) conditions. If this bit is set to 1, at least one of the ports has met the $I_{LIMT}$ current limit timer or the $I_{CUT}$ OC timeout condition. |
| D[4] | CLSC | 0 | Interrupt signal for classification completion. This bit is set to 1 if at least one port has completed its classification process. |
| D[3] | DETC | 0 | Interrupt signal for detection completion. This bit is set to 1 if at least one port has completed its detection process. |
| D[2] | DCDIS | 0 | Interrupt signal for a disconnected DC load. This bit is set to 1 if at least one port has had its DC load disconnected (load < 7.5mA). |
| D[1] | PGC | 0 | Interrupt signal for power good (PG) status change. This bit is set to 1 if at least one port has a new PG status. |
| D[0] | PEC | 0 | Interrupt signal for power enable status change. This bit is set to 1 if at least one port has changed its enable or disable status. |

Read the register address with an R/C byte, or write 1 to CLRAIN to reset the corresponding bit. The IN1 and INT2 pins go low to report if an interrupt bit is set to 1. These pins do not go low if the interrupt signal is masked.

## INTERRUPT_MASK (01h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | VINF_M | 1 | Masks the interrupt signal for $V_{IN}$ power failures. Set this bit to 0 to disable the interrupt function. |
| D[6] | STF_M | A | Masks the interrupt signal for start-up failures. Set this bit to 0 to disable the interrupt function. |
| D[5] | OCP_M | A | Masks the interrupt signal for over-current (OC) conditions. Set this bit to 0 to disable the interrupt function. |
| D[4] | CLSC_M | 0 | Masks the interrupt signal for classification completion. Set this bit to 0 to disable the interrupt function. |
| D[3] | DETC_M | 0 | Masks the interrupt signal for detection completion. Set this bit to 0 to disable the interrupt function. |
| D[2] | DCDIS_M | A | Masks the interrupt signal for DC load disconnection. Set this bit to 0 to disable the interrupt function. |
| D[1] | PGC_M | 0 | Masks the interrupt signal for power good (PG) status change interrupt. Set this bit to 0 to disable the interrupt function. |


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| | | | |
|---|---|---|---|
| D[0] | PEC_M | 0 | Masks the interrupt signal for power enable status change interrupt. Set this bit to 0 to disable the interrupt function. |

Write 1 to enable the interrupt function; write 0 to disable the interrupt function. “A” is “1” if the AUTO pin is set high during start-up or a reset. “A” is “0” if the AUTO pin is set low.

These bits only disable the response from the INT1 and INT2 pins. The corresponding interrupt bit always changes. The device cannot mask certain interruptions during start-up or a reset event, including $V_{IN}$ under-voltage lockout (UVLO) and VCC UVLO.

### INTERRUPT PRIORITY (02h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | VINF_P | 1 | Selects if the INT2 pin responds to a $V_{IN}$ power failure interrupt signal. |
| D[6] | STF_P | 0 | Selects if the INT2 pin responds to a start-up failure interrupt signal. |
| D[5] | OCP_P | 1 | Selects if the INT2 pin responds to an over-current (OC) interrupt signal. |
| D[4] | CLSC_P | 0 | Selects if the INT2 pin responds to a classification completion interrupt signal. |
| D[3] | DETC_P | 0 | Selects if the INT2 pin responds to a detection completion interrupt signal. |
| D[2] | DCDIS_P | 0 | Selects if the INT2 pin responds to a DC load disconnect interrupt signal. |
| D[1] | PGC_P | 0 | Selects if the INT2 pin responds to a power good (PG) status change interrupt signal. |
| D[0] | PEC_P | 0 | Selects if the INT2 pin responds to a power enable status change interrupt signal. |

If a bit is set to 1, the INT2 pin pulls low in response to the corresponding interrupt signal. The INT1 pin responds to all interrupt sources, as long as they are not masked. INT2 only responds to the interrupt sources that are not masked.


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# CONFIGURATION AND CONTROL REGISTERS

## OPERATION_MODE_SETTING (03h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:6] | MODE4 | AA | Sets the operation mode for ports 1 through 4. “A” is 1 if the AUTO pin is set high during start-up or a reset. “A” is 0 if the AUTO pin is set low. The status is latched only during start-up or a reset. This can be changed via the I$^2$C.<br>00: Shutdown mode. The port is off, and there is no detection or classification process<br>01: Manual mode. There is no automatic state change<br>10: Semi-automatic mode. The detection and classification processes are automated, but the port does not turn on automatically<br>11: Automatic mode. Start-up, as well as detection and classification processes, are automated |
| D[5:4] | MODE3 | AA | |
| D[3:2] | MODE2 | AA | |
| D[1:0] | MODE1 | AA | |

## MIDSPAN_SETTING (04h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:4] | RESERVED | - | Reserved. |
| D[3] | MID4 | M | Sets the midspan mode for ports 1 through 4. “M” is “1” if the MID pin is high during start-up or a reset. “M” is “0” if MID pin is low. These changes can be configured by writing to the I$^2$C. Set this bit to 1 to enable midspan mode for the corresponding port. |
| D[2] | MID3 | M | |
| D[1] | MID2 | M | |
| D[0] | MID1 | M | |

## PORT_ENABLE (05h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:5] | RESERVED | - | Reserved. |
| D[4] | ENAL | 1 | Enables the MP3924. If this bit is set to 1, all internal IC circuits are enabled. Each port is enabled if the ENAL and ENx bits are set to 1. If ENAL is disabled, the I$^2$C continues to operate, but the ports are shut down. |
| D[3] | EN4 | 1 | Enables ports 1 through 4. These bits can disable the corresponding port, which includes detection and classification processes, resets the port and status registers, and shuts down the port. If a port is already turned off and these bits are set to 0, then there is no change.<br>1: Enabled<br>0: Disabled |
| D[2] | EN3 | 1 | |
| D[1] | EN2 | 1 | |
| D[0] | EN1 | 1 | |

## DET/CLS_ENABLE (06h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | CLSEN4 | A | Enables the classification process for the corresponding port. Set these bits to 1 to enable classification. |
| D[6] | CLSEN3 | A | |
| D[5] | CLSEN2 | A | |
| D[4] | CLSEN1 | A | |
| D[3] | DETEN4 | A | Enables the detection process for the corresponding port. Set these bits to 1 to enable detection. |
| D[2] | DETEN3 | A | |
| D[1] | DETEN2 | A | |
| D[0] | DETEN1 | A | |


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"A" is "1" if the AUTO pin is set high during start-up or a reset. "A" is "0" if the AUTO pin is set low. In automatic and semi-automatic mode, the detection and classification processes are enabled when the bit is set to 1. In manual made, set the bit to 1 for one-time detection or classification. Then the bit is reset to 0.

### DISCONNECT_ENABLE (07h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:4] | RESERVED | - | Reserved. |
| D[3] | DISEN4 | A | Enables DC load disconnection for ports 1 through 4. "A" is 1 if the AUTO pin is set high during start-up or a reset. "A" is 0 if the AUTO pin is set low. If these bits are set to 1, the DC load disconnection function is enabled on the corresponding port. |
| D[2] | DISEN3 | A | |
| D[1] | DISEN2 | A | |
| D[0] | DISEN1 | A | |

### FAULT_TIMER (08h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:6] | TPMAX | 10 | Sets the total power overload timer after start-up.<br>00: 15ms<br>01: 30ms<br>10: 60ms<br>11: 120ms |
| D[5:4] | TINRUSH | 10 | Sets the start-up inrush current timer for all ports.<br>00: 15ms<br>01: 30ms<br>10: 60ms<br>11: 120ms |
| D[3:2] | TILIM | 11 | Sets the current limit trigger timer after start-up for all ports.<br>00: 7.5ms<br>01: 15ms<br>10: 30ms<br>11: 60ms |
| D[1:0] | TCUT | 10 | Set the over-current (OC) timer after start-up for all ports.<br>00: 15ms<br>01: 30ms<br>10: 60ms<br>11: 120ms |

The timer begins counting up after a load triggers the threshold. If the current drops below the threshold, the timer begins counting down at 1/16 of the rising rate. If it times out, the port shuts down. The port cannot be redetected once the timer counts down to 0.

### FOLDBACK_ILIM (0Bh)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:1] | RESERVED | - | Reserved. |
| D[0] | FBLIMT | 1 | Sets the foldback over-current (OC) threshold when the OUTx pin exceeds 46V.<br>0: The foldback current limit is 22mV (88mA if $R_{SENSE}$ = 0.25Ω).<br>1: The foldback current limit is 40mV (160mA $R_{SENSE}$ = 0.25Ω). |


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### 2-EVENT_AND_CLASS_5_ENABLE (0Ch)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | CLS5_EN4 | C | Enables Class 5 classification for all ports. If these bits are set to 1, Class 5 classification is enabled on the corresponding port, and the default current limit can support up to 40W of power. |
| D[6] | CLS5_EN3 | C | |
| D[5] | CLS5_EN2 | C | |
| D[4] | CLS5_EN1 | C | |
| D[3] | 2EVNTEN4 | A | Enables two-event classification for all ports. If these bits are set to 1, two-event classification is enabled when the first classification result on the port is Class 4 or Class 5. |
| D[2] | 2EVNTEN3 | A | |
| D[1] | 2EVNTEN2 | A | |
| D[0] | 2EVNTEN1 | A | |

“A” is “1” if the AUTO pin is set high during start-up or a reset. “A” is “0” if the AUTO pin is set low. “C” is “1” if the CLS5 pin is set high during start-up or a reset. “C” is “0” if the CLS5 pin is set low. The CLS5 pin has a high power level under the IEEE802.3 at classification, but it is not a standard class level that is compatible with IEEE802.3.

### PMAX_SHUTDOWN_PORT_PRIORITY (0Dh)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:6] | PRTY4 | 11 | Sets the shutdown priority for all ports after the PMAX limit is triggered. If the value is the same on several ports, priority is arranged based on the default priority. For example, if both port 1 and port 2 are 00, then port 2 shuts down first.<br>11: The lowest priority port, which shuts down first if the PMAX limit is triggered<br>10: The third level priority port if the PMAX limit is triggered<br>01: The second level priority port if the PMAX limit is triggered<br>00: The highest priority port, which shuts down last if the PMAX limit is triggered |
| D[5:4] | PRTY3 | 10 | |
| D[3:2] | PRTY2 | 01 | |
| D[1:0] | PRTY1 | 00 | |

### INTERRUPT_ENABLE_CONTROL (0Eh)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:3] | RESERVED | - | Reserved. |
| D[2] | CLRPIN | 0 | Controls the reset function for the INT1 and INT2 pins. If this bit is set to 1, resetting the INT1 and INT2 pins does not affect the registers. This bit is automatically set to 0 after the INT1 and INT2 pins are reset. |
| D[1] | CLRAINT | 0 | Controls the reset function for the interrupt source. If this bit is set to 1, all registers and the INT1 and INT2 bit are reset. This bit is automatically set to 0 after the INT1 and INT2 pins are reset. |
| D[0] | INTEN | 1 | Enables the interrupt function. This bit does not affect the event register. If this bit is set to 1, the interrupt function is enabled. |

### GENERAL_ENABLE_CONTROL (0Fh)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:3] | RESERVED | - | Reserved. |
| D[2] | PMAXEN | A | Enables the maximum total load power limit. If this bit = 1, automatic shutdown is triggered when the PMAX pin reaches its maximum input power setting. |
| D[1] | ADCEN | 1 | Enables the ADC. If this bit = 1, the ADC is enabled. |
| D[0] | WDEN | 0 | Enables the $I^2C$ watchdog. If this bit is set to 0, the watchdog is disabled. |

“A” is “1” if the AUTO pin is set high during start-up or a reset. “A” is “0” if the AUTO pin is set low.


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# MANUAL MODE AND LEGACY DETECTION CONTROL REGISTERS

## DET/CLS_TRIGGER (10h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | RCLS4 | 0 | Re-enables the classification function on all ports. If these bits are set to 1, a one-time classification event is enabled on the corresponding port. These bits are reset after classification is complete. |
| D[6] | RCLS3 | 0 | |
| D[5] | RCLS2 | 0 | |
| D[4] | RCLS1 | 0 | |
| D[3] | RDET4 | 0 | Re-enables the detection function on all ports. If these bits are set to 1, a one-time detection event is enabled on the corresponding port. These bits are reset after detection is complete. |
| D[2] | RDET3 | 0 | |
| D[1] | RDET2 | 0 | |
| D[0] | RDET1 | 0 | |

In manual mode, one-time detection or classification occurs after the corresponding bit is set. In semi-automatic or automatic mode, detection and classification are controlled by the DETENx and CLSENx bits. These processes are repeated once they are enabled.

## POWER_ON/OFF_TRIGGER (11h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | POFF4 | 0 | Triggers a shutdown on the corresponding port. If these bits are set to 1, the port powers off. The bit automatically resets afterward. |
| D[6] | POFF3 | 0 | |
| D[5] | POFF2 | 0 | |
| D[4] | POFF1 | 0 | |
| D[3] | PON4 | 0 | Triggers start-up on the corresponding port. If these bits are set to 1, the corresponding port powers on. These bits are reset after start-up is complete. The device performs a detection cycle first if the DETENx and PONx bits are set simultaneously.<br><br>The PONx bits are operational in manual mode. If the port is powered on or in shutdown mode, the port does not respond to these bits.<br><br>The PONx bits are operational in semi-automatic mode. The port responds to these bits if the detection and classification results are valid.<br><br>The PONx bits are only functional during legacy detection if the device is set to automatic mode.<br><br>For all modes, the PONx bits may be cleared by DET/CLS/LEGACY_DET failures, start-up failures, or if the PON signal lasts for 400ms when the port is operational. |
| D[2] | PON3 | 0 | |
| D[1] | PON2 | 0 | |
| D[0] | PON1 | 0 | |

## LEGACY_ENABLE (12h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:6] | LEGEN4 | 00 | Enables legacy detection mode for all ports.<br><br>00: Legacy detection is disabled<br>01: Legacy detection is enabled while standard detection is disabled<br>10: Legacy detection is enabled after standard detection is complete<br>11: Reserved |
| D[5:4] | LEGEN3 | 00 | |
| D[3:2] | LEGEN2 | 00 | |
| D[1:0] | LEGEN1 | 00 | |


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## CURRENT LIMIT CONFIGURATION REGISTER

### ICUT1_THRESHOLD (13h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:3] | RESERVED | - | Reserved. |
| D[2:0] | ICUT1 | 000 | Sets port 1's over-current (OC) threshold. The default value is 000. In automatic mode, the bits are set to 000 for Class 0~3 results, 100 for Class 4 results, and 101 for Class 5 results. In semi-automatic mode or manual mode, the bits do not change unless changes are made via the $I^2C$.<br>000 = 93.75mV (375mA with $R_{SENSE}$ = 0.25Ω)<br>001 = 27.5mV (110mA with $R_{SENSE}$ = 0.25Ω)<br>010 = 47mV (188mA with $R_{SENSE}$ = 0.25Ω)<br>011 = 93.75mV (375mA with $R_{SENSE}$ = 0.25Ω)<br>100 = 162.5mV (650mA with $R_{SENSE}$ = 0.25Ω)<br>101 = 230mV (920mA with $R_{SENSE}$ = 0.25Ω)<br>110 = 125mV (500mA with $R_{SENSE}$ = 0.25Ω)<br>111 = 156.25mV (625mA with $R_{SENSE}$ = 0.25Ω) |

### ICUT2_THRESHOLD (14h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:3] | RESERVED | - | Reserved. |
| D[2:0] | ICUT2 | 000 | Sets port 2's over-current (OC) threshold. The default value is 000. In automatic mode, the bits are set to 000 for Class 0~3 results, 100 for Class 4 results, and 101 for Class 5 results. In semi-automatic mode or manual mode, the bits do not change unless changes are made via the $I^2C$.<br>000 = 93.75mV (375mA with $R_{SENSE}$ = 0.25Ω)<br>001 = 27.5mV (110mA with $R_{SENSE}$ = 0.25Ω)<br>010 = 47mV (188mA with $R_{SENSE}$ = 0.25Ω)<br>011 = 93.75mV (375mA with $R_{SENSE}$ = 0.25Ω)<br>100 = 162.5mV (650mA with $R_{SENSE}$ = 0.25Ω)<br>101 = 230mV (920mA with $R_{SENSE}$ = 0.25Ω)<br>110 = 125mV (500mA with $R_{SENSE}$ = 0.25Ω)<br>111 = 156.25mV (625mA with $R_{SENSE}$ = 0.25Ω) |

### ICUT3_THRESHOLD (15h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:3] | RESERVED | - | Reserved. |
| D[2:0] | ICUT3 | 000 | Sets port 3's over-current (OC) threshold. The default value is 000. In automatic mode, the bits are set to 000 for Class 0~3 results, 100 for Class 4 results, and 101 for Class 5 results. In semi-automatic mode or manual mode, the bits do not change unless changes are made via the $I^2C$.<br>000 = 93.75mV (375mA with $R_{SENSE}$ = 0.25Ω)<br>001 = 27.5mV (110mA with $R_{SENSE}$ = 0.25Ω)<br>010 = 47mV (188mA with $R_{SENSE}$ = 0.25Ω)<br>011 = 93.75mV (375mA with $R_{SENSE}$ = 0.25Ω)<br>100 = 162.5mV (650mA with $R_{SENSE}$ = 0.25Ω)<br>101 = 230mV (920mA with $R_{SENSE}$ = 0.25Ω)<br>110 = 125mV (500mA with $R_{SENSE}$ = 0.25Ω)<br>111 = 156.25mV (625mA with $R_{SENSE}$ = 0.25Ω) |


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### ICUT4_THRESHOLD (16h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:3] | RESERVED | - | Reserved. |
| D[2:0] | ICUT4 | 000 | Sets port 4's over-current (OC) threshold. The default value is 000. In automatic mode, the bits are set to 000 for Class 0~3 results, 100 for Class 4 results, and 101 for Class 5 results. In semi-automatic mode or manual mode, the bits do not change unless changes are made via the $I^2C$.<br>000 = 93.75mV (375mA with $R_{SENSE}$ = 0.25Ω)<br>001 = 27.5mV (110mA with $R_{SENSE}$ = 0.25Ω)<br>010 = 47mV (188mA with $R_{SENSE}$ = 0.25Ω)<br>011 = 93.75mV (375mA with $R_{SENSE}$ = 0.25Ω)<br>100 = 162.5mV (650mA with $R_{SENSE}$ = 0.25Ω)<br>101 = 230mV (920mA with $R_{SENSE}$ = 0.25Ω)<br>110 = 125mV (500mA with $R_{SENSE}$ = 0.25Ω)<br>111 = 156.25mV (625mA with $R_{SENSE}$ = 0.25Ω) |

### ILIM1_THRESHOLD (17h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:1] | RESERVED | - | Reserved. |
| D[0] | ILIM1 | 0 | Sets port 1's over-current (OC) limit. The default value is 0. In automatic mode, the bits are set to 0 for Class 0~3, and set to 1 for Class 4 or Class 5 results. In semi-automatic mode and manual mode, the bits do not change unless changes are made via the $I^2C$.<br>0: 106.25mV (425mA if $R_{SENSE}$ = 0.25Ω)<br>1: 212.5mV. The current limit is 265mV under Class 5 conditions |

### ILIM2_THRESHOLD (18h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:1] | RESERVED | - | Reserved. |
| D[0] | ILIM2 | 0 | Sets port 2's over-current (OC) limit. The default value is 0. In automatic mode, the bits are set to 0 for Class 0~3, and set to 1 for Class 4 or Class 5 results. In semi-automatic mode and manual mode, the bits do not change unless changes are made via the $I^2C$.<br>0: 106.25mV (425mA if $R_{SENSE}$ = 0.25Ω)<br>1: 212.5mV. The current limit is 265mV under Class 5 conditions |

### ILIM3_THRESHOLD (19h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:1] | RESERVED | - | Reserved. |
| D[0] | ILIM3 | 0 | Sets port 3's over-current (OC) limit. The default value is 0. In automatic mode, the bits are set to 0 for Class 0~3, and set to 1 for Class 4 or Class 5 results. In semi-automatic mode and manual mode, the bits do not change unless changes are made via the $I^2C$.<br>0: 106.25mV (425mA if $R_{SENSE}$ = 0.25Ω)<br>1: 212.5mV. The current limit is 265mV under Class 5 conditions |


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### ILIM4_THRESHOLD (1Ah)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:1] | RESERVED | - | Reserved. |
| D[0] | ILIM4 | 0 | Sets port 4's over-current (OC) limit. The default value is 0. In automatic mode, the bits are set to 0 for Class 0~3, and set to 1 for Class 4 or Class 5 results. In semi-automatic mode and manual mode, the bits do not change unless changes are made via the $I^2C$.<br><br>0: 106.25mV (425mA if $R_{SENSE}$ = 0.25Ω)<br>1: 212.5mV. The current limit is 265mV under Class 5 conditions |


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# STATUS REGISTERS

## POWER_SOURCE_STATUS1 (20h and 21h)

(20h) Read-only
(21h) Read and clear

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | FETF4 | 0 | Indicates whether an external power MOSFET failure has occurred. This bit is set to 1 if the external MOSFET on the corresponding port has failed. If this occurs, the current limit cannot be reached, or the OUTx pin is high after start-up. |
| D[6] | FETF3 | 0 | |
| D[5] | FETF2 | 0 | |
| D[4] | FETF1 | 0 | |
| D[3] | VCCUV | 1 | Indicates whether a VCC under-voltage condition has occurred. This bit is set to 1 if VCC has recovered from a shutdown or reset condition. |
| D[2] | OTP | 0 | Indicates whether an over-temperature (OT) condition has occurred. This bit is set to 1 if the junction temperature exceeds 150°C. For more details, see the Over-Temperature Protection (OTP) section on page 28. |
| D[1] | VINOV | 0 | Indicates whether a $V_{IN}$ over-voltage (OV) condition has occurred. This bit is set to 1 if $V_{IN}$ exceeds 65V. |
| D[0] | VINUV | 1 | Indicates whether a $V_{IN}$ under-voltage (UV) condition has occurred. This bit is set to 1 if $V_{IN}$ drops below 29.5V. |

Read and Clear (0x21h) means that the bit is reset after a read operation. If read on 0x20h, the bits are not cleared.

## POWER_SOURCE_STATUS2 (22h and 23h)

(22h) Read-only
(23h) Read and clear

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:2] | RESERVED | - | Reserved. |
| D[1] | VINOK | 0 | Indicates whether the $V_{IN}$ source power is working normally. This bit is set to 1 if $V_{IN}$ exceeds 40V. |
| D[0] | OVPMAX | 0 | Indicates whether a power overload condition has occurred. This bit is set to 1 if the total power load on all ports exceeds the PMAX threshold set by the PMAX pin. |

## DET/CLS_COMPLETE_STATUS (24h and 25h)

(24h) Read-only
(25h) Read and clear

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | CLSC4 | 0 | Indicates whether a port has completed its classification process. These bits are set to 1 if classification has completed on the corresponding bit. |
| D[6] | CLSC3 | 0 | |
| D[5] | CLSC2 | 0 | |
| D[4] | CLSC1 | 0 | |
| D[3] | DETC4 | 0 | Indicates whether a port has completed its detection process. These bits are set to 1 if detection has completed on the corresponding bit. |
| D[2] | DETC3 | 0 | |
| D[1] | DETC2 | 0 | |
| D[0] | DETC1 | 0 | |


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### DET/CLS_RESULT1 (26h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:4] | CLSR1 | 0000 | Returns the classification result for port 1.<br><br>0000: Classification is not done<br>0001: Class 1<br>0010: Class 2<br>0011: Class 3<br>0100: Class 4<br>0101: Class 5<br>0110: Class 0<br>0111: Over-current (OC) condition<br>1000: The first and secondary class results do not match<br><br>If Class 5 is enabled, any current that exceeds Class 4's upper limit is considered a Class 5 result. An OC condition triggers a current limit. If Class 5 is disabled, any current exceeding Class 4's upper limit is considered an OC condition. |
| D[3] | 2EVNTC1 | 0 | Indicates whether two-event classification has been completed on port 1. This bit is set to 1 if two-event classification has been completed. This bit is only set once Class 4 and Class 5 are successfully detected. |
| D[2:0] | DETR1 | 000 | Indicates port 1's detection result.<br><br>000: Detection has not completed (default after a power-on reset)<br>001: The port is shorted (VIN - OUT < 1.5V)<br>010: $C_{DET}$ too high (exceeds 5µF)<br>011: $R_{DET}$ is too low (below 19kΩ)<br>100: Detection is valid (19kΩ < $R_{DET}$ < 26.5kΩ)<br>101: $R_{DET}$ is too high (exceeds 26.5kΩ)<br>110: The port is open (<15µA load current)<br>111: Low impedance to PGND (OUT - PGND < 2V) |

### DET/CLS_RESULT2 (27h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:4] | CLSR2 | 0000 | Returns the classification result for port 2.<br><br>0000: Classification is not done<br>0001: Class 1<br>0010: Class 2<br>0011: Class 3<br>0100: Class 4<br>0101: Class 5<br>0110: Class 0<br>0111: Over-current (OC) condition<br>1000: The first and secondary class results do not match<br><br>If Class 5 is enabled, any current that exceeds Class 4's upper limit is considered a Class 5 result. An OC condition triggers a current limit. If Class 5 is disabled, any current exceeding Class 4's upper limit is considered an OC condition. |
| D[3] | 2EVNTC2 | 0 | Indicates whether two-event classification has been completed on port 2. This bit is set to 1 if two-event classification has been completed. This bit is only set once Class 4 and Class 5 are successfully detected. |


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| | | | |
|---|---|---|---|
| D[2:0] | DETR2 | 000 | Indicates port 2's detection result.<br><br>000: Detection has not completed (default after a power-on reset)<br>001: The port is shorted (VIN - OUT < 1.5V)<br>010: $C_{DET}$ too high (exceeds 5µF)<br>011: $R_{DET}$ is too low (below 19kΩ)<br>100: Detection is valid (19kΩ < $R_{DET}$ < 26.5kΩ)<br>101: $R_{DET}$ is too high (exceeds 26.5kΩ)<br>110: The port is open (<15µA load current)<br>111: Low impedance to PGND (OUT - PGND < 2V) |

## DET/CLS_RESULT3 (28h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:4] | CLSR3 | 0000 | Returns the classification result for port 3.<br><br>0000: Classification is not done<br>0001: Class 1<br>0010: Class 2<br>0011: Class 3<br>0100: Class 4<br>0101: Class 5<br>0110: Class 0<br>0111: Over-current (OC) condition<br>1000: The first and secondary class results do not match<br><br>If Class 5 is enabled, any current that exceeds Class 4's upper limit is considered a Class 5 result. An OC condition triggers a current limit. If Class 5 is disabled, any current exceeding Class 4's upper limit is considered an OC condition. |
| D[3] | 2EVNTC3 | 0 | Indicates whether two-event classification has been completed on port 3. This bit is set to 1 if two-event classification has been completed. This bit is only set once Class 4 and Class 5 are successfully detected. |
| D[2:0] | DETR3 | 000 | Indicates port 3's detection result.<br><br>000: Detection has not completed (default after a power-on reset)<br>001: The port is shorted (VIN - OUT < 1.5V)<br>010: $C_{DET}$ too high (exceeds 5µF)<br>011: $R_{DET}$ is too low (below 19kΩ)<br>100: Detection is valid (19kΩ < $R_{DET}$ < 26.5kΩ)<br>101: $R_{DET}$ is too high (exceeds 26.5kΩ)<br>110: The port is open (<15µA load current)<br>111: Low impedance to PGND (OUT - PGND < 2V) |

## DET/CLS_RESULT4 (29h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:4] | CLSR4 | 0000 | Returns the classification result for port 4.<br><br>0000: Classification is not done<br>0001: Class 1<br>0010: Class 2<br>0011: Class 3<br>0100: Class 4<br>0101: Class 5<br>0110: Class 0<br>0111: Over-current (OC) condition<br>1000: The first and secondary class results do not match<br><br>If Class 5 is enabled, any current that exceeds Class 4's upper limit is considered a Class 5 result. An OC condition triggers a current limit. If Class 5 is disabled, any current exceeding Class 4's upper limit is considered an OC condition. |


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| | | | |
|---|---|---|---|
| D[3] | 2EVNTC4 | 0 | Indicates whether two-event classification has been completed on port 4. This bit is set to 1 if two-event classification has been completed. This bit is only set once Class 4 and Class 5 are successfully detected. |
| D[2:0] | DETR4 | 000 | Indicates port 4's detection result.<br>000: Detection has not completed (default after a power-on reset)<br>001: The port is shorted (VIN - OUT < 1.5V)<br>010: $C_{DET}$ too high (exceeds 5µF)<br>011: $R_{DET}$ is too low (below 19kΩ)<br>100: Detection is valid (19kΩ < $R_{DET}$ < 26.5kΩ)<br>101: $R_{DET}$ is too high (exceeds 26.5kΩ)<br>110: The port is open (<15µA load current)<br>111: Low impedance to PGND (OUT - PGND < 2V) |

## POWER_STATUS (2Ah)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | PG4 | 0 | Indicates the power good (PG) status for all ports. This bit is set to 1 if the corresponding port's power is on, and if the OUTx pin's voltage is below $V_{PG}$.<br>The PG bit resets once the OUTx pin's voltage exceeds the $V_{PG}$ threshold with a short deglitch time. |
| D[6] | PG3 | 0 | |
| D[5] | PG2 | 0 | |
| D[4] | PG1 | 0 | |
| D[3] | PEN4 | 0 | Indicates whether power has been enabled on a port. These bits are set to 1 if the corresponding port is powered on. |
| D[2] | PEN3 | 0 | |
| D[1] | PEN2 | 0 | |
| D[0] | PEN1 | 0 | |

## POWER_STATUS_CHANGE (2Bh and 2Ch)

(2Bh) Read-only
(2Ch) Read and clear

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | PGC4 | 0 | Indicates whether the power good (PG) status has changed on the ports. This bit is set to 1 if the PG status changes on the corresponding port. |
| D[6] | PGC3 | 0 | |
| D[5] | PGC2 | 0 | |
| D[4] | PGC1 | 0 | |
| D[3] | PEC4 | 0 | Indicates whether the power status has been enabled or disabled on the ports. This bit is set 1 if the power status changes (disabled or enabled) on the corresponding port. |
| D[2] | PEC3 | 0 | |
| D[1] | PEC2 | 0 | |
| D[0] | PEC1 | 0 | |

## OVER_LOAD_STATUS (2Dh and 2Eh)

(2Dh) Read-only
(2Eh) Read and clear

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7] | OCUT4 | 0 | Indicates whether the ICUT1~4 timer ($t_{ICUT}$) has finished counting after ICUTx exceeds the over-current (OC) threshold. This bit is set to 1 if $t_{ICUT}$ times out. |
| D[6] | OCUT3 | 0 | |
| D[5] | OCUT2 | 0 | |
| D[4] | OCUT1 | 0 | |
| D[3] | STF4 | 0 | Indicates a start-up failure for all ports. This bit is set to 1 if start-up inrush timer times out, or if there is a power-on command failure. |
| D[2] | STF3 | 0 | |
| D[1] | STF2 | 0 | |
| D[0] | STF1 | 0 | |


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## CURRENT_LIMIT_STATUS (2Fh and 30h)

(2Fh) Read-only
(30h) Read and clear

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:4] | RESERVED | - | Reserved. |
| D[3] | OLIM4 | 0 | Indicates whether a hardware current limit has been triggered on the ports. These bits are set to 1 if a current limit is triggered on a corresponding port. |
| D[2] | OLIM3 | 0 | |
| D[1] | OLIM2 | 0 | |
| D[0] | OLIM1 | 0 | |

## DISCONNECT_STATUS (31h and 32h)

(31h) Read-only
(32h) Read and clear

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:5] | RESERVED | - | Reserved. |
| D[3] | DCDIS4 | 0 | Indicates whether a disconnected DC load event has occurred on the ports. These bits are set to 1 if a disconnected DC load event occurs on the corresponding port. |
| D[2] | DCDIS3 | 0 | |
| D[1] | DCDIS2 | 0 | |
| D[0] | DCDIS1 | 0 | |

## WATCHDOG_STATUS (33h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:1] | RESERVED | - | Reserved. |
| D[0] | WDS | 0 | Indicates the watchdog status. This bit is set to 0 if the watchdog times out without an active CLK signal. |

## PIN_STATUS (34h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:5] | RESERVED | - | Reserved. |
| D[4] | AUTO | A | Returns the AUTO pin's status during start-up. "A" is "1" if the AUTO pin is set high during start-up or a reset. "A" is "0" if the AUTO pin is set low. This bit is set to 1 if the AUTO pin is pulled high. |
| D[3] | A4A3 | D | Returns the A3~A0 pins' statuses during start-up. "D" is "1" if the corresponding pin is set high during start-up or a reset. "D" is "0" if the corresponding pin is set low. These bits are set to 1 if the corresponding pin's voltage is high. |
| D[2] | A3A2 | D | |
| D[1] | A2A1 | D | |
| D[0] | A1A0 | D | |

## LEGACY_DETECT_RESULT1 (35h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:4] | LEGDET2 | 0000 | Returns the legacy detection results for port 2.<br>0000: No legacy detection<br>0001: Valid (5µF < PD input capacitor < 100µF)<br>0010: Unable to discharge the PD input capacitance to 2.4V<br>0100: The first measurement exceeds the 18.5V maximum voltage<br>0101: The second measurement exceeds the 18.5V maximum voltage<br>0110: The difference between the measured voltages is below 0.5V |


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| | | | |
|---|---|---|---|
| D[3:0] | LEGDET1 | 0000 | Returns the legacy detection results for port 1.<br><br>0000: No legacy detection<br>0001: Valid (5µF < PD input capacitor < 100µF)<br>0010: Unable to discharge the PD input capacitance to 2.4V<br>0100: The first measurement exceeds the 18.5V maximum voltage<br>0101: The second measurement exceeds the 18.5V maximum voltage<br>0110: The difference between the measured voltages is below 0.5V |

**LEGACY_DETECT_RESULT2 (36h)**

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:4] | LEGDET4 | 0000 | Returns the legacy detection results for port 4.<br><br>0000: No legacy detection<br>0001: Valid (5µF < PD input capacitor < 100µF)<br>0010: Unable to discharge the PD input capacitance to 2.4V<br>0100: The first measurement exceeds the 18.5V maximum voltage<br>0101: The second measurement exceeds the 18.5V maximum voltage<br>0110: The difference between the measured voltages is below 0.5V |
| D[3:0] | LEGDET3 | 0000 | Returns the legacy detection results for port 3.<br><br>0000: No legacy detection<br>0001: Valid (5µF < PD input capacitor < 100µF)<br>0010: Unable to discharge the PD input capacitance to 2.4V<br>0100: The first measurement exceeds the 18.5V maximum voltage<br>0101: The second measurement exceeds the 18.5V maximum voltage<br>0110: The difference between the measured voltages is below 0.5V |


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# ADC RESULT REGISTERS

## PORT_1_CURRENT (40h and 41h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| (40h) D[0] | PORT_1_ CURRENT_DATA | 0 | Returns the lower bit of port 1's ADC current result. |
| 41h D[7:0] | | 0000 0000 | Returns the higher bits of port 1's ADC current result.<br>The output current can be calculated with the following equation:<br>Output current = 2.4mA x COUNT - 10mA<br>Where COUNT is the unsigned binary integer of the ADC result. |

## PORT_1_VOLTAGE (42h and 43h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| 42h D[0] | OUT1_ PIN_ VOLTAGE _DATA | 0 | Returns the lower bit of port 1's ADC voltage result. |
| 43h D[7:0] | | 0000 0000 | Returns the higher bits of port 1's ADC voltage result.<br>The sum of these two registers is the OUT1 pin voltage. The port output voltage can be calculated with the following equation:<br>Output voltage = 0.15V x ($V_{IN}$ COUNT - OUT1 COUNT)<br>Where COUNT is the unsigned binary integer of the ADC result. |

## PORT_2_CURRENT (44h and 45h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| 44h D[0] | PORT_2_ CURRENT_ DATA | 0 | Returns the lower bit of port 2's ADC current result. |
| 45h D[7:0] | | 0000 0000 | Returns the higher bits of port 2's ADC current result.<br>The output current can be calculated with the following equation:<br>Output current = 2.4mA x COUNT - 10mA<br>Where COUNT is the unsigned binary integer of the ADC result. |

## PORT_2_VOLTAGE (46h and 47h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| 46h D[0] | OUT2_PIN_ VOLTAGE_ DATA | 0 | Returns the lower bit of port 2's ADC voltage result. |
| 47h D[7:0] | | 0000 0000 | Returns the higher bits of port 2's ADC voltage result.<br>The sum of these two registers is the OUT2 pin voltage. The port output voltage can be calculated with the following equation:<br>Output voltage = 0.15V x ($V_{IN}$ COUNT - OUT2 COUNT)<br>Where COUNT is the unsigned binary integer of the ADC result. |


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## PORT_3_CURRENT (48h and 49h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| 48h D[0] | PORT_3_ CURRENT_ DATA | 0 | Returns the lower bit of port 3's ADC current result. |
| 49h D[7:0] | | 0000 0000 | Returns the higher bits of port 3's ADC current result.<br>The output current can be calculated with the following equation:<br>Output current = 2.4mA x COUNT - 10mA<br>Where COUNT is the unsigned binary integer of the ADC result. |

## PORT_3_VOLTAGE (4Ah and 4Bh)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| 4Ah D[0] | OUT3_PIN_ VOLTAGE_ DATA | 0 | Returns the lower bit of port 3's ADC voltage result. |
| 4Bh D[7:0] | | 0000 0000 | Returns the higher bits of port 3's ADC voltage result.<br>The sum of these two registers is the OUT3 pin voltage. The port output voltage can be calculated with the following equation:<br>Output voltage = 0.15V x ($V_{IN}$ COUNT - OUT3 COUNT)<br>Where COUNT is the unsigned binary integer of the ADC result. |

## PORT_4_CURRENT (4Ch and 4Dh)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| 4Ch D[0] | PORT_4_ CURRENT_ DATA | 0 | Returns the lower bit of port 4's ADC current result. |
| 4Dh D[7:0] | | 0000 0000 | Returns the higher bits of port 4's ADC current result.<br>The output current can be calculated with the following equation:<br>Output current = 2.4mA x COUNT - 10mA<br>Where COUNT is the unsigned binary integer of the ADC result. |

## PORT_4_VOLTAGE (4Eh and 4Fh)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| 4Eh D[0] | OUT4_PIN_ VOLTAGE_ DATA | 0 | Returns the lower bit of port 4's ADC voltage result. |
| 4Fh D[7:0] | | 0000 0000 | Returns the higher bits of port 4's ADC voltage result.<br>The sum of these two registers is the OUT4 pin voltage. The port output voltage can be calculated with the following equation:<br>Output voltage = 0.15V x ($V_{IN}$ COUNT - OUT4 COUNT)<br>Where COUNT is the unsigned binary integer of the ADC result. |


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### INPUT_VOLTAGE (50h and 51h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| 50h D[0] | INPUT_ VOLTAGE_ DATA | 0 | Returns the lower bit of the ADC $V_{IN}$ result. |
| 51h D[7:0] | | 0000 0000 | Returns the higher bits of the ADC $V_{IN}$ result.<br>$V_{IN}$ can be calculated with the following equation:<br>$V_{IN} = 0.15V \times COUNT$<br>Where COUNT is the unsigned binary integer of the ADC result. |

### JUNCTION_TEMPERATURE (52h and 53h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| 52h D[0] | JUNCTION_ TEMP ERATURE_ DATA | 0 | Returns the lower bit of the ADC die temperature result. |
| 53h D[7:0] | | 0000 0000 | Returns the higher bits of the ADC die temperature result.<br>The junction temperature can be calculated with the following equation:<br>Junction temperature = 0.4°C x COUNT - 40°C<br>Where COUNT is the unsigned binary integer of the ADC result. |

### PMAX_POWER_SETTING (54h and 55h)

Read/write

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| 54h D[0] | PMAX_ SETTING_ DATA | 0 | Returns the lower bit of the ADC PMAX setting data result. |
| 55h D[7:0] | | 0000 0000 | Returns the higher bits of the ADC PMAX setting data result.<br>The maximum power load can be calculated with the following equation:<br>Max power load = 0.4W x COUNT<br>Where COUNT is the unsigned binary integer of the ADC result. The PMAX power result is latched when the MP3924 starts up or is reset. The PMAX power rating is in a decimal value as a multiple 0.4W. |

### DIE_ID (60h)

Read-only

| Bits | Bit Name | Default Value | Description |
|---|---|---|---|
| D[7:6] | FAB | 00 | Returns the fab location. |
| D[5:4] | MAJOR_REV | 00 | Returns the major revision. |
| D[3:2] | MINOR_REV | 00 | Returns the minor revision. |
| D[1:0] | VENDOR_ID | 00 | Returns the vendor ID. |


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## APPLICATION INFORMATION

### Selecting the Input Capacitor

The supply voltage ($V_{IN}$) must be between 44V and 57V. The input capacitor ($C_{IN}$) maintains the DC input voltage. The system input capacitor(s) must be rated for 100V, and they can be aluminum electrolytic capacitors. Place a 0.1µF decoupling ceramic capacitor close to VIN and PGND to bypass VIN.

### Selecting the VCC Capacitor

The MP3924 integrates the VCC (about 3.3V) to power the internal control circuit. The internal regulator requires a minimum 1µF ceramic bypass capacitor to be connected from VCC to DGND. The VCC current limit is typically 17mA. Do not connect a heavy external load to VCC, as the VCC voltage may drop. This can result in a high VIN to VCC LDO power loss.

### Selecting the Output Capacitor for Each Port

An output capacitor must be placed from VIN to OUTx for the MP3924's output. It is recommended to use a 0.1µF, 100V ceramic capacitor.

### Output Transient Voltage Suppression (TVS)

The port transient voltage suppression (TVS) should be rated for the expected port surge environment. $D_{TVS}$ should have a minimum reverse standoff voltage of 58V, as well as a maximum clamping voltage of 95V at the expected peak surge current.

### Selecting the Output MOSFET for Each Port

The port's MOSFET can be a small, inexpensive device with average performance characteristics as long as it meets the following conditions:

- The voltage rating should be 100V minimum for high-voltage surge environments.
- $R_{DS(ON)}$ should be below 150mΩ for power dissipation.
- The power dissipation for the power MOSFET (Q1) when $R_{DS(ON)}$ = 100mΩ at the maximum $I_{CUT}$ is about 85mW.
- The gate charge ($Q_G$) when $V_{GATE}$ = 10V should be below 50nC to satisfy faster response times under overload conditions.
- The gate voltage should be 20V to establish a sufficient margin while GATEx is about 10V.

The FDMC3612 is recommended for most applications.

### Selecting the SENSE Resistor for Each Port

The load current in each PSE port is sensed as the voltage across a current-sense resistor ($R_{SENSE}$, which is about 250mΩ). For more accurate current sensing, a Kelvin sense at the low end of the current-sense resistor is provided through pins SGND1 for ports 1 and 2, and SGND2 for ports 3 and 4 (see Figure 21).

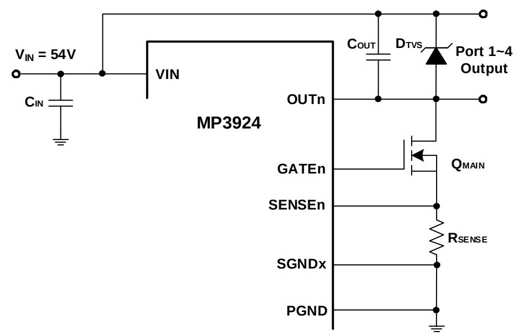


**Figure 21: Typical Output Components**

### Maximum Power Supply Setting

Connect one resistor from the PMAX pin to DGND to set the total power capability for all four output ports. The maximum output power is equal to the PMAX resistor value (in kΩ). For example, if 120W power is required for all for output, connect a 120kΩ resistor from PMAX to DGND.

### Selecting the Digital I/O Pull-Up Resistors

#### *EN*

EN is the enable input pin that can turn all internal circuits and ports on and off (except for the VCC regulator). Connect EN to VCC through a 100kΩ resistor to automatically turn on the MP3924.

#### *AUTO*

The AUTO pin sets automatic mode. AUTO is internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added). Float the AUTO pin for automatic mode. Connect the AUTO pin to DGND for shutdown mode.


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### *MID*

The MID pin sets the midspan mode. MID is internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added). Float the MID pin for midspan mode, and wait 2.8s before reinitiating detection. Connect MID to DGND to disable midspan mode.

### *A0~A3*

The A0~A3 pins set the MP3924's address. These pins are internally pulled up to VCC through a 50kΩ resistor (an external 10kΩ resistor can also be added). Connect these pins to VCC or DGND to set the lower 4 bits of the address (Address = 010 A3 A2 A1 A0).

### *CLS5*

The CLS5 enables Class 5. CLS5 is internally pulled down to DGND through a 50kΩ resistor. Leave CLS5 disconnected to disable the classification for Class 5 devices. (This is a high power level with the same classification as IEEE802.3 at. This is not standard class level that is compatible with IEEE802.3). Connect CLS5 to VCC to enable the classification of Class 5 devices.

### *SCL and SDAI*

SCL and SDAI are the $I^2C$ input pins. They must be connected to VCC through an external pull-up resistor (typically 4.7kΩ). If the $I^2C$ interface is not used, connect SCL to VCC and connect SDAI to DGND.

### *SDAO*

SDAO is open-drain output pin as well as the $I^2C$ serial data output pin. Connect SDAO to VCC through an external pull-up resistor (typically 4.7kΩ). Connect SDAO to SDAI for non-isolated applications. If the $I^2C$ interface is not used, connect SDAO to DGND.

### *INT1 and INT2*

INT1 and INT2 are open-drain outputs that act as the interrupt request pins for all interrupt source events. These pins are set low when the interrupt register is set and the interrupt function is enabled. Connect these pins to VCC through an external pull-up resistor (typically 4.7kΩ). If the interrupt function is not used, connect these pins to DGND.

## Over-Current Protection (OCP) and Overload Protection (OLP)

### *Inrush Current Limit*

The MP3924 provides a 425mA inrush current limit for inrush protection. When the external MOSFET begins to operate, inrush current protection is enabled. This protection allows the input capacitance of the PD to charge to the full $V_{IN}$ on the power interface. It also ensures the pass FET remains within its safe operating range.

If $I_{INRUSCH}$ exceeds $I_{CUT}$ during the inrush, the $I_{CUT}$ timer ($t_{ICUT}$) begins working. If $t_{ICUT}$ times out, the output turns off.

### *ICUT*

Following the end of start-up, a two current-limit protection scheme is applied to the ports. The first level is the ICUT current limit, which includes an ICUT timer ($t_{ICUT}$). If $t_{ICUT}$ times out because the ICUT current threshold is exceeded, the port shuts down. The ICUT current limit threshold is configured by the ICUTx bits (see Table 2).

**Table 2: ICUT Threshold**

| ICUT Register Value | $I_{CUT}$ (mA) |
|---|---|
| 000 | 375 |
| 001 | 110 |
| 010 | 188 |
| 011 | 375 |
| 100 | 650 |
| 101 | 920 |
| 110 | 500 |
| 111 | 625 |

In automatic mode, the bits are set to 000 for Class 0~3 results, set to 100 for Class 4 result, and set to 101 for Class 5 result automatically based on classification result.

### *ILIM*

The second level of current-limit protection is the ILIM current limit. The ILIM current limit is a hard limit. The GATE pin regulates the load at the current limit level, and one additional timer ($t_{ILIM}$) is enabled to record the current limit event. When $t_{ILIM}$ completes, the port shuts down. The ILIM current limit threshold can be configured via the ILIMx threshold register (see Table 3 on page 52).


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**Table 3: ILIM Threshold**

| ILIM Register Value | $I_{CUT}$ (mA) |
|---|---|
| 0 | 425 |
| 1 | 850 for Class 4 |
| | 1060 for Class 5 |

In automatic mode, the bits are set to 0 for Class 0~3 results, or they are set to 1 for Class 4 and Class 5 based on the classification result.

### Design Example

Table 4 shows a design example following the application guidelines.

**Table 4: Design Example**

| | |
|---|---|
| $V_{IN}$ | 44V to 57V |
| $V_{OUT}$ | 0V to 57V |
| $P_{OUT}$ | 4 x 0W to 30W |

Figure 23 on page 53 shows the detailed application schematic. The Typical Performance Characteristics section on page 15 shows the typical performance and circuit waveforms. For more device applications, refer to the related evaluation board datasheet(s).

### PCB Layout Guidelines

Efficient PCB layout is critical, as poor layout can result in reduced performance, resistive loss, and system instability. For the best results, refer to Figure 22 and follow the guidelines below:

1. Place the current-sense resistor close to the IC. To optimize accuracy, place the SENSE1~4 pins and the SGND1~2 pins close to the current-sense resistor. This minimizes the impact of the PCB trace resistance.
2. Kelvin connect the top of R1A–R1D to the SENSE1~4 pins. Kelvin connect the bottom of R1A and R1B to SGND1, then Kelvin connect R1C and R1D to SGND2.
3. Place the input capacitor (C1B) as close to the VIN and PGND pins as possible.
4. Place the VCC capacitor (C3) as close to the VCC and DGND pins as possible.
5. Place the PMAX resistor (R2) as close to the PMAX and DGND pins as possible.
6. Place a sufficient number of GND vias under the MP3924 to provide good thermal dissipation. This also lowers the PCB trace resistance from the bottom of the current-sense resistor to PGND.
7. Use a separated DGND and PGND layout. Connect DGND and PGND under the package, and between the DGND and PGND pins.

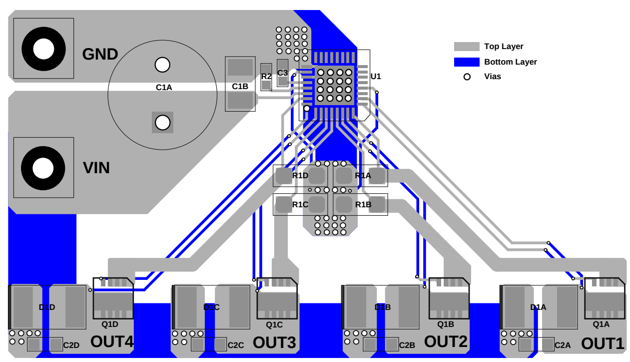


**Figure 22: Recommended PCB Layout**


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# TYPICAL APPLICATION CIRCUIT

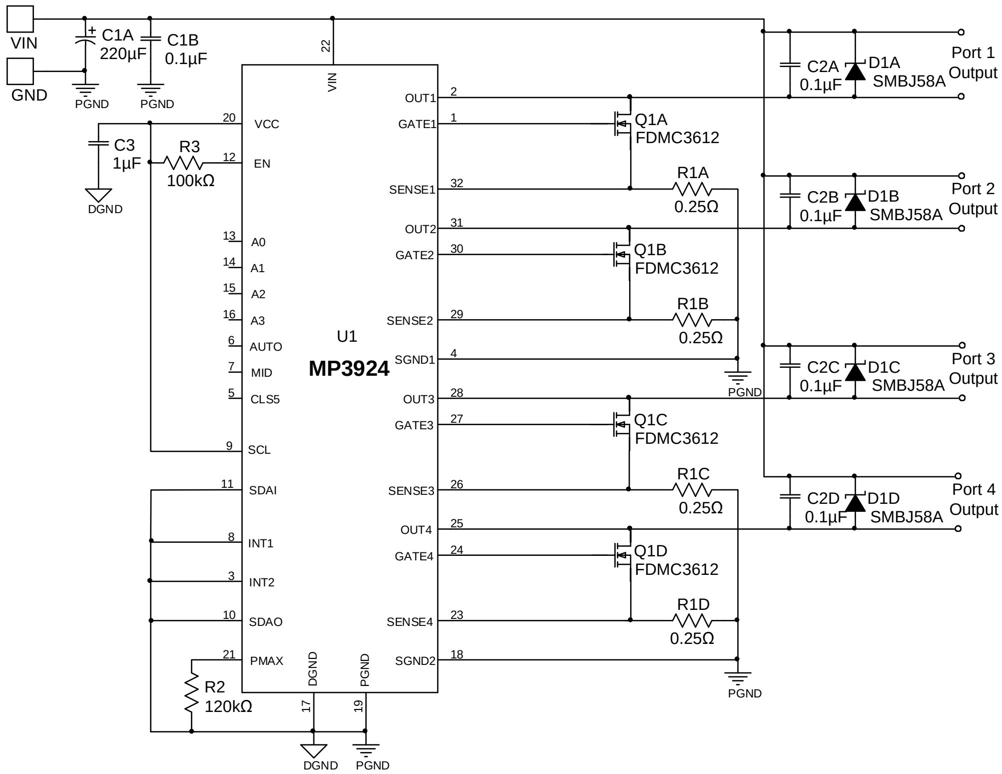


**Figure 23: Typical Application Circuit without I²C Control**


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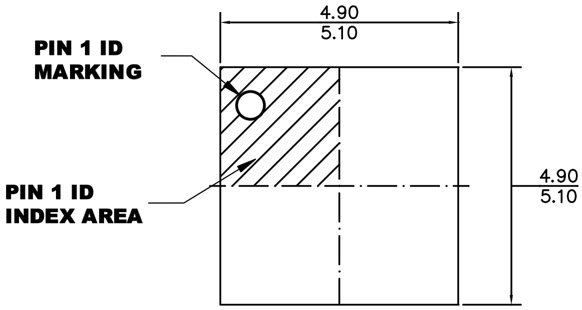
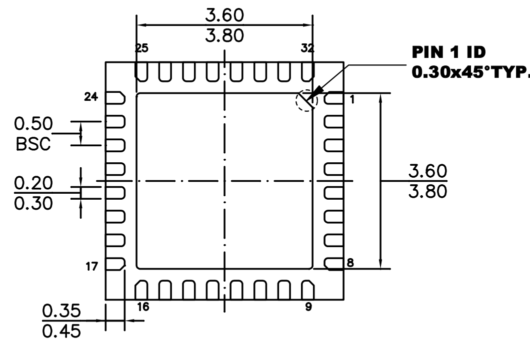
# PACKAGE INFORMATION

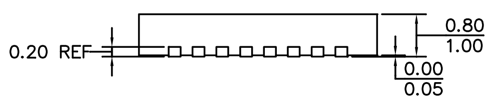
## QFN-32 (5mmx5mm)



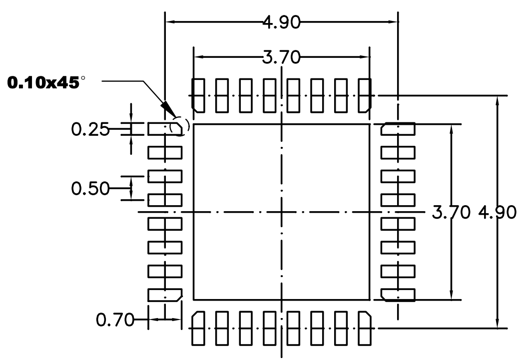

**TOP VIEW**




**BOTTOM VIEW**




**SIDE VIEW**




**RECOMMENDED LAND PATTERN**

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) DRAWING CONFIRMS TO JEDEC MO-220, VARIATION WHHE-1.
5) DRAWING IS NOT TO SCALE.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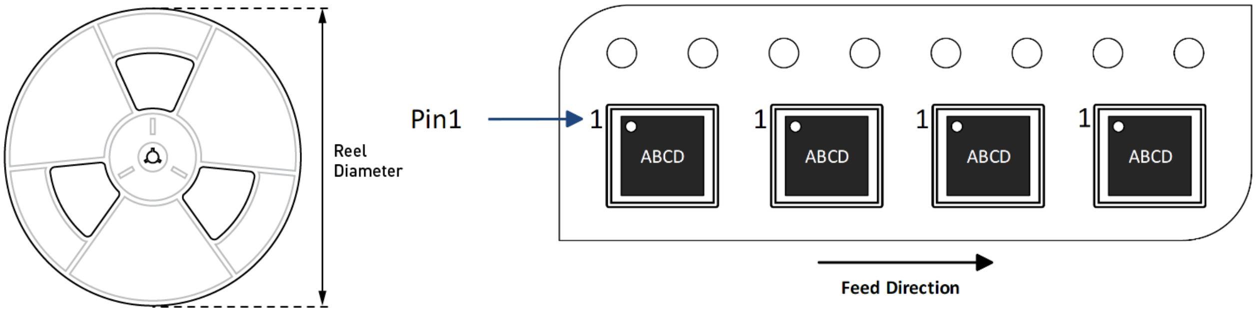
# CARRIER INFORMATION




| Part Number | Package Description | Quantity/ Reel | Quantity/ Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|
| MP3924GU-Z | QFN-32 (5mmx5mm) | 5000 | N/A | 13in | 12mm | 8mm |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## REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 07/16/2021 | Initial Release | - |

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