CA3262A, CA3262

November 1995

Quad-Gated Inverting Power Drivers

Features

- **Independent Over-Current Limiting On Each Output**
- **Independent Over-Temperature Limiting On Each Output**
- **Output Drivers Capable of Switching 700mA Load**
- **Inputs Compatible With TTL or 5V CMOS Logic**
- **Suitable For Resistive, Lamp or Inductive Loads**
- **Power-Frame Package Construction For Good Heat Dissipation**
- **Operating Temperature Ranges**
  - **CA3262A . . . . . -40°C to +125°C**
  - **CA3262 . . . . . -40°C to +85°C**

Applications

- **Solenoids**
- **Relays**
- **Lamps**
- **Steppers**
- **Small Motors**
- **Displays**

System Applications

- **Automotive**
- **Appliances**
- **Industrial Controls**
- **Robotics**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3262E	-40°C to +85°C	16 Lead Plastic DIP
CA3262AE	-40°C to +125°C	16 Lead Plastic DIP
CA3262AQ	-40°C to +125°C	28 Lead PLCC
CA3262AM	-40°C to +125°C	24 Lead Plastic SOIC (W)

Description

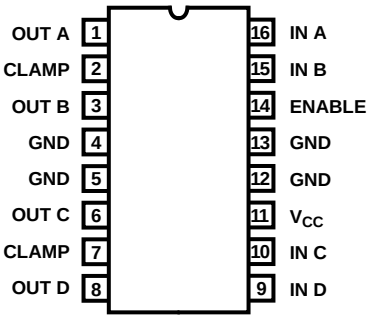
The CA3262 and CA3262A are used to interface low-level logic to high current loads. Each Power Driver has four inverting switches consisting of a non-inverting logic input stage and an inverting low-side driver output stage. All inputs are 5V TTL/CMOS logic compatible and have a common Enable input. Each output device has independent current limiting (I_{LIM}) and thermal limiting (T_{LIM}) for protection from over-load conditions. Steering diodes connected from each output (in pairs) to the Clamp pins may be used in conjunction with external zener diodes to protect the IC against over-voltage transients that result from inductive load switching.

To allow for maximum heat transfer from the chip, all ground pins on the DIP, PLCC and SOIC packages are directly connected to the mounting pad of the chip. Integral heat spreading lead frames directly connect the bond pads and ground leads to conduct heat from the chip junction to the PC Board for good heat dissipation.

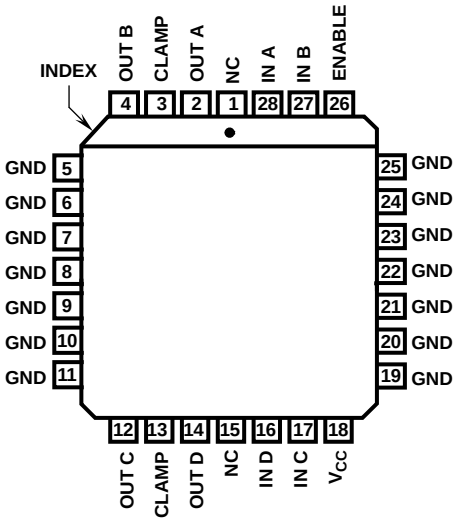
The CA3262 and CA3262A can drive four incandescent lamp loads without modulating their brilliance when the “cold” lamps are energized. Outputs may be parallel connected to drive high current loads. The maximum output current of each output is determined by the over-current limiting threshold which is typically 1.2A but may be as low as 0.7A.

Pinouts

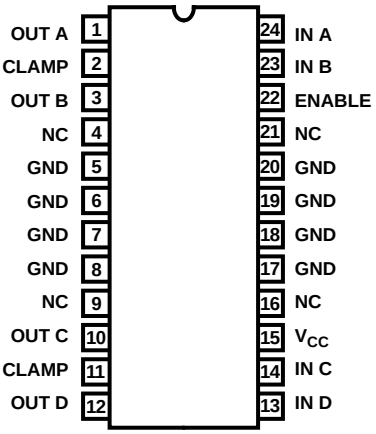
CA3262, CA3262A (PDIP)
TOP VIEW



CA3262A (PLCC)
TOP VIEW



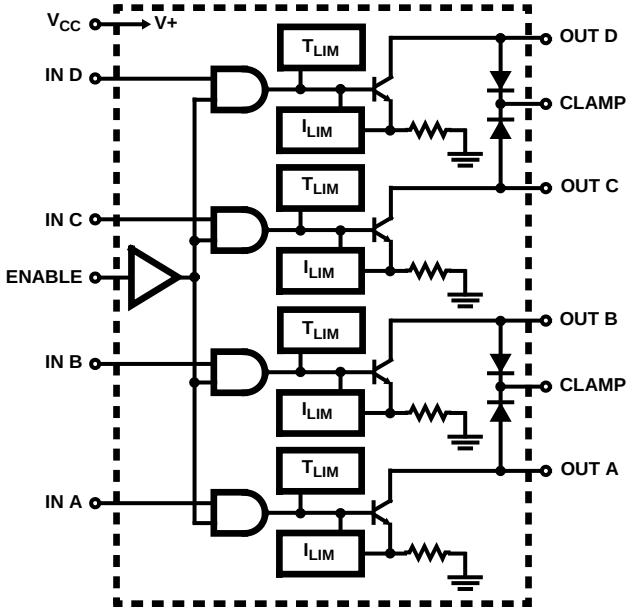
CA3262A (SOIC)
TOP VIEW
PRELIMINARY



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **1836.5**

Functional Block Diagram



TRUTH TABLE (Each Output)

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

H = High, L = Low, X = Don't Care

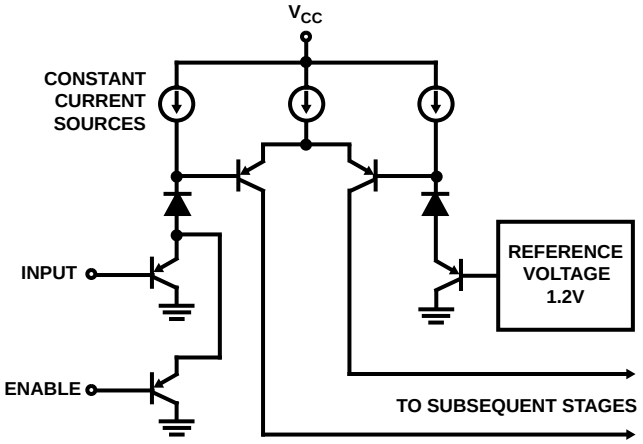


FIGURE 1. CA3262A EQUIVALENT SCHEMATIC OF ONE INPUT STAGE

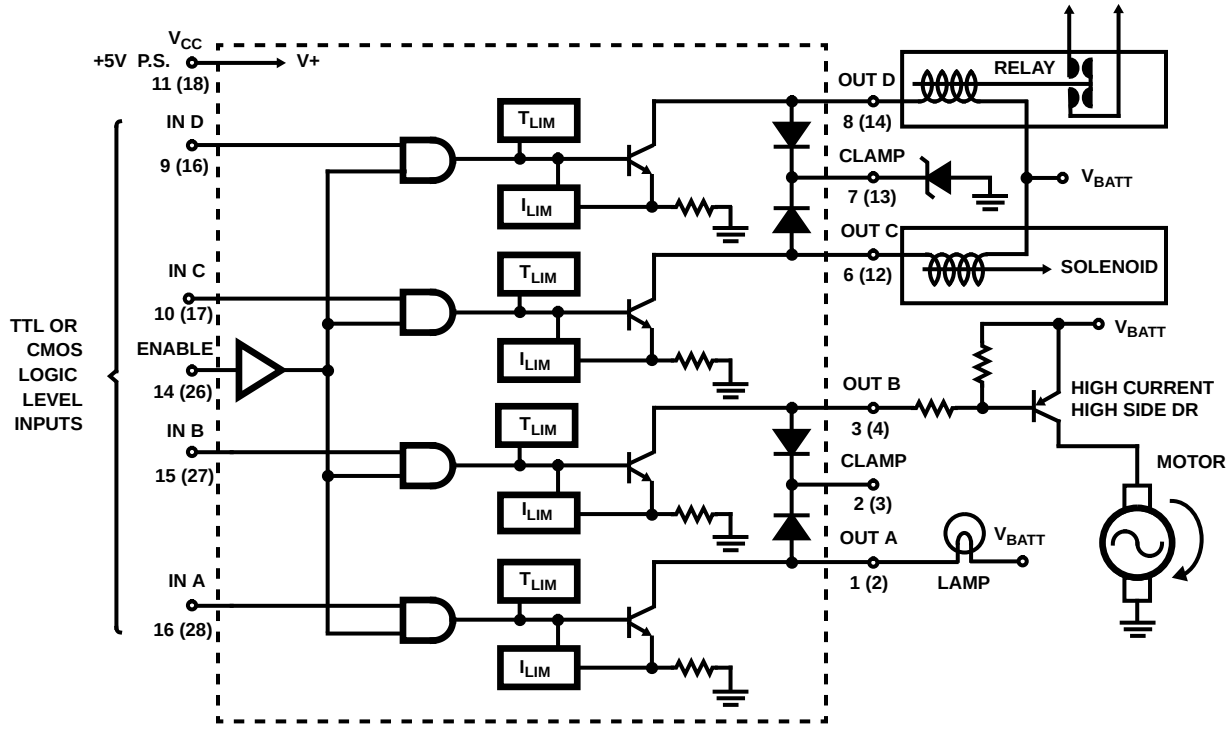


FIGURE 2. QUAD INVERTING POWER DRIVER (QDR) SHOWN WITH TYPICAL APPLICATION LOADS

Absolute Maximum Ratings

Logic Supply Voltage, V_{CC} 7.0V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CEX} 60V
Output Sustaining Voltage, $V_{CE(SUS)}$ 40V
Output Transient Current . . . . . (Note 1)
Output Load Current. . . . . (Note 2)
Storage Temperature Range . . . . . -65^oC to $+150^oC$
Operating Temperature Range
CA3262AE, CA3262AQ, CA3262AM . . . . . -40^oC to $+125^oC$
CA3262E. . . . . -40^oC to $+85^oC$
Maximum Junction Temperature . . . . . $+150^oC$
Lead Temperature (Soldering 10s). . . . . $+265^oC$

Thermal Information (Typical)

Thermal Resistance (Note 3)	θ_{JA}
CA3262AQ	$45^oC/W$
CA3262E, CA3262AE, CA3262AM	$60^oC/W$

Power Dissipation, P_D
CA3262E, CA3262AE (PDIP)
Up to $+60^oC$ (Free Air). 1.5W
Above $+60^oC$ . . . . . Derate Linearly at 16.6mW/^oC
Up to $+85^oC$ with PC Board Heat Sink 1.625W
Above $+85^oC$ . . . . . Derate Linearly at 25 mW/^oC
CA3262AQ (PLCC)
Up to $+85^oC$ (Free Air). 1.44W
Above $+85^oC$ . . . . . Derate Linearly at 22 mW/^oC
Up to $+105^oC$ with PC Board Heat Sink 1.5W
Above $+105^oC$ . . . . . Derate Linearly at 33 mW/^oC
CA3262AM (SOIC)
Up to $+60^oC$ (Free Air). 1.5W
Above $+60^oC$ . . . . . Derate Linearly at 16.6 mW/^oC
Up to $+85^oC$ with PC Board Heat Sink 1.80W
Above $+85^oC$ . . . . . Derate Linearly at 27.7 mW/^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{CC} = 5.5V, T_A= -40^oC to $+125^oC$ for CA3262A and V_{CC} = 5.5V, T_A= -40^oC to $+85^oC$ for CA3262 Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3262			CA3262A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Leakage Current	I_{CEX}	V_{CE} = 60V, V_{ENABLE} = 0.8V	-	-	100	-	0.6	50	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	Note 5	40	-	-	40	-	-	V
Collector Emitter Saturation Voltage (See Figures 4B and 5B)	$V_{CE(SAT)}$	V_{IN} = 2V, V_{CC} = 4.75V, I_C = 100mA	-	-	0.25	-	0.05	0.15	V
		I_C = 200mA	-	-	-	-	-	0.2	V
		I_C = 300mA	-	-	-	-	-	0.25	V
		I_C = 400mA	-	-	0.4	-	0.2	0.3	V
		I_C = 500mA	-	-	-	-	-	0.4	V
		I_C = 600mA	-	-	0.6	-	-	0.5	V
		I_C = 700mA, T_A = -40^oC	-	-	0.6	-	-	0.5	V
Input Low Voltage	V_{IL}		-	-	0.8	-	-	0.8	V
Input High Voltage	V_{IH}		2	-	-	2	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0.8V	-	-	10	-	0.75	10	µA
Input High Current	I_{IH}	V_{IN} = V_{ENABLE} = 5.5V, I_C = 600mA	-	-	10	-	-	10	µA
Supply Current, All Outputs ON, (See Figures 4A and 5A)	$I_{CC(ON)}$	V_{IN} = 2V, V_{ENABLE} = 5.5V, I_{OUTA} = 250mA, I_{OUTB} = 250mA, I_{OUTC} = 250mA, I_{OUTD} = 250mA	-	-	70	-	(Note 4)	55	mA
Supply Current, All Outputs OFF, (See Figures 4A and 5A)	$I_{CC(OFF)}$	V_{IN} = 0V	-	-	5	-	(Note 4)	5	mA
Clamp Diode Leakage Current	I_R	V_R = 60V	-	-	100	-	-	50	µA
Clamp Diode Forward Voltage, (See Figures 4D and 5D)	V_F	I_F = 1A, V_{IN} = 0V	-	-	1.7	-	-	1.7	V
		I_F = 1.5A, V_{IN} = 0V	-	-	2.1	-	-	2.1	V
Turn-On Delay, (See Figures 4C and 5C)	t_{PHL}, t_{PLH}	I_{OUT} = 500mA	-	-	8	-	-	8	µs
Over Current Limiting	I_{LIM}	V_{OUT} = 2V, V_{IN} = 5.5V, V_{ENABLE} = 5.5V	0.7	-	(Note 1)	0.7	-	(Note 1)	A

Electrical Specifications V_{CC} = 5.5V, T_A= -40°C to +125°C for CA3262A and V_{CC} = 5.5V, T_A= -40°C to +85°C for CA3262 Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3262			CA3262A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DESIGN PARAMETERS									
Over Temperature Limiting (Junction Temperature)	T_{LIM}		-	155	-	-	155	-	°C
Input Capacitance, Input	C_{IN}		-	-	-	-	3	-	pF
Enable Capacitance	C_{EN}		-	-	-	-	4.4	-	pF

NOTES:

1. The CA3262 and CA3262A have on-chip limiting for transient peak currents. Under short-circuit conditions with voltage applied to the collector of the output transistor and with the output transistor turned ON, the current will increase to 1.2A, typical. Over-Current Limiting protects a short circuit condition for a normal operating range of output supply voltage. During a short circuit condition, the output driver will shortly thereafter (approx. 5ms) go into Over-Temperature Limiting. While Over-Current Limiting may range to peak currents greater than 2A, each output will typically withstand a direct short circuit up to supply voltage levels of 16V. Excessive dissipation before thermal limiting occurs may cause damage to the chip for supply voltages greater than 18V. The CA3262 and CA3262A are rated to withstand peak current, cold turn-on conditions of #168 or #194 lamp loads.
2. The total DC current for the CA3262 and CA3262A with all 4 outputs ON should not exceed the total of (4 x 0.7A + Max. I_{CC}) ~ 2.85A. This level of current will significantly increase the chip temperature due to increased dissipation and may cause thermal shutdown in high ambient temperature conditions (See Absolute Maximum Ratings for Dissipation). Any one output may be allowed to exceed 0.7A but may be subject to Over-Current Limiting above the I_{LIM} min. limit of 0.7A. As a practical limit, no single output should be loaded to more than 1A max.
3. Normal applications require a surface mount of the 28 lead PLCC and 24 lead SOIC packages on a PC Board. The PLCC, SOIC and PDIP packages have power lead frame construction through the ground pins to conduct heat from the frame to the PC Board. With 2 square inches of surface copper area adjacent to the ground pins, the thermal resistance of each package may be as low as 30°C/W for the PLCC, 36°C/W for the 24 lead SOIC and 40°C/W for the 16 lead PDIP.
4. I_{CC} varies with temperature. Typically, $I_{CC(ON)}$ is 18mA at +125°C and 41mA at -40°C. Typically, $I_{CC(OFF)}$ is 2.2mA at +125°C and 1.2mA at -40°C.
5. Tested with a switched-off 500mA Load (24Ω series resistance), V_{BATT} = 12V and the outputs (V_{CE}) clamped to +40V maximum with an external zener diode.

Applications

Typical circuit configurations for applying the CA3262 and CA3262A are shown in the application circuit of Figure 2. To their rated capabilities, both circuits can be used to drive inductive, resistive and lamp loads. The CA3262A has a lower V_{SAT} than the CA3262 and is rated for +125°C ambient temperature applications. The CA3262 data sheet rating is +85°C. Otherwise, the protection features described apply to both the CA3262 and CA3262A.

The maximum voltage for full load current switching is the output sustaining voltage, $V_{CE(SUS)}$ which should not exceed 40V. To provide a means of over-voltage protection, on-chip steering diodes are connected from each output to one of two CLAMP pins. Over-voltage pulses may be generated from inductive load switching and must be clamped or limited to a peak voltage less than $V_{CE(SUS)}$. To limit an inductive voltage pulse, a zener diode should be connected to the appropriate CLAMP pin. When the voltage pulse exceeds the zener threshold, the excess energy is dumped to ground via the on-chip steering diode and the external zener diode.

The on-chip diodes may be used in a free-wheeling mode by connecting the CLAMP pins to an external clamp supply voltage. Zener diode clamp protection is preferred over the power supply clamp option, primarily because the power supplies may be subject to large transient changes; including turn-ON and turn-OFF conditions where non-tracking conditions between supplies could allow forward conduction through the steering diodes. For all transient conditions of either method, the clamp voltage should greater than the maximum supply voltage of the switching outputs and less than $V_{CE(SUS)}$.

Note that the rate of change of the output current during load switching is fast. Therefore, even small values of inductance, including the inductance of a few meters of hook-up wire to the load circuit, can generate voltage spikes of considerable amplitude at the output terminals and may require clamping to protect the device ratings.

Current-limiting is provided as protection for shorted or overloaded output conditions. Voltage is sampled across a small metal resistor in the emitter of each output stage. When the voltage exceeds a preset comparator level, drive is reduced to the output. Current limiting is sustained unless thermal conditions exceed the preset thermal shutdown temperature of +155°C.

If an output is shorted, the remaining three outputs will continue to function normally unless the continued heat spreading is sufficient to raise the junction temperature at any other output to a level greater than +155°C. High ambient temperature conditions may allow this to happen. The degree of interaction is minimized at chip layout design by separating the output devices, each to a separate corner of the chip.

As noted, the thermal resistance values of the PDIP, PLCC and SOIC packages are improved by direct connection of the leads to the chip mounting pad. For a normal PC Board application, the thermal resistance coefficient for each package can be significantly lowered by increasing ground copper area on the PC board next to the ground pins of the IC.

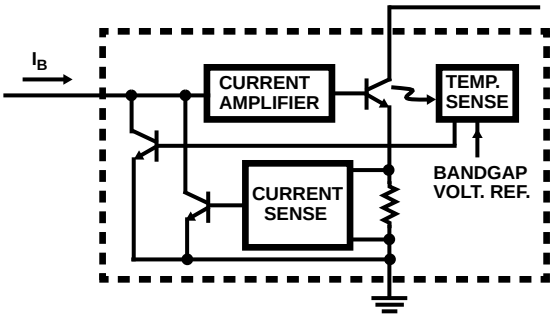


FIGURE 3. EACH OUTPUT POWER DRIVER IS A COMPOSITE CIRCUIT WITH OVER-TEMPERATURE SENSE FOR THERMAL LIMITING AND OVER-CURRENT SENSE TO PROVIDE CURRENT LIMITING

Typical Performance Curves

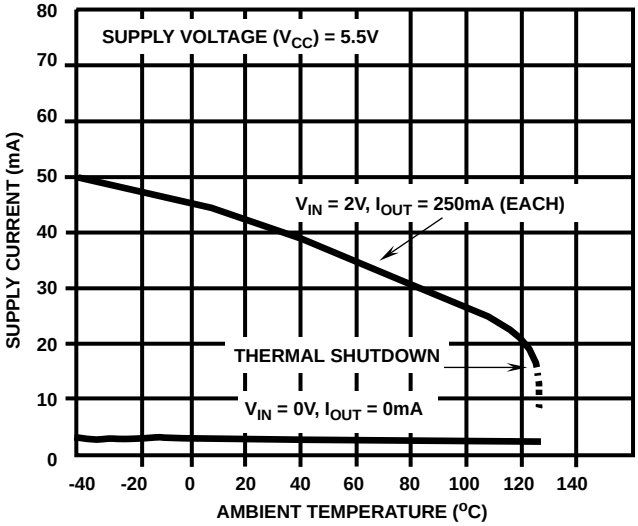


FIGURE 4A. TYPICAL SUPPLY CURRENT (PIN 11) CHARACTERISTICS

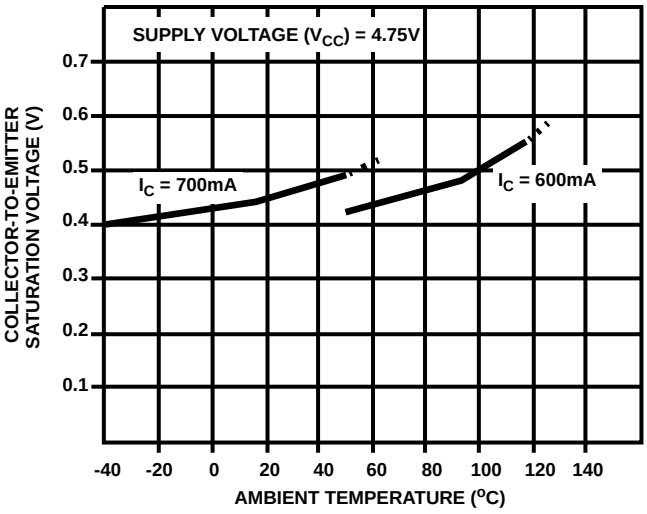


FIGURE 4B. TYPICAL COLLECTOR-TO-EMITTER SATURATION VOLTAGE CHARACTERISTICS IN QUAD-GATED INVERTING POWER DRIVER OUTPUT

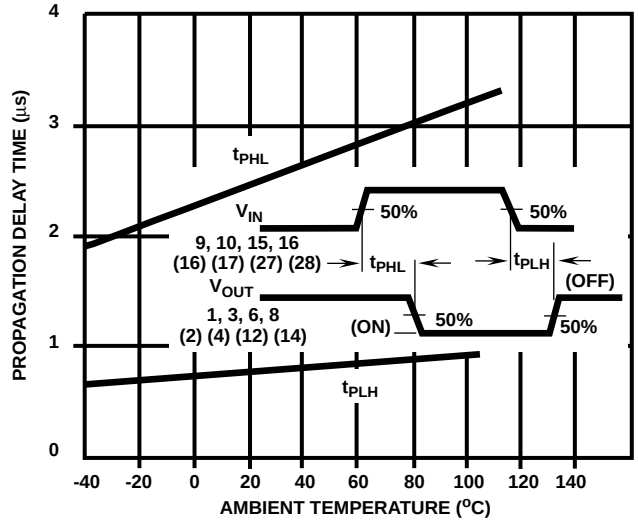


FIGURE 4C. TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS

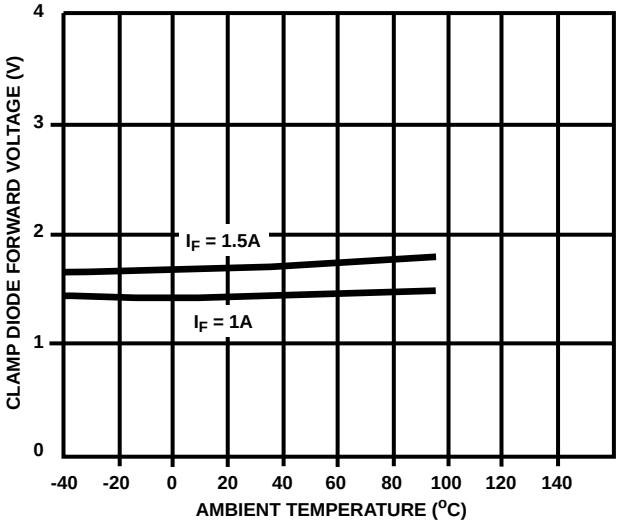


FIGURE 4D. TYPICAL CLAMP-DIODE FORWARD VOLTAGE CHARACTERISTICS

FIGURE 4. TYPICAL CHARACTERISTICS OF THE CA3262E

Typical Performance Curves (Continued)

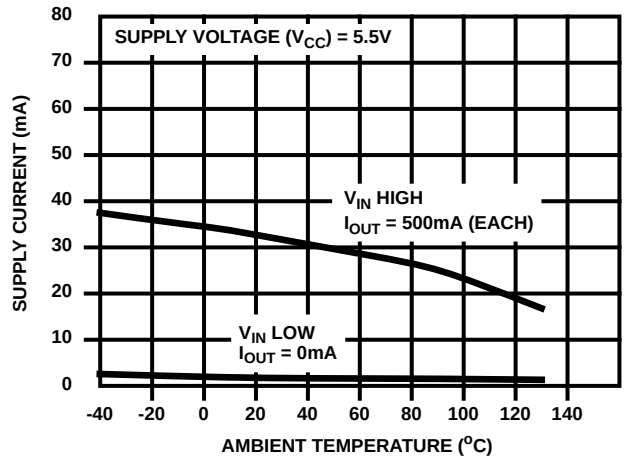


FIGURE 5A. TYPICAL SUPPLY CURRENT (PIN 11) CHARACTERISTICS

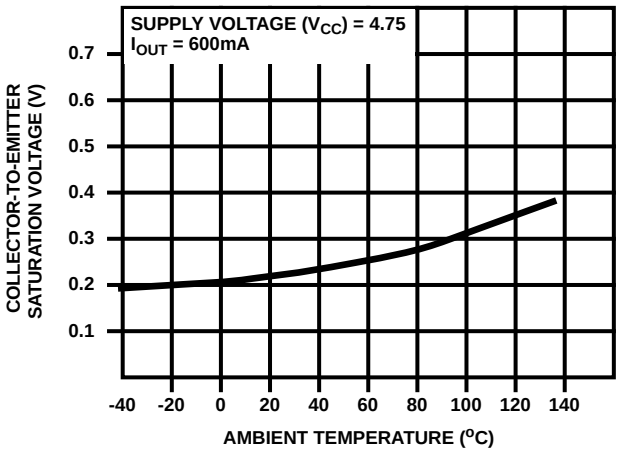


FIGURE 5B. TYPICAL COLLECTOR-TO-EMITTER SATURATION VOLTAGE CHARACTERISTICS IN QUAD-GATED INVERTING POWER DRIVER OUTPUTS

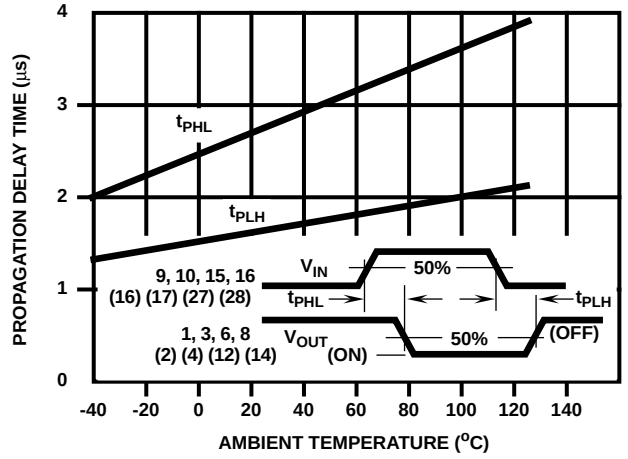


FIGURE 5C. TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS

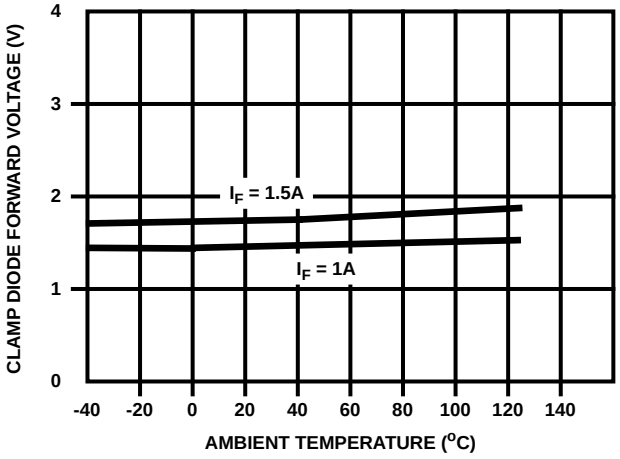


FIGURE 5D. TYPICAL CLAMP-DIODE FORWARD VOLTAGE CHARACTERISTICS

FIGURE 5. TYPICAL CHARACTERISTICS OF THE CA3262AE AND CA3262AQ

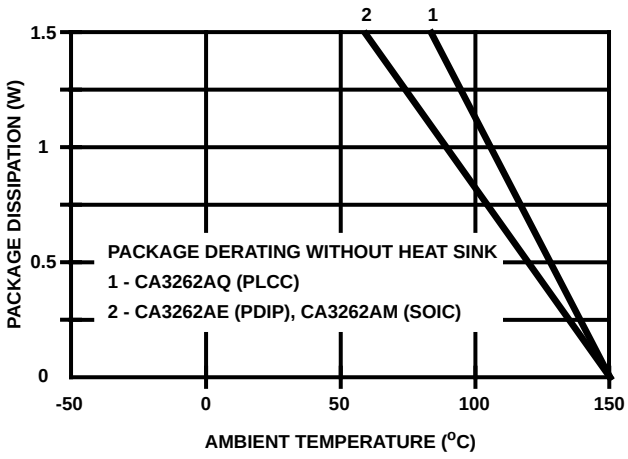


FIGURE 6A. DISSIPATION RATING CHART FOR PLCC, PDIP AND SOIC PACKAGES WITHOUT ADDITIONAL HEAT SINKS

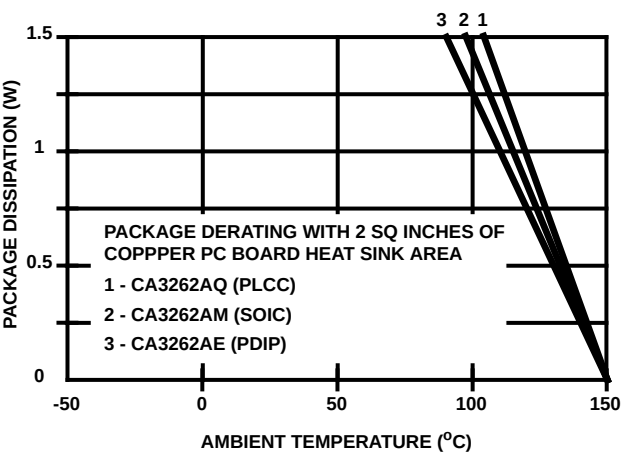
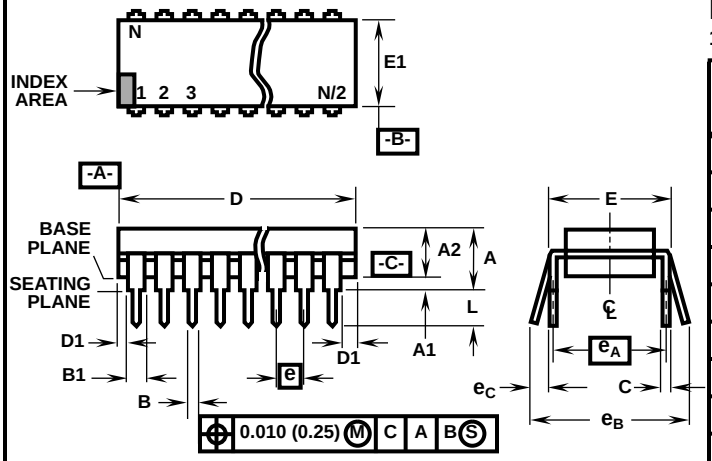


FIGURE 6B. DISSIPATION RATING CHART FOR PLCC, PDIP AND SOIC PACKAGES WITH 2 SQ. IN. OF COPPER PC BOARD HEAT SINKING

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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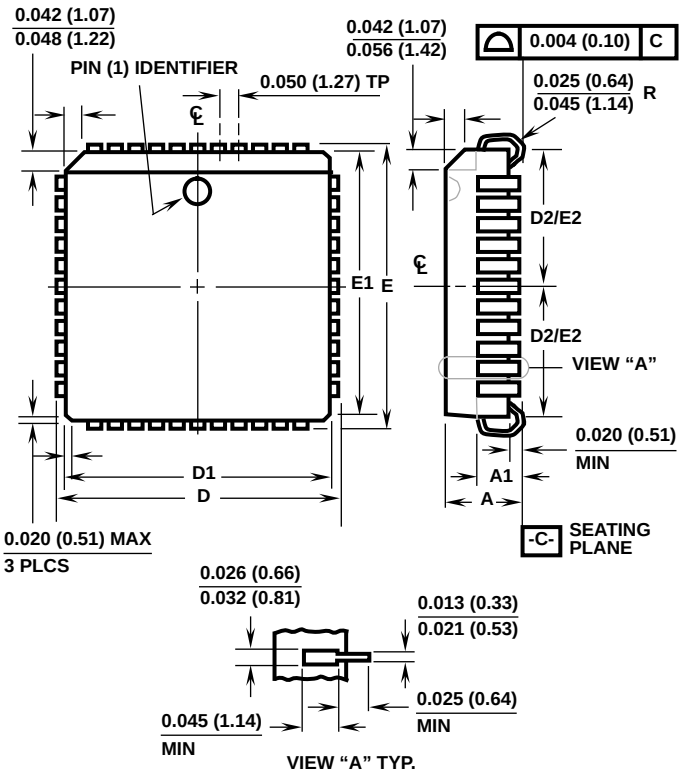
Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

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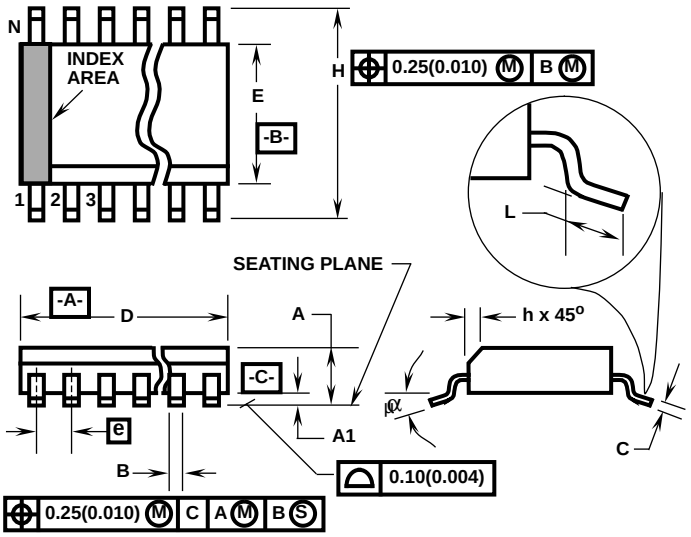
NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

Small Outline Plastic Packages (SOIC)



M24.3 **(JEDEC MS-013-AD ISSUE C)**
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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