UNITRODE

UCC1895
UCC2895
UCC3895
PRELIMINARY

BiCMOS Advanced Phase Shift PWM Controller

FEATURES

- Programmable Output Turn-on Delay
- Adaptive Delay Set
- Bidirectional Oscillator Synchronization
- Capability for Voltage Mode or Current Mode Control
- Programmable Soft Start/Soft Stop and Chip Disable via a Single Pin
- 0% to 100% Duty Cycle Control
- 6.5MHz Error Amplifier
- Operation to 1MHz
- Low Active Current Consumption (5mA Typical @ 500kHz)
- Very Low Current Consumption During Undervoltage Lock-out (150µA typical)

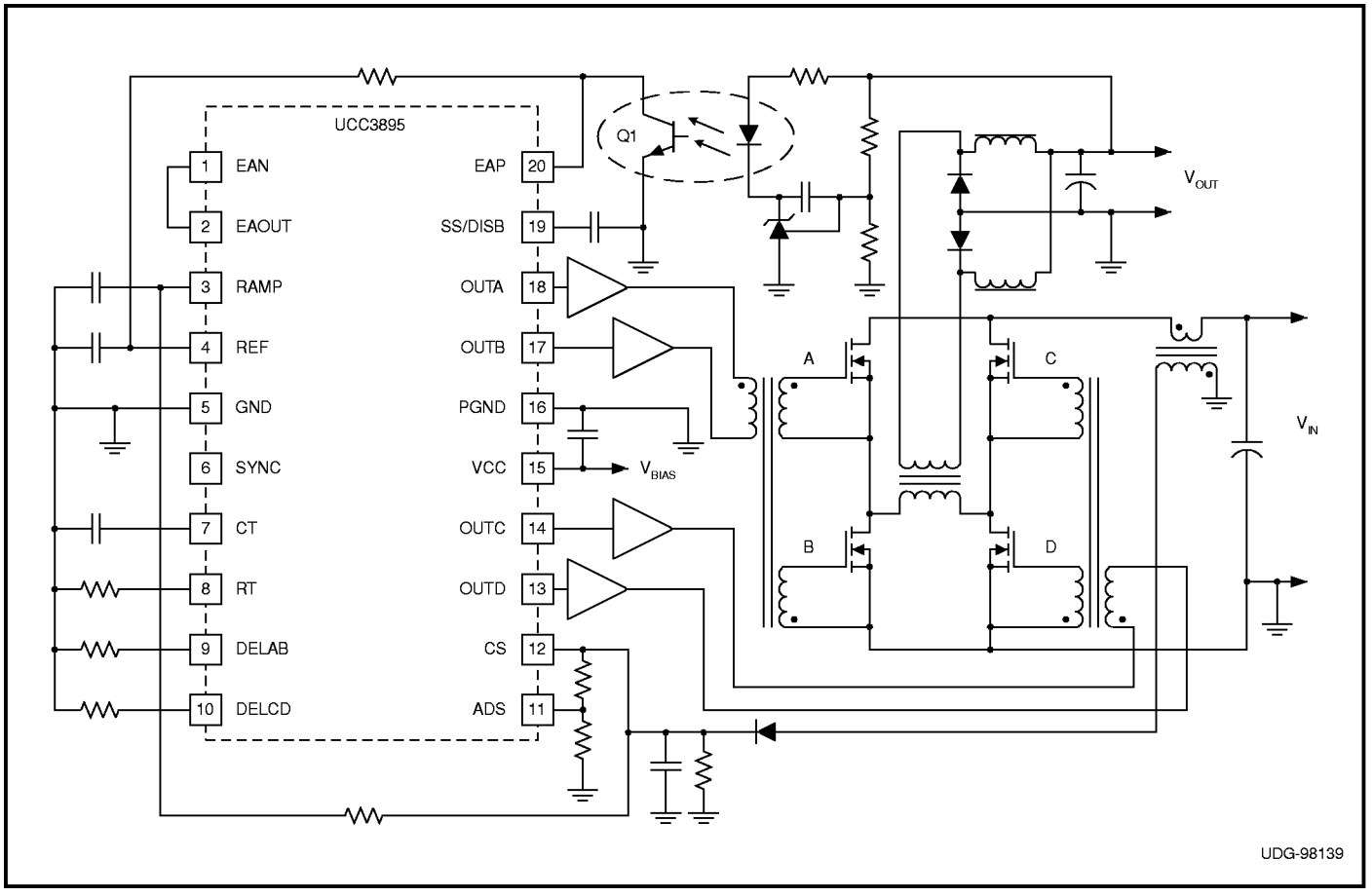
DESCRIPTION

The UCC3895 is a phase shift PWM controller that implements control of a full-bridge power stage by phase shifting the switching of one half-bridge with respect to the other. It allows constant frequency pulse-width modulation in conjunction with resonant zero-voltage switching to provide high efficiency at high frequencies. The part can be used either as a voltage mode or current mode controller.

While the UCC3895 maintains the functionality of the UC3875/6/7/8 family and UC3879, it improves on that controller family with additional features such as enhanced control logic, adaptive delay set, and shutdown capability. Since it is built in BCDMOS, it operates with dramatically less supply current than it's bipolar counterparts. The UCC3895 can operate with a maximum clock frequency of 1MHz.

The UCC3895 and UCC2895 are offered in the 20 pin SOIC (DW) package, 20 pin PDIP (N) package, 20 pin TSSOP (PW) package, and 20 pin PLCC (Q). The UCC1895 is offered in the 20 pin CDIP (J) package, and 20 pin CLCC package (L).

SIMPLIFIED APPLICATION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

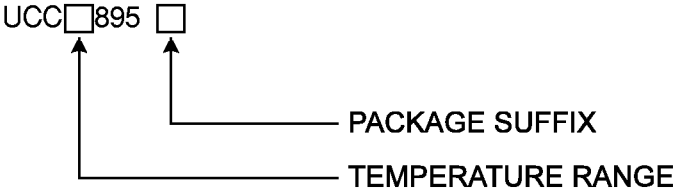
Supply Voltage (IDD < 10mA) 17V
Supply Current 30mA
REF current 15mA
OUT Current 100mA
Analog inputs
(EAP, EAN, EAOUT, RAMP,
SYNC, ADS, CS, SS/DISB) . . . . . –0.3V to REF+0.3V
Power Dissipation at T_A=+25°C (N Package) 1W
Power Dissipation at T_A=+25°C (D Package) 650mW
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +125°C
Lead Temperature (soldering, 10 sec) . . . . . +300°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of package.

TEMPERATURE & PACKAGE SELECTION TABLE

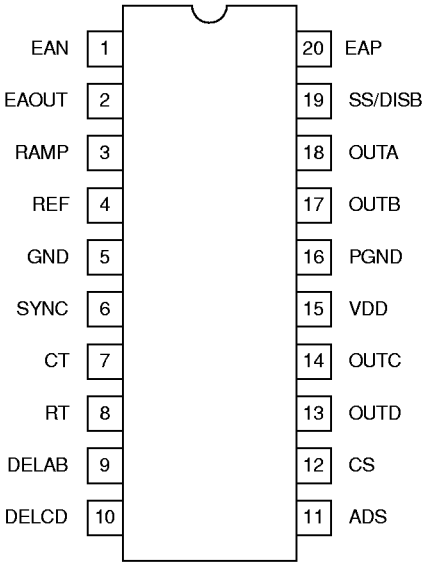
	TEMPERATURE RANGE	PACKAGE SUFFIX
UCC1895	–55°C to +125°C	J, L
UCC2895	–40°C to +85°C	DW, N, PW, Q
UCC3895	0°C to +70°C	DW, N, PW, Q

ORDERING INFORMATION

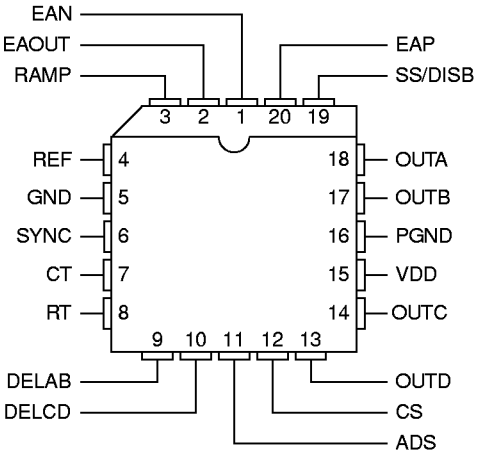


CONNECTION DIAGRAMS

DIL-20,c SOIC-20, TSSOP-20 (TOP VIEW)
J or N Package, DW Package, PW Package



PLCC-20, CLCC-20 (TOP VIEW)
Q Package, L Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VDD=12V, RT=82k, CT=220pF, RDELAB=10k, RDELCD=10k, C_{REF}=0.1µF, C_{VDD}=1.0µF, no load at outputs. $T_A = T_J$. T_A = 0°C to 70°C for UCC3895x, –40°C to +85°C for UCC2895x, and –55°C to +125°C for UCC1895x.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UVLO Section					
Start Threshold			11		V
Stop Threshold			9		V
Hysteresis			2		V
Supply Current					
Start-up Current	VDD = 8V		150	300	µA
I_{DD} Active			5		mA
VDD Clamp Voltage	IDD = 10mA		17.5		V
Voltage Reference Section					
Output Voltage	T_J = 25°C	4.95	5	5.05	V
	9V < VDD < 17.5V, 0mA < IREF < 5mA, Temperature	4.85	5	5.15	V
Short Circuit Current	REF = 0V, T_J = 25°C		20		mA
Error Amplifier Section					
Common Mode Input Voltage Range		–0.1		3.6	V
Offset Voltage		–5		5	mV
Input Bias Current (EAP, EAN)		–2		2	µA
EAOUT VOH	EAP–EAN = 500mV, I_{EAOUT}= –0.5mA	3.6	4	5	V
EAOUT VOL	EAP–EAN = –500mV, I_{EAOUT}= 0.5mA	0	0.3	0.4	V
EAOUT Source Current	EAP–EAN = 500mV, EAOUT= 2.5V	0.7	1		mA
EAOUT Sink Current	EAP–EAN = –500mV, EAOUT= 2.5V	2.5	3		mA
Open Loop DC Gain		70	80		dB
Unity Gain Bandwidth			6.5		MHz
Slew Rate	EAN from 1V to 0V, EAP = 500mV, EAOUT from 0.5V to 3.0V		2		V/µs
No Load Comparator Turn-Off Threshold			0.5		V
No Load Comparator Turn-On Threshold			0.6		V
Oscillator Section					
Frequency	T_J = 25°C	484	511	538	kHz
Total Variation	Line, Temperature		2.5	5	%
SYNC VIH			2.1		V
SYNC VIL			1.9		V
SYNC VOH	I_{SYNC} = –400µA, CT = 2.6V	4	4.3		V
SYNC VOL	I_{SYNC} = 100µA, CT = 2.6V		0.7	1	V
SYNC Output Pulse Width	SYNC Load = 1MEG and 10pF in parallel		75	125	ns
RT Voltage		2.9	3	3.1	V
CT Peak Voltage		2.45	2.5	2.55	V
CT Valley Voltage		0	0.1	0.2	V
PWM Comparator Section					
EAOUT to RAMP Input Offset Voltage	RAMP = 0V, DELAB = DELCD = REF	0.7	0.8	0.95	V
Minimum Phase Shift (OUTA to OUTC, OUTB to OUTD)	RAMP = 0V, EAOUT = 650mV (Note 1)	0	0.6		%
RAMP to OUTC/OUTD Delay	RAMP from 0V to 2.5V, EAOUT = 1.2V, DELAB = DELCD = REF (Note 2)		75		ns
RAMP Bias Current	0V < RAMP < 5V, SYNC = 0V to REF, CT = 0V	–5		50	µA

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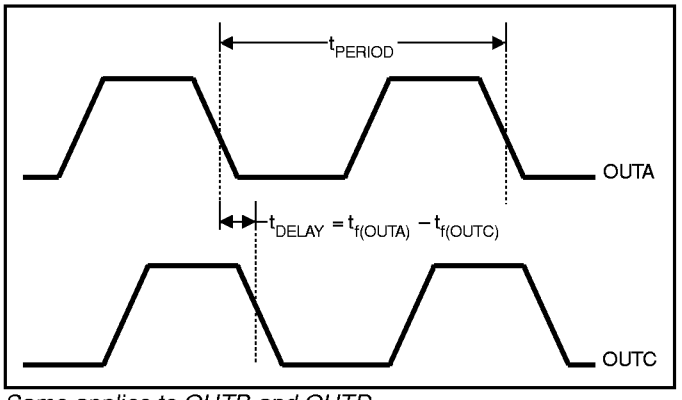
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Current Sense Section					
CS Bias Current	0 < CS , 2.5V, 0 < ADS < 2.5V	–3		20	µA
Peak Current Threshold			2		V
Overcurrent Threshold			2.5		V
CS to Output Delay	CS from 0 to 2.3V, DELAB = DELCD = REF		75		ns
Soft Start/Shutdown Section					
Soft Start Current	SS/DISB = 3.0V, CS < 1.9V		–37		µA
Soft Stop Current	SS/DISB = 3.0V, CS > 2.6V		370		µA
Soft Start/Disable Comparator Threshold			0.5		V
Delay Set Section					
DELAB/DELCD Output Voltage	ADS = CS = 0V		0.5		V
	ADS = 0V, CS = 2.0V		2.0.		V
Output Delay	ADS = CS = 0V (Note 2)		500		ns
ADS Bias Current	0V < ADS < 2.5V, 0V < CS < 2.5V	–20		20	µA
Output Section					
VOH (all outputs)	IOUT = –10mA, VDD to Output		250	350	mV
VOL (all outputs)	IOUT = 10mA		150	250	mV
Rise TIme	C_{LOAD} = 100pF		30		ns
Fall Time	C_{LOAD} = 100pF		20		ns

Note 1: Minimum phase shift is defined as followed:

$$\Phi = 200 \bullet \frac{t_{f(OUTA)} - t_{f(OUTC)}}{t_{PERIOD}} \quad Or$$

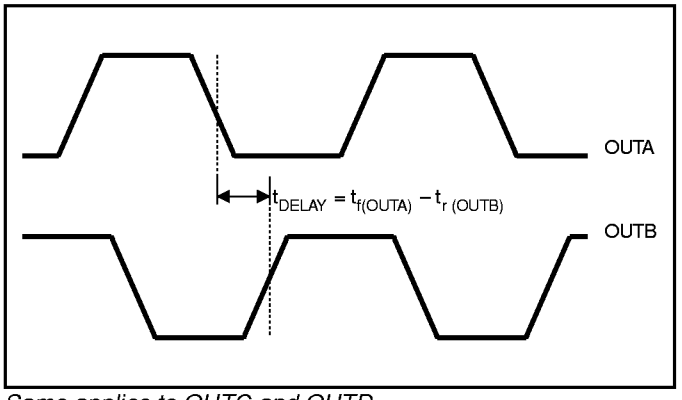
$$\Phi = 200 \bullet \frac{t_{f(OUTB)} - t_{f(OUTD)}}{t_{PERIOD}} \quad where$$

$t_{f(OUTA)}$ = *falling edge of OUTA signal*
$t_{f(OUTB)}$ = *falling edge of OUTB signal*
$t_{f(OUTC)}$ = *falling edge of OUTC signal*
$t_{f(OUTD)}$ = *falling edge of OUTD signal*
$t_{(PERIOD)}$ = *period of OUTA or OUTB signal*



Same applies to OUTB and OUTD

Note 2. Output delay is measured between OUTA/OUTB or OUTC/OUTD. Output delay is defined as shown below, where:
$t_{f(OUTA)}$ = *falling edge of OUTA signal*
$t_{r(OUTB)}$ = *rising edge of OUTB signal*



Same applies to OUTC and OUTD

PIN DESCRIPTIONS

ADS: Adaptive Delay Set. This function sets the ratio between the maximum and minimum programmed output delay dead time. When the ADS pin is directly connected to the CS pin, no delay modulation occurs. The maximum delay modulation occurs when ADS is grounded. In this case, delay time is four times longer when CS = 0 than when CS = 2.0V (the Peak Current threshold), ADS changes the output voltage on the delay pins DELAB and DELCD by the following formula:

$$V_{DEL} = [0.75 \bullet (V_{CS} - V_{ADS})] + 0.5V$$

where V_{CS} and V_{ADS} are in Volts. ADS must be limited to between 0V and 2.5V.

EAOUT: Error Amplifier Output. It is also connected internally to the non-inverting input of the PWM comparator and the no-load comparator. EAOUT is internally clamped to the soft start voltage. The no-load comparator shuts down the output stages when EAOUT falls below 500mV, and allows the outputs to turn-on again when EAOUT rises above 600mV.

CT: Oscillator Timing Capacitor. (Refer to Fig. 1, Oscillator Block Diagram) The UCC3895's oscillator charges CT via a programmed current. The waveform on C_T is a sawtooth, with a peak voltage of 2.5V. The approximate oscillator period is calculated by the following formula:

$$t_{OSC} = \frac{5 \bullet R_T \bullet C_T}{48} + 75\,ns$$

where C_T is in Farads, and R_T is in Ohms and t_{OSC} is in seconds. C_T can range from 100pF to 880pF. Please note that a large C_T and a small R_T combination will result in extended fall times on the C_T waveform. The increased fall time will increase the SYNC pulse width, hence limiting the maximum phase shift between OUTA, OUTB and OUTC, OUTD outputs, which limits the maximum duty cycle of the converter.

CS: Current Sense. This is the inverting input of the Current Sense comparator and the non-inverting input of the Over-current comparator, and the ADS amplifier. The current sense signal is used for cycle-by-cycle current limiting in peak current mode control, and for overcurrent protection in all cases with a secondary threshold for output shutdown. An output disable initiated by an overcurrent fault also results in a restart cycle, called "soft stop", with full soft start.

DELAB, DELCD: Delay Programming Between Complementary Outputs. DELAB programs the dead time between switching of outputs A and B, and DELCD programs the dead time between output C and D. This delay is introduced between complementary outputs in the same leg of the external bridge. The UCC3895 allows the user to select the delay, in which the resonant switching of the external power stages takes place. Separate delays are provided for the two half-bridges to accommodate differences in resonant capacitor charging currents. The delay in each stage is set according to the following formula:

$$t_{DELAY} = \frac{\left(25 \bullet 10^{-12}\right) \bullet R_{DEL}}{V_{DEL}}$$

where V_{DEL} is in Volts, and R_{DEL} is in Ohms and t_{DELAY} is in seconds. DELAB and DELCD can source about 1mA maximum. Choose the delay resistors so that this maximum is not exceeded. Programmable output delay can be defeated by tying DELAB and/or DELCD to REF. For an optimum performance keep stray capacitance on these pins at <10pF.

EAP: The non-inverting input to the error amplifier.

EAN: The inverting input to the error amplifier.

GND: Chip ground for all circuits except the output stages.

OUTA–OUTD: The 4 outputs are 100mA complementary MOS drivers, and are optimized to drive FET driver circuits. Output A and B are fully complementary, always operate up to 50% duty cycle and one-half the oscillator frequency. A and B outputs are intended to drive one half-bridge circuit in an external power stage. Outputs C and D will drive the other half-bridge and will have the same characteristics as OUTA and OUTB. Output C is phase shifted with respect to Output A, and Output D is phase shifted with respect to Output B. Note that changing the phase relationship of OUTC and OUTD with respect to OUTA and OUTB requires other than the nominal 50% duty ratio on OUTC and OUTD during those transients.

PGND: Output Stage Ground. To keep output switching noise from critical analog circuits, the UCC3895 has 2 different ground connections. PGND is the ground connection for the high-current output stages. Both GND and PGND must be electrically tied together. Also, since PGND carries high current, board traces must be low impedance.

PIN DESCRIPTIONS (cont.)

RAMP: The Inverting Input of the PWM Comparator. This pin receives either the CT waveform in voltage and average current mode controls, or the current signal (plus slope compensation) in peak current mode control.

RT: Oscillator Timing Resistor. (Refer to Fig. 1, Oscillator Block Diagram) The oscillator in the UCC3895 operates by charging an external timing capacitor, CT, with a fixed current programmed by R_T. R_T current is calculated as follows:

$$I_{RT} = \frac{3.0V}{R_T}$$

where R_T is in Ohms and I_{RT} is in Amperes. R_T can range from 40kΩ to 120kΩ Soft start charging and discharging current are also programmed by I_{RT} .

SS/DISB: Soft Start/Disable. This pin combines the 2 independent functions.

Disable Mode: A rapid shutdown of the chip is accomplished by externally forcing SS/DISB below 0.5V, externally forcing REF below 4V, or if VDD drops below the undervoltage lockout threshold. In the case of REF being pulled below 4V or an undervoltage condition, SS/DISB is actively pulled to ground via an internal MOSFET switch.

Note that if externally forcing SS/DISB below 0.5V, the pin will start to source current equal to I_{RT}.

If an overcurrent fault is sensed (CS ≥ 2.5V), a "soft stop" is initiated. In this mode, SS/DISB will sink a constant current of (10 • I_{RT}). The soft stop will continue until SS/DISB falls below 0.5V. When any of these faults are detected, all outputs are forced to ground immediately. Note that the only time the part switches into low I_{DD} current mode, though, is when the part is in undervoltage lockout.

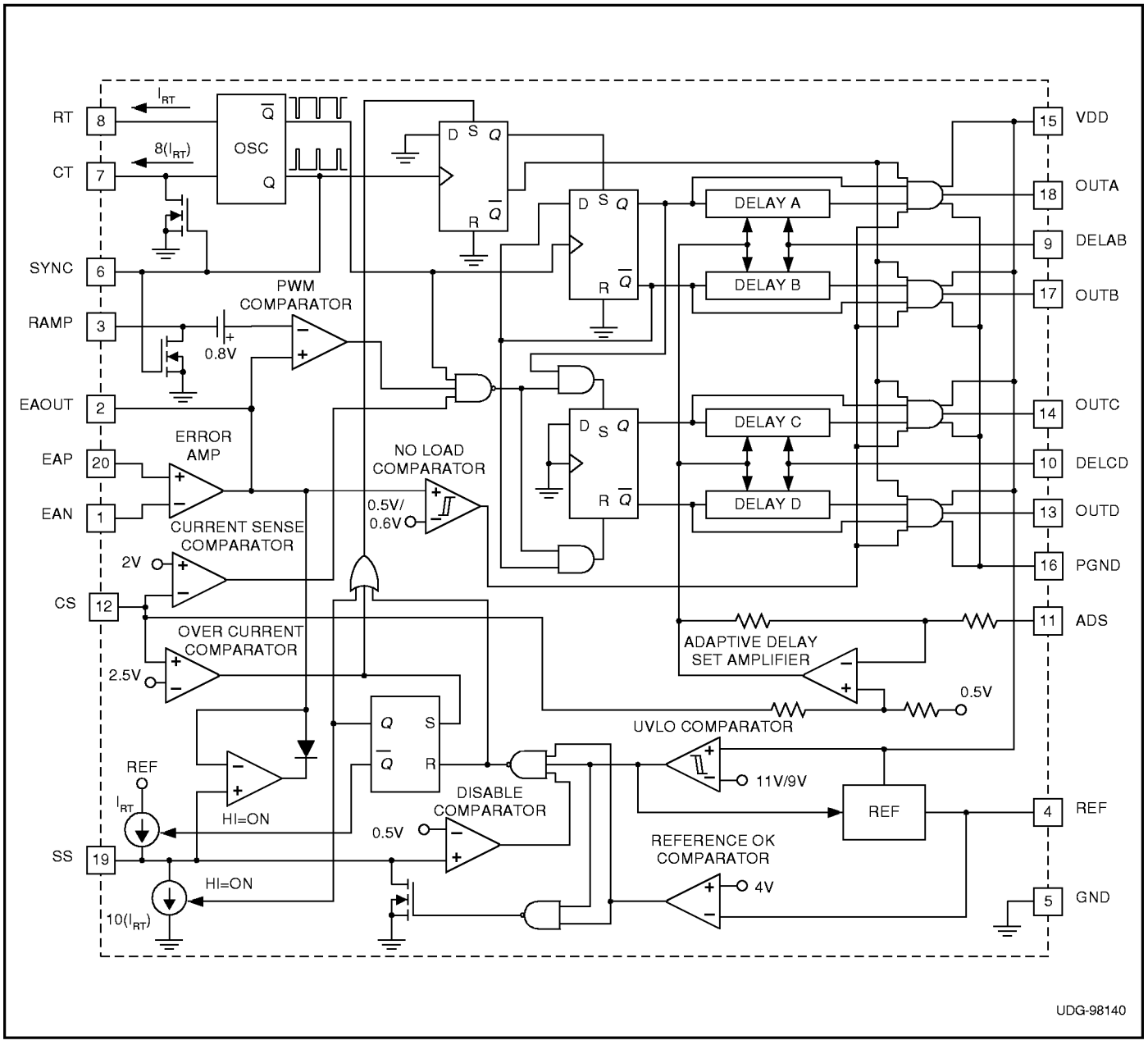
Soft Start Mode: After a fault or disable condition has passed, VDD is above the start threshold, and/or SS/DISB falls below 0.5V during a soft stop, SS/DISB will switch to a soft start mode. The pin will now source current, equal to I_{RT}. A user selected resistor/capacitor combination on SS/DISB determines the soft start time constant. Note that SS/DISB will actively clamp the EAOUT pin voltage to approximately the SS/DISB pin voltage during both soft start, soft stop, and disable conditions.

SYNC: Oscillator Synchronization. (Refer to Fig. 1, Oscillator Block Diagram) This pin is bidirectional. When used as an output, SYNC can be used as a clock, which is the same as the chip's internal clock. When used as an input, SYNC will override the chip's internal oscillator and act as it's clock signal. This bidirectional feature allows synchronization of multiple power supplies. The SYNC signal will also internally discharge the CT capacitor and any filter capacitors that are present on the RAMP pin. The internal SYNC circuitry is level sensitive, with an input low threshold of 1.9V, and an input high threshold of 2.1V.

VDD: Power Supply. VDD must be bypassed with a minimum of a 1.0μF low ESR, low ESL capacitor to ground.

REF: 5V, ±2% voltage reference. The reference supplies power to internal circuitry, and can also supply up to 5mA to external loads. The reference is shut down during undervoltage lock-out but is operational during all other disable modes. For best performance, bypass with a 0.1μF low ESR, low ESL capacitor to ground

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

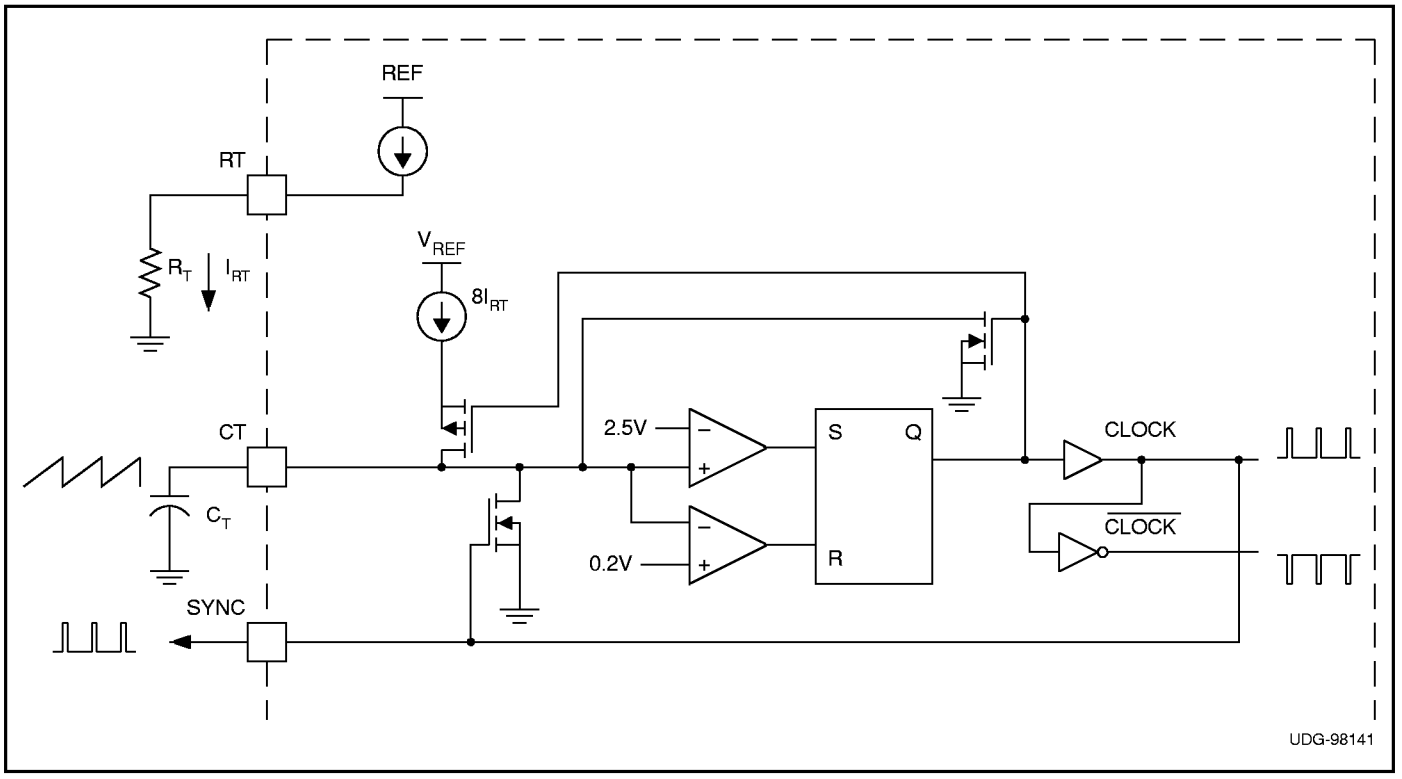


Figure 1. Oscillator block diagram.

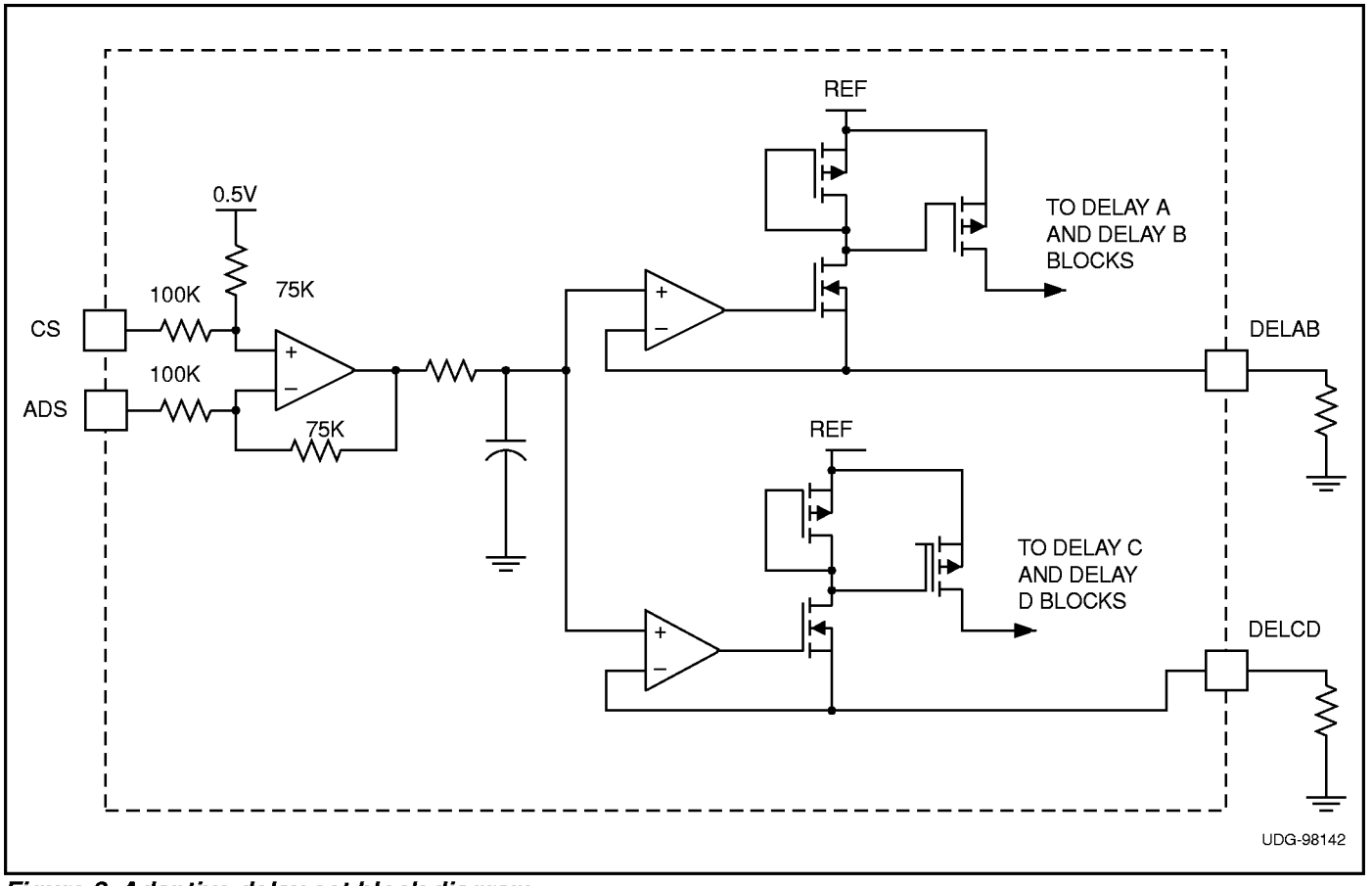


Figure 2. Adaptive delay set block diagram.

CIRCUIT DESCRIPTION (cont.)

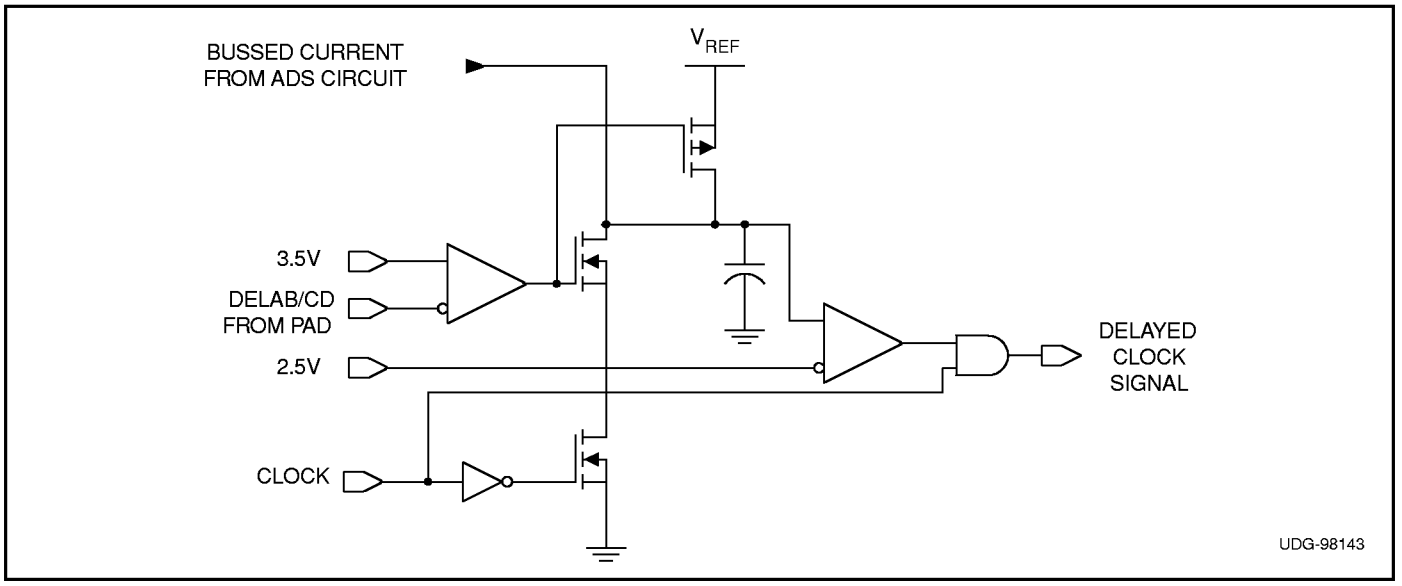


Figure 3. Delay block diagram (one delay block per output).

APPLICATION INFORMATION

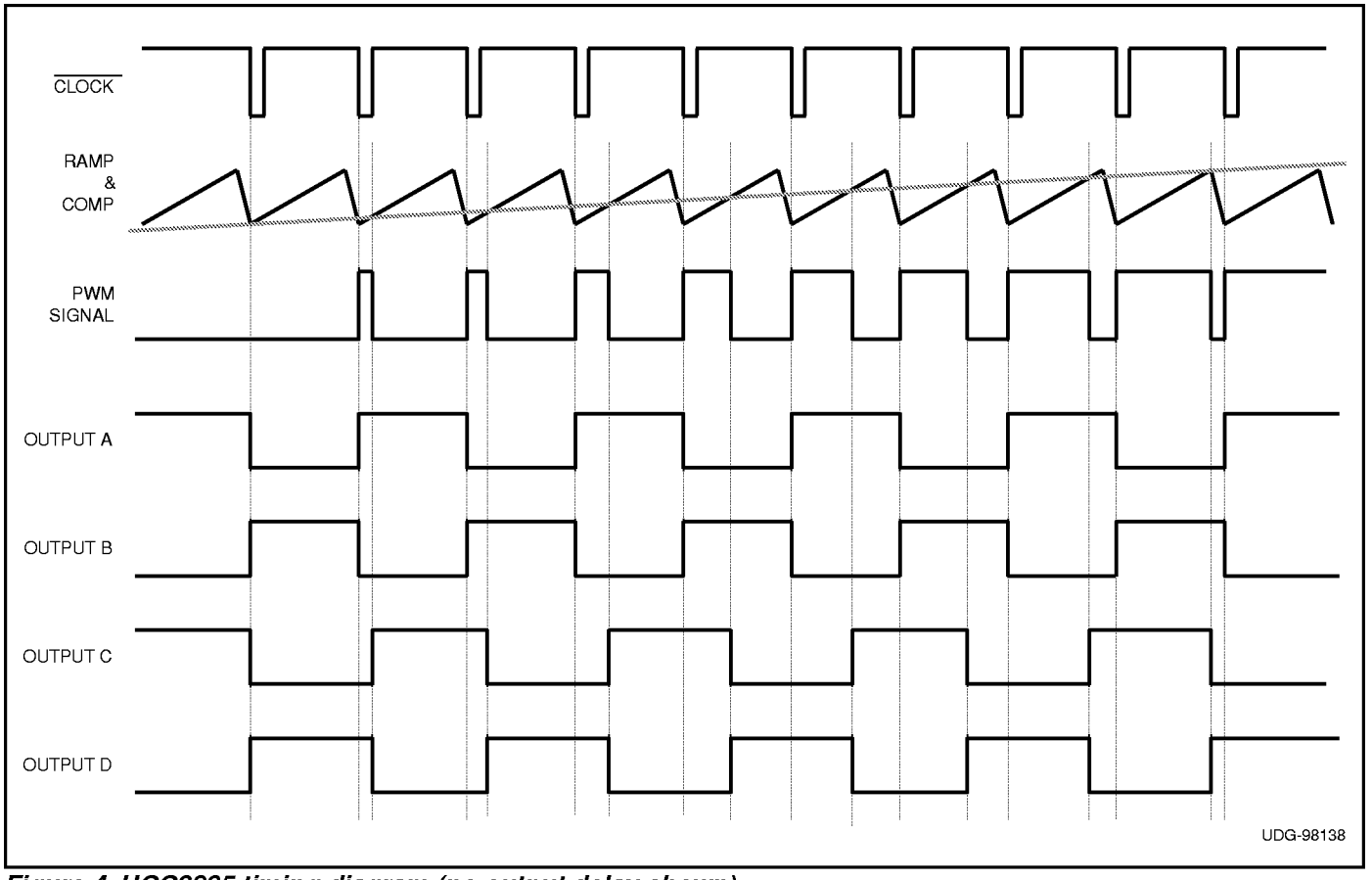


Figure 4. UCC3895 timing diagram (no output delay shown).

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