# MP8007H

## Fully Integrated, 802.3af-Compatible PoE PD Interface with 13W Primary-Side Regulated Flyback or Buck Converter

## DESCRIPTION

The MP8007H is an integrated, IEEE 802.3af-compatible, PoE-powered device with a PD interface and power converter. It is targeted for isolated or non-isolated 13W PoE applications.

The PD interface has all the functions of IEEE 802.3af, including detection, classification, 120mA inrush current, 840mA operation current limit, and a 100V hot-swap MOSFET.

The DC/DC converter uses fixed peak current and variable frequency discontinuous conduction mode (DCM) to regulate a constant output voltage. The primary-side regulation without optocoupler feedback in flyback mode simplifies the design. Buck mode minimizes the solution size for non-isolated applications. A 180V integrated power MOSFET optimizes the device for various wide-voltage applications.

The device's protection features include over-current protection, over-voltage protection, open-circuit protection and thermal shutdown.

The MP8007H can support a front-end solution for PoE-PD applications with minimal external components. It is available in a QFN-28 (4mmx5mm) package.

## FEATURES

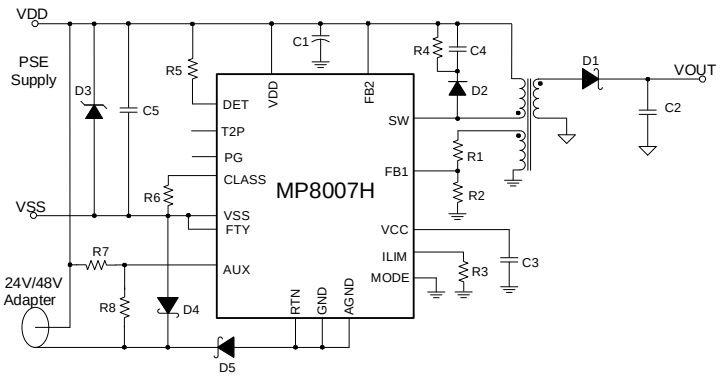
- Compatible with 802.3af Specifications
- Supports 13W PoE Power Applications
- 300KHz Maximum Switching Frequency
- 100V 0.48Ω PD Integrated Pass Switch
- 120mA PD Inrush Current
- 840mA PD Operation Current Limit
- Auxiliary Adapter ORing Power Supply
- Integrated 180V Switching Power MOSFET
- Supports Primary-Side Regulated Flyback without Optocoupler Feedback
- Supports Low-Side Switch Buck Converter
- Up to 3A Programmable Switching Current Limit
- OLP, OVP, Open-Circuit, and Thermal Protection
- Minimal External Components
- Available in a QFN-28 (4mmx5mm) Package

## APPLICATIONS

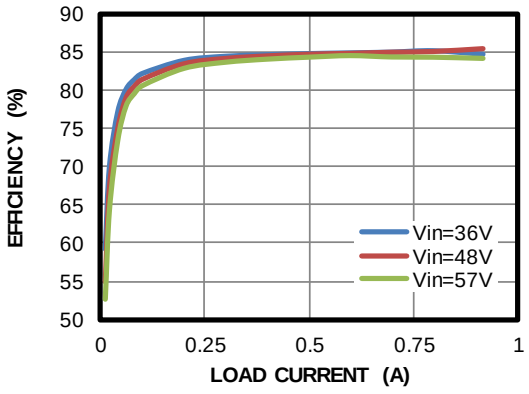
- IEEE 802.3af-Compliant Devices
- Security Cameras
- VoIP Phones
- WLAN Access Points
- IoT Devices



## TYPICAL APPLICATION




**Efficiency vs. Load Current**



## ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating |
|---|---|---|---|
| MP8007HGV | QFN-28 (4mmx5mm) | *See Below* | 2 |

* For Tape & Reel, add suffix –Z (e.g. MP8007HGV–Z).

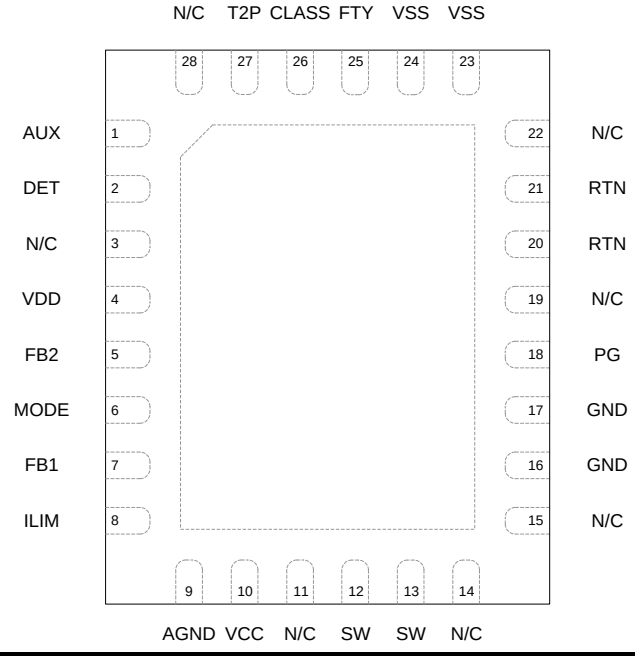
## TOP MARKING

MPSYWW
M8007H
LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M8007H: Part number
LLLLLL: Lot number

## PACKAGE REFERENCE

**TOP VIEW**




**QFN-28 (4mmx5mm)**

## PIN FUNCTIONS

| Pin # | Name | Description |
|---|---|---|
| 1 | AUX | **Auxiliary power input detector.** Use this pin for adapter power supply application. Drive VDD-AUX above 2.3V to disable the hot-swap MOSFET and CLASS pin function, and force T2P and PG to be active. |
| 2 | DET | **Connect a 24.9kΩ resistor between VDD and DET for PoE detection.** |
| 3, 11, 14, 15, 19, 22, 28 | N/C | **Not connected internally.** Can be connected to the GND pin and exposed thermal pad in the layout. |
| 4 | VDD | **Positive power supply terminal from PoE input power rail.** |
| 5 | FB2 | **Feedback pin for non-isolated buck solution.** Connect FB2 to VDD in flyback application mode. |
| 6 | MODE | **Buck mode or flyback mode select pin.** MODE is pulled up internally to VCC through a 1.5μA current source. Float MODE for buck application mode. Connect MODE to GND for flyback application mode. |
| 7 | FB1 | **Feedback for flyback solution.** Connect FB1 to GND in buck application mode. |
| 8 | ILIM | **DC/DC converter switching current limit program pin.** Connect ILIM to GND through a resistor to program the peak current limit. |
| 9 | AGND | **Analog power return for DC/DC converter control circuit.** Connect to GND through a single point. |
| 10 | VCC | **Supply bias voltage pin.** Powered through internal LDO from VIN. It is recommended to connect a capacitor (no less than 1μF) between VCC and GND. |
| 12, 13 | SW | **Drain of converter-switching MOSFET.** |
| 16, 17 | GND | **Switching converter power return.** Connect to RTN for PoE power supply. Exposed thermal pad can be connected to GND plane for heat sink. |
| 18 | PG | **PD supply power good indicator.** This signal enables the DC/DC converter internally. It is pulled up by an internal current source in output high conditions, and it is recommended to float it in application mode. |
| 20, 21 | RTN | **Drain of PD hot-swap MOSFET**. Connect the RTN pin to GND and AGND. |
| 23, 24 | VSS | **Negative power supply terminal from PoE input power rail.** |
| 25 | FTY | **Factory use only.** Connect FTY to VSS in application mode. |
| 26 | CLASS | **Connect resistor from CLASS to VSS to program the classification current.** |
| 27 | T2P | **Type 2 PSE indicator.** Open-drain output. Pull low to VSS to indicate the presence of a Type-2 PSE or when AUX is enabled. |

## ABSOLUTE MAXIMUM RATINGS (1)

***Pins Voltage Respects to VSS:*** (2)

VDD, RTN, DET, T2P, AUX, GND, AGND…….. ..... -0.3V to +100V
CLASS, FTY ..... -0.3V to +6.5V

***Pins Voltage Respects to GND:*** (2)

VDD ..... -0.3V to +100V
SW ..... -0.7V to +180V
FB1 ..... -0.7V to +6.5V (3)
VCC(4), MODE, ILIM, PG..... -0.3V to +6.5V

***Pins Voltage Respects to VDD:***

AUX, FB2..... -6.5V to +0.3V (5)

***Pins Current:***

T2P.....10mA
VCC sinking current.....1.5 mA (4)
AUX sinking current..... -5 mA (5)
FB1 sinking current.....±1 mA (3)
Continuous power dissipation ($T_A$ = 25°) (6) (8)
QFN-28 (4mmX5mm) .....3.37W
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

## *Recommended Operating Conditions* (7)

Supply voltage ($V_{DD}$) ..... 0V to 57V
Switching voltage ($V_{SW}$) ..... -0.5V to +150V
Maximum T2P current.....5mA
Maximum VCC sinking current.....1.2mA (4)
Maximum AUX sinking current.....-3mA (5)
Maximum FB1 sinking current.....±0.5 mA (3)
Maximum switching frequency .....300 kHz
Maximum switching current limit .....3A
Operating junction temp ($T_J$)…. -40°C to +125°C

## *Thermal Resistance* $\theta_{JA}$ $\theta_{JC}$

EV8007H-V-00A (4mmx5mm) (8)...37 .... 2..°C/W
QFN-28 (4mmx5mm) (9).....40 ..... 9..°C/W

**Notes:**

1) Exceeding these ratings may damage the device.
2) GND and AGND must be connected to RTN.
3) See the Converter Output Voltage Setting section on page 24.
4) VCC voltage can be pulled above this rating, but the external pull-up current should be limited. See the VCC sinking current rating above and VCC Power Supply Setting section on page 24.
5) When the VDD-to-adapter ground voltage is high, the AUX-VDD voltage may exceed -6.5V if the divider resistor is not appropriate. In this condition, the current should be limited by external resistor, see the Wall Power Adapter Detection Circuit section on page 23 for more detail.
6) The maximum allowable power dissipation is a function of the maximum junction temperature $T_J$ (MAX), the junction-to-ambient thermal resistance $\theta_{JA}$, and the ambient temperature $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
7) The device is not guaranteed to function outside of its operating conditions.
8) Measured on EV8007H-V-00A, 2-layer PCB.
9) The value of $\theta_{JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

## ELECTRICAL CHARACTERISTICS – PD INTERFACE

**VDD, CLASS, DET, T2P and RTN voltages are referred to VSS, and all other pin voltages are referred to GND. GND and RTN are shorted together. $V_{DD}$ - $V_{SS}$ = 48V, $V_{SS}$ = 0V, $R_{DET}$ = 24.9kΩ, $R_{CLASS}$ = 41.2Ω. $T_J$ = -40°C to +125°C (10), typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Detection** | | | | | | |
| Detection on | $V_{DET-ON}$ | $V_{DD}$ rising | | 1.9 | | V |
| Detection off | $V_{DET-OFF}$ | $V_{DD}$ rising | | 11 | | V |
| DET leakage current | $V_{DET-LK}$ | $V_{DET}$ = $V_{DD}$ = 57V, measure $I_{DET}$ | | 0.1 | 5 | μA |
| Bias current | | $V_{DD}$ = 10.1V, float DET pin, not in mark event, measure $I_{SUPPLY}$ | | | 12 | μA |
| Detection current | $I_{DET}$ | $V_{DD}$ = 2.5V, measure $I_{SUPPLY}$ | 96 | 99 | 102 | μA |
| | | $V_{DD}$ = 10.1V, measure $I_{SUPPLY}$ | 395 | 410 | 425 | μA |
| **Classification** | | | | | | |
| Classification stability time | | | | 90 | | μs |
| $V_{CLASS}$ output voltage | $V_{CLASS}$ | 13V < $V_{DD}$ < 21V<br>1mA < $I_{CLASS}$ < 42mA | 1.1 | 1.16 | 1.21 | V |
| Classification current | $I_{CLASS}$ | 13 ≤ $V_{VDD}$ ≤ 21V, guaranteed by $V_{CLASS}$ | | | | |
| | | $R_{CLASS}$ = 578Ω, 13V ≤ $V_{DD}$ ≤ 21V | 1.8 | 2 | 2.4 | mA |
| | | $R_{CLASS}$ = 110Ω, 13V ≤ $V_{DD}$ ≤ 21V | 9.9 | 10.55 | 11.3 | |
| | | $R_{CLASS}$ = 62Ω, 13V ≤ $V_{DD}$ ≤ 21V | 17.7 | 18.7 | 19.8 | |
| | | $R_{CLASS}$ = 41.2Ω, 13V ≤ $V_{DD}$ ≤ 21V | 26.6 | 28.15 | 29.7 | |
| | | $R_{CLASS}$ = 28.7Ω, 13V ≤ $V_{DD}$ ≤ 21V | 38.2 | 40.4 | 42.6 | |
| Classification lower threshold | $V_{CL-ON}$ | Class regulator turns on, $V_{DD}$ rising | 11.8 | 12.5 | 13 | V |
| Classification upper threshold | $V_{CL-OFF}$ | Class regulator turns off, $V_{DD}$ rising | 21 | 22 | 23 | V |
| Classification hysteresis | $V_{CL-HYS}$ | Low side hysteresis | | 0.8 | | V |
| | | High side hysteresis | | 0.5 | | |
| Mark event reset threshold | $V_{MARK-L}$ | | 4.5 | 5 | 5.5 | V |
| Max mark event voltage | $V_{MARK-H}$ | | 11 | 11.5 | 12 | V |
| Mark event current | $I_{MARK}$ | | 0.5 | 1.5 | 2 | mA |
| event resistance | $R_{MARK}$ | Two-point measure at 7V and 10V | | | 12 | kΩ |
| IC supply current during classification | $I_{IN-CLASS}$ | $V_{DD}$ = 17.5V, CLASS floating | | 220 | 300 | μA |
| Class leakage current | $I_{LEAKAGE}$ | $V_{CLASS}$ = 0V, $V_{DD}$ = 57V | | | 1 | μA |
| **PD UVLO** | | | | | | |
| VDD turn-on threshold | $V_{DD-VSS-R}$ | $V_{DD}$ rising | 35 | 37.5 | 40 | V |
| VDD turn-off threshold | $V_{DD-VSS-F}$ | $V_{DD}$ falling | 29 | 31 | 33 | V |
| VDD UVLO hysteresis | $V_{DD-VSS-HYS}$ | | 4.9 | | | V |
| IC supply current during operation | $I_{IN}$ | | | 450 | | μA |

## ELECTRICAL CHARACTERISTICS – PD INTERFACE *(continued)*

**VDD, CLASS, DET, T2P and RTN voltages are referred to VSS, and all other pin voltages are referred to GND. GND and RTN are shorted together. $V_{DD}$ - $V_{SS}$ = 48V, $V_{SS}$ = 0V, $R_{DET}$ = 24.9kΩ, $R_{CLASS}$ = 41.2Ω. $T_J$ = -40°C to +125°C (10), typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Pass Device and Current Limit** | | | | | | |
| On resistance | $R_{ON-RTN}$ | $I_{RTN}$ = 600mA | | 0.48 | | Ω |
| Leakage current | $I_{RTN-LK}$ | $V_{DD}$ = $V_{RTN}$ = 57V | | 1 | 15 | μA |
| Current limit | $I_{LIMIT}$ | $V_{RTN}$ = 1V | 720 | 840 | 920 | mA |
| Inrush current limit | $I_{INRUSH}$ | $V_{RTN}$ = 2V | | 120 | | mA |
| Inrush current termination | | $V_{RTN}$ falling | | 1.2 | | V |
| Inrush to operation mode delay | $t_{DELAY}$ | | 80 | 100 | | ms |
| Current fold-back threshold | | $V_{RTN}$ rising | | 10 | | V |
| Fold-back deglitch time | | $V_{RTN}$ rising to inrush current fold-back | | 1 | | ms |
| **T2P** | | | | | | |
| T2P output low voltage | | $I_{T2P}$ = 2mA, respect to VSS | | 0.1 | 0.3 | V |
| T2P output high leakage current | | $V_{T2P}$ = 48V | | | 1 | μA |
| **AUX** | | | | | | |
| AUX high-voltage threshold (11) | | Respect to VDD | | | -2.3 | V |
| AUX low-voltage threshold (11) | | Respect to VDD | -0.6 | | | V |
| AUX leakage current | | $V_{DD}$ - $V_{AUX}$ = 6V | | | 2 | μA |
| **PG** | | | | | | |
| PG output high voltage | | PG pin floating | | 5.5 | | V |
| Source current capability | | PG is logic high, pull down PG pin to 0V | | 30 | | μA |
| PG pull-down resistance | | PG is logic low, pull up PG pin to 1V | | 460 | | kΩ |
| PG high-level voltage to enable DC/DC converter | $V_{PG-EN-H}$ | | 3.9 | | | V |
| PG low-level voltage to disable DC/DC converter | $V_{PG-EN-L}$ | | | | 1.3 | V |
| **PD Thermal Shutdown** | | | | | | |
| Thermal shut down temperature (12) | $T_{PD-SD}$ | | | 150 | | °C |
| Thermal shutdown hysteresis (12) | $T_{PD-HYS}$ | | | 20 | | °C |

## ELECTRICAL CHARACTERISTICS – DC/DC CONVERTER

**VDD, CLASS, DET, T2P and RTN voltages are referred to VSS, and all other pin voltages are referred to GND. GND and RTN are shorted together. $V_{DD}$ - $V_{SS}$ = 48V, $V_{SS}$ = 0V, $R_{DET}$ = 24.9kΩ, $R_{CLASS}$ = 41.2Ω. $T_J$ = -40°C to +125°C (10), typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Converter Power Supply and UVLO** | | | | | | |
| Converter VDD UVLO rising threshold | $V_{DD-RTN-R}$ | PG-RTN = 5V, Test VDD-RTN | 10.5 | 11.6 | 12.8 | V |
| Converter VDD UVLO falling threshold | $V_{DD-RTN-F}$ | PG-RTN = 5V, Test VDD-RTN | 7.4 | 8.2 | 9 | V |
| VCC regulation (13) | $V_{CC}$ | Load = 0mA to 10mA | 4.8 | 5.4 | 5.9 | V |
| VCC UVLO rising threshold (13) | $V_{CC-R}$ | VDD is greater than UVLO, VCC rising | 4.3 | 4.7 | 5.1 | V |
| VCC UVLO falling threshold (13) | $V_{CC-F}$ | VDD is greater than UVLO, VCC falling | 4 | 4.5 | 4.8 | V |
| Quiescent current | $I_Q$ | $V_{FB1}$ = 2.2V, $V_{FB2}$ = VDD, test supply from VDD to VSS | | 0.87 | | mA |
| **Voltage Feedback** | | | | | | |
| FB1 reference voltage | $V_{REF1}$ | Respect to GND, $T_J$ = 25°C | 1.94 | 1.99 | 2.04 | V |
| | | Respect to GND, $T_J$ = -40°C to +125°C | 1.93 | 1.99 | 2.05 | V |
| FB1 leakage current | $I_{FB1}$ | Respect to GND, $V_{FB1}$ = 2V | | 10 | 50 | nA |
| Flyback mode DCM detect threshold on FB1 | $V_{DCM1}$ | Respect to GND | 25 | 50 | 75 | mV |
| FB1 open-circuit threshold | $V_{FB1OPEN}$ | | -90 | -60 | -20 | mV |
| FB1 OVP threshold | $V_{FB1OVP}$ | | 120% | 125% | 130% | $V_{REF1}$ |
| Minimum diode conduction time for FB1 sample | $t_{SAMPLE}$ | | 0.95 | 1.4 | 1.85 | μs |
| FB2 reference voltage | $V_{REF2}$ | Respect to VDD, $T_J$ = 25°C | -1.955 | -1.88 | -1.805 | V |
| | | Respect to VDD, $T_J$ = -40°C to +125°C | -1.96 | -1.88 | -1.8 | V |
| FB2 leakage current | $I_{FB2}$ | Respect to VDD, $V_{FB2}$ = -2V | | 10 | 50 | nA |
| Buck mode DCM detection threshold on SW | $V_{DCM2}$ | Respect to VDD | 0 | | 0.14 | V |
| **Switching Power Device** | | | | | | |
| On resistance | $R_{ON-SW}$ | $V_{CC}$ = 5.4V | | 0.8 | | Ω |
| **Current Sense** | | | | | | |
| Switching current limit | $I_{LIMIT}$ | $R_{ILIM}$ = 53.6kΩ, L = 47μH | 1.85 | 2.05 | 2.25 | A |
| Switching current leading-edge blanking time | $t_{LEB}$ | | | 450 | | ns |

## ELECTRICAL CHARACTERISTICS – DC/DC CONVERTER *(continued)*

**VDD, CLASS, DET, T2P and RTN voltages are referred to VSS, and all other pin voltages are referred to GND. GND and RTN are shorted together. $V_{DD}$–$V_{SS}$ = 48V, $V_{SS}$ = 0V, $R_{DET}$ = 24.9kΩ, $R_{CLASS}$ = 41.2Ω. $T_J$ = -40°C to +125°C (10), typical values are tested at $T_J$ = 25°C, unless otherwise noted.**

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DC/DC Converter Thermal Shutdown** | | | | | | |
| Thermal shutdown temperature (12) | $T_{SD}$ | | | 150 | | °C |
| Thermal shutdown hysteresis (12) | $T_{HYS}$ | | | 20 | | °C |

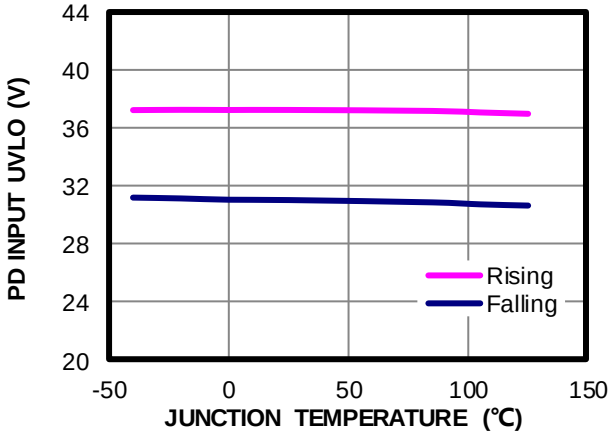
**Notes:**

10) Not tested in production. Guaranteed by over-temperature correlation.
11) If VDD - AUX > 2.3V, the IC enables adapter input. If VDD - AUX < 0.6V, the IC enables PSE input.
12) Guaranteed by characterization. Not tested in production.
13) The maximum VCC UVLO rising threshold is higher than the minimum VCC regulation in the EC table due to production distribution. However, for one unit, VCC regulation is higher than the VCC UVLO rising threshold. The VCC UVLO rising threshold is about 87% of the VCC regulation voltage, and the VCC UVLO falling threshold is about 83% of the VCC regulation voltage in one unit.

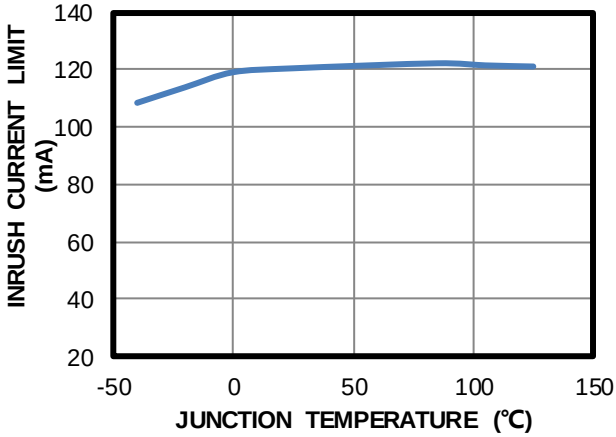
## TYPICAL CHARACTERISTICS

**$V_{IN}$ = 48V, $V_{OUT}$ = 12V, $P_{OUT}$ = 11W, $T_A$ = 25°C, unless otherwise noted.**

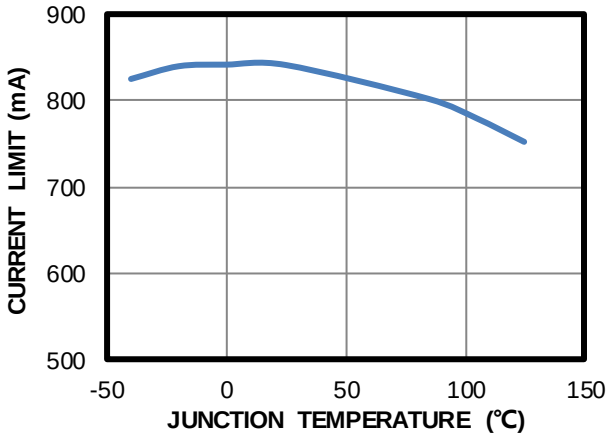
### PD Input UVLO vs. Junction Temperature




### PD Inrush Current Limit vs. Junction Temperature

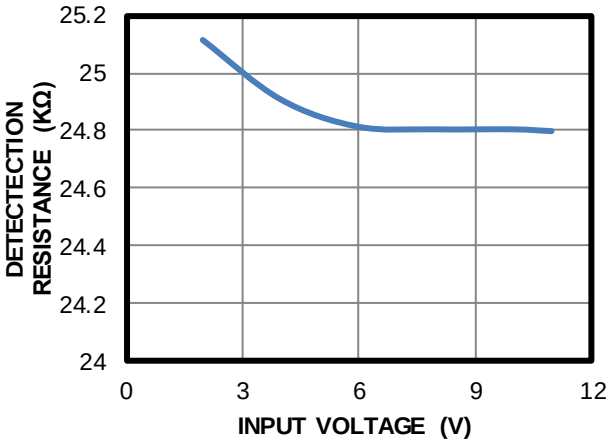



### PD Current Limit vs. Junction Temperature

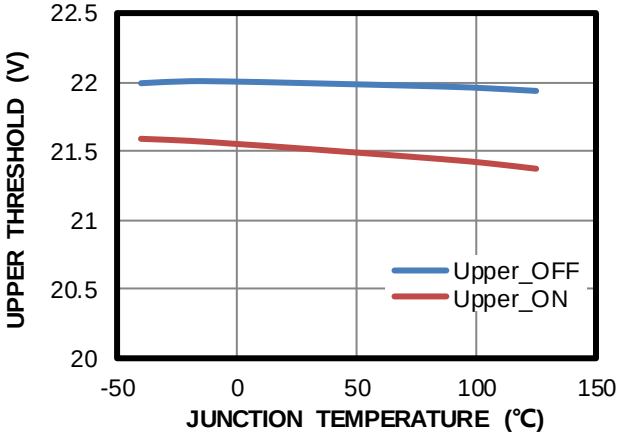



### Detection Resistance vs. Input Voltage

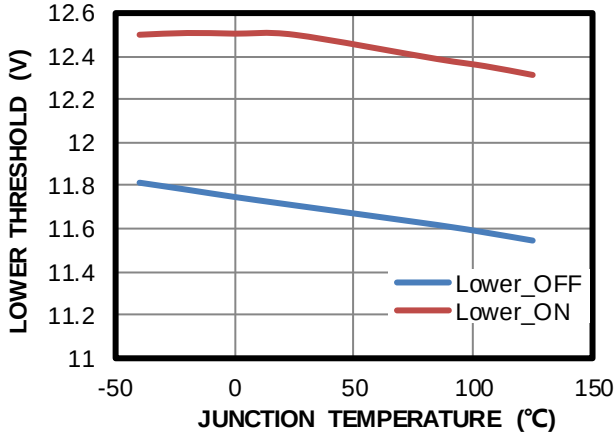
RDET = 24.9kΩ




### CLASS Upper Threshold vs. Junction Temperature



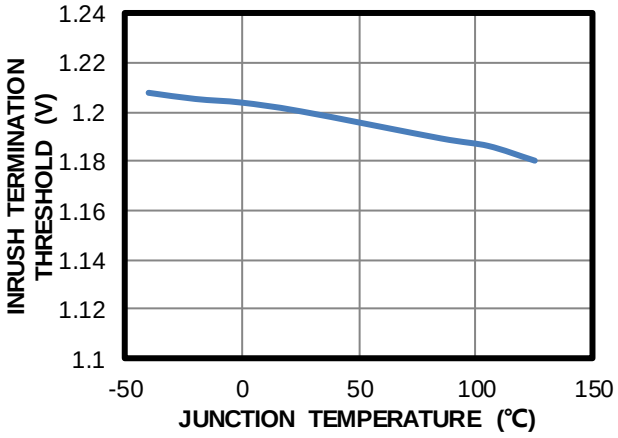

### CLASS Lower Threshold vs. Junction Temperature



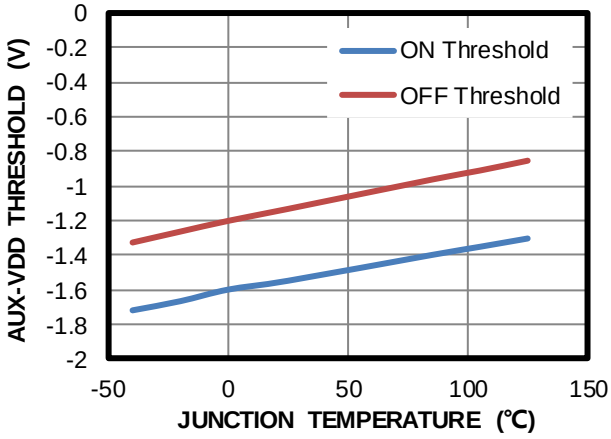
## TYPICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 48V, $V_{OUT}$ = 12V, $P_{OUT}$ = 11W, $T_A$ = 25°C, unless otherwise noted.**

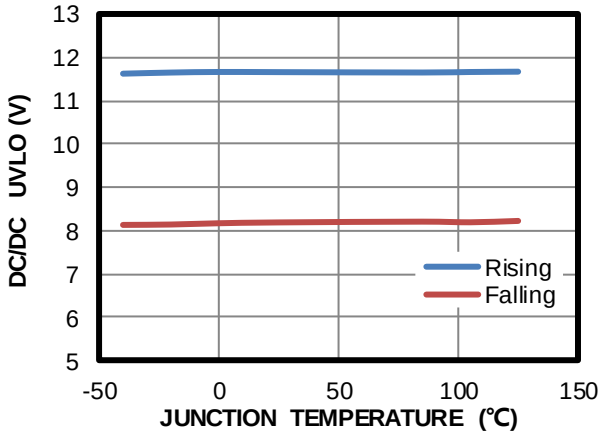
### Inrush Current Termination Threshold vs. Junction Temperature



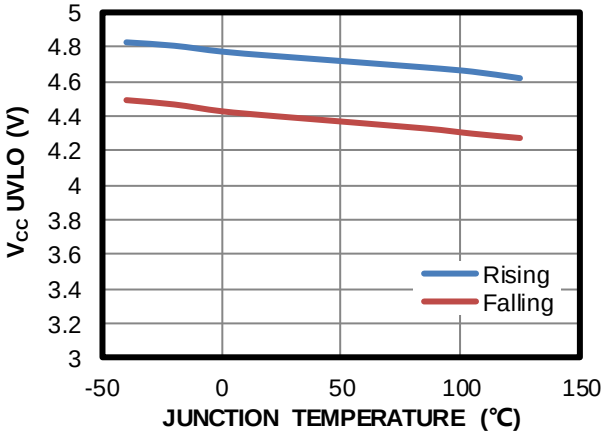

### AUX-VDD Threshold vs. Junction Temperature




### DC/DC Input UVLO vs. Junction Temperature

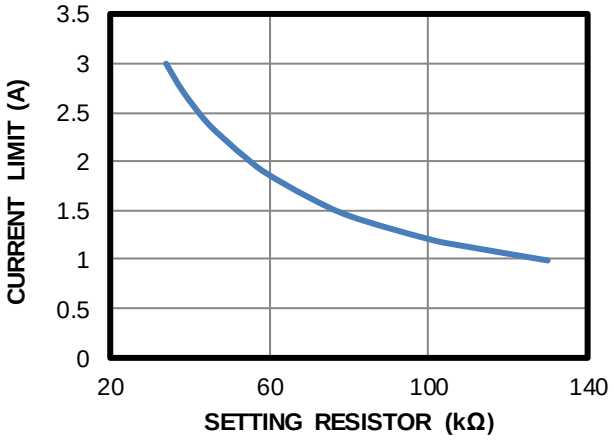



### $V_{CC}$ UVLO vs. Junction Temperature



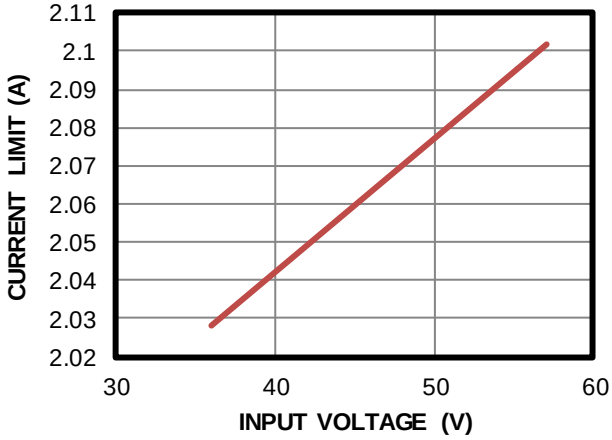

### Switching Current Limit vs. Setting Resistor

L = 47µH




### Switching Current Limit vs. Input Voltage

$R_{ILIM}$ = 53.6kΩ, L = 47µH

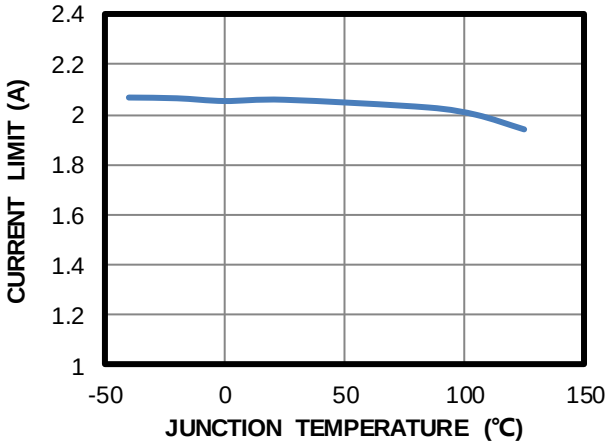


## TYPICAL CHARACTERISTICS *(continued)*

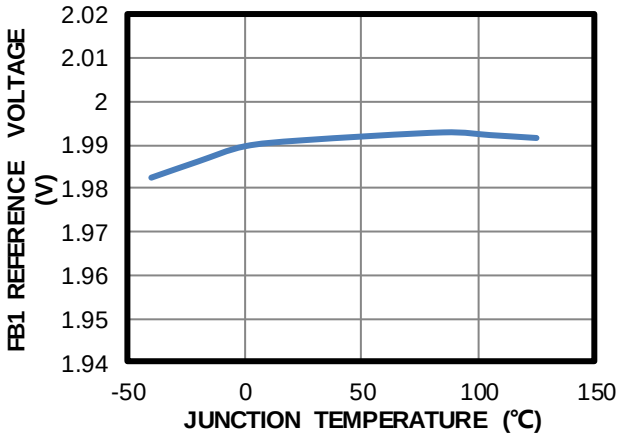
**$V_{IN}$ = 48V, $V_{OUT}$ = 12V, $P_{OUT}$ = 11W, $T_A$ = 25°C, unless otherwise noted.**

### Switching Current Limit vs. Junction Temperature

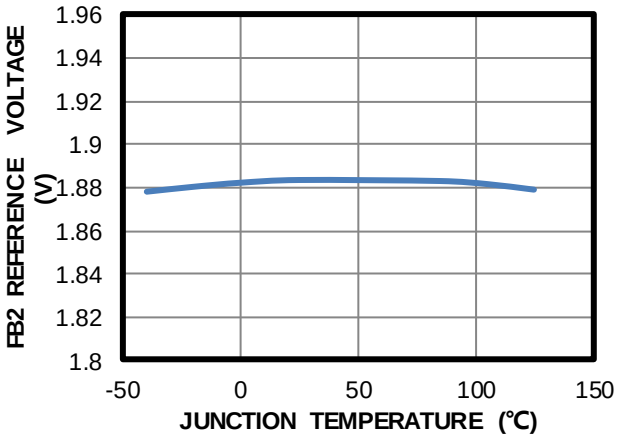
$R_{ILIM}$ = 53.6kΩ, L = 47μH




### FB1 Reference Voltage vs. Junction Temperature



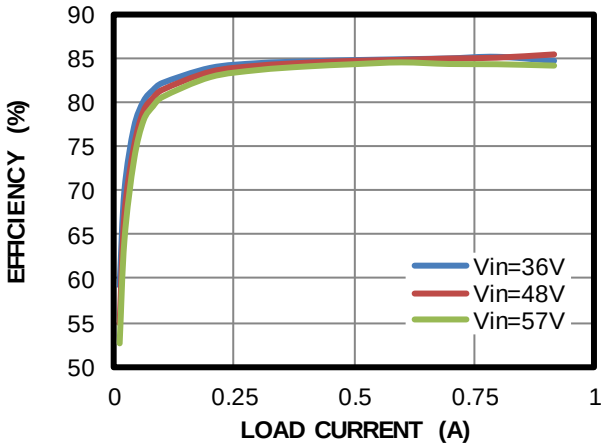

### FB2 Reference Voltage vs. Junction Temperature



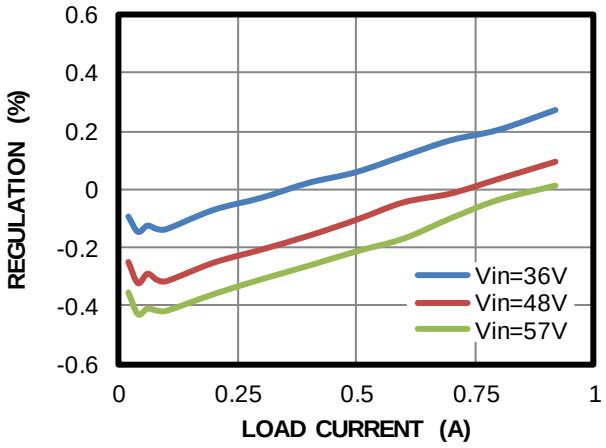
## TYPICAL PERFORMANCE CHARACTERISTICS

**$V_{IN}$ = 48V, $V_{OUT}$ = 12V, $P_{OUT}$ = 11W, $T_A$ = 25°C, unless otherwise noted.**

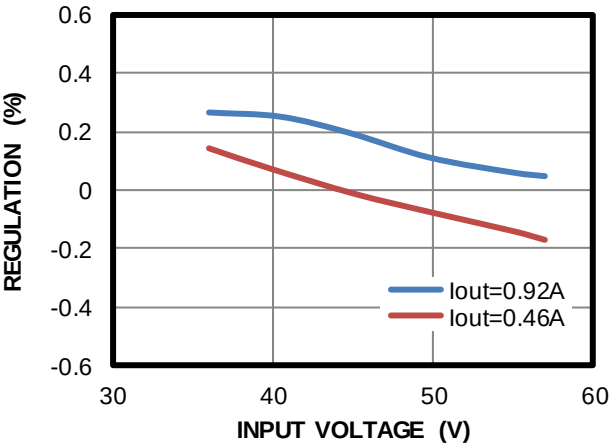
### Efficiency vs. Load Current




### Load Regulation



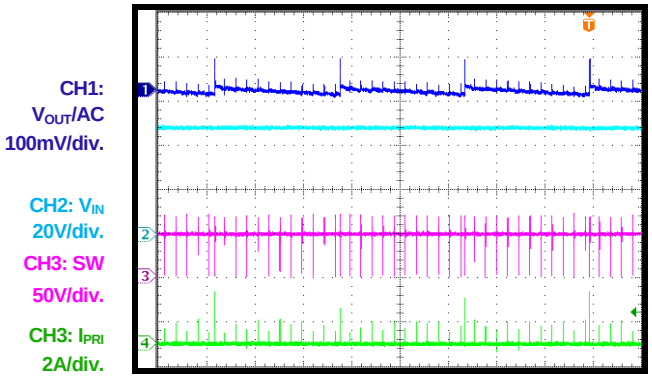

### Line Regulation



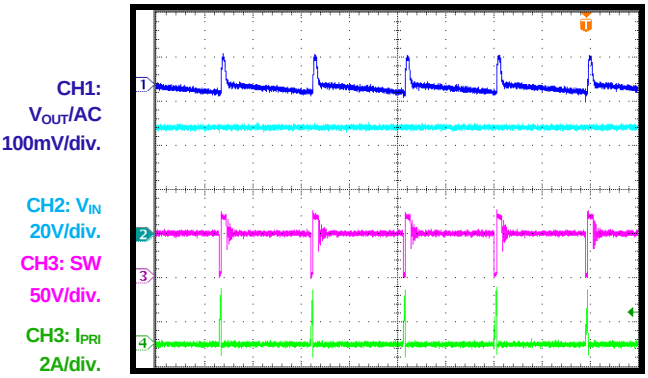
## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 48V, $V_{OUT}$ = 12V, $P_{OUT}$ = 11W, $T_A$ = 25°C, unless otherwise noted.**

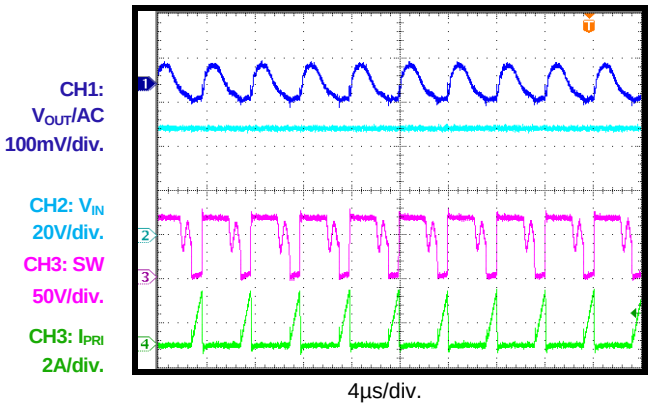
### Steady State
$I_{OUT}$ = 15mA



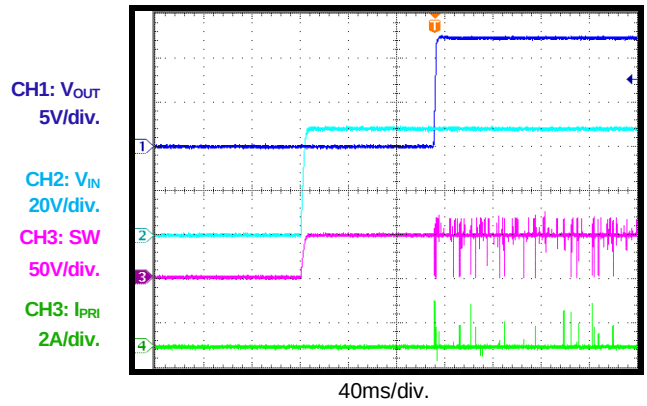

### Steady State
$I_{OUT}$ = 100mA



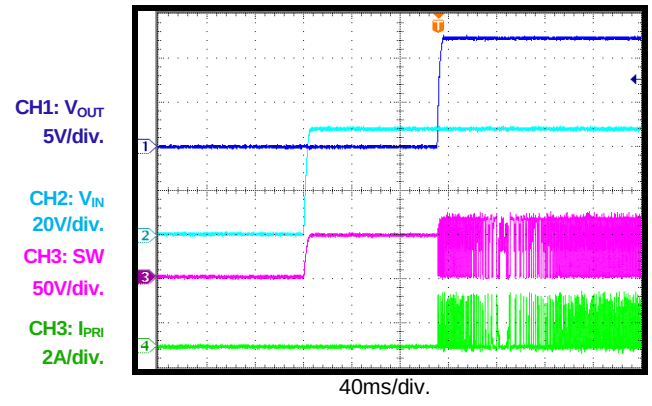

### Steady State
$I_{OUT}$ = 0.92A



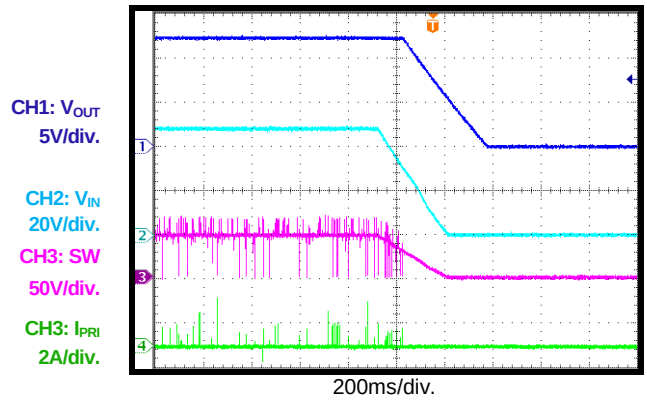

### $V_{IN}$ Start-Up
$I_{OUT}$ = 15mA




### $V_{IN}$ Start-Up
$I_{OUT}$ = 0.92A




### $V_{IN}$ Shutdown
$I_{OUT}$ = 15mA

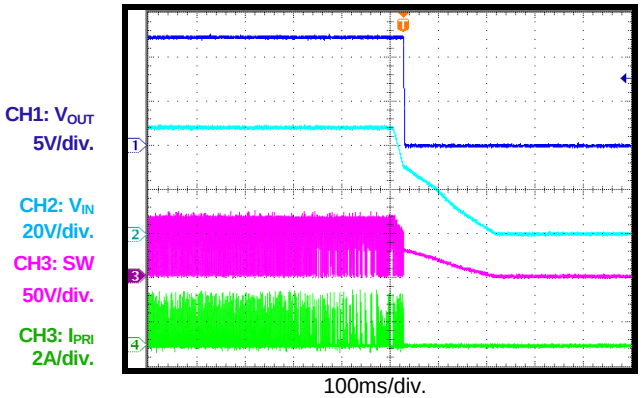


## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 48V, $V_{OUT}$ = 12V, $P_{OUT}$ = 11W, $T_A$ = 25°C, unless otherwise noted.**

### $V_{IN}$ Shutdown

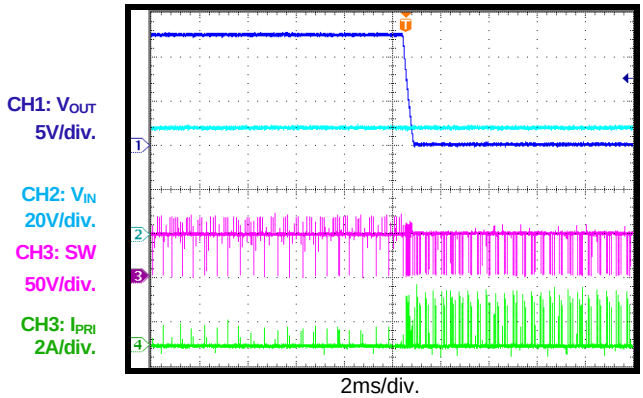
$I_{OUT}$ = 0.92A




100ms/div.

### SCP Entry

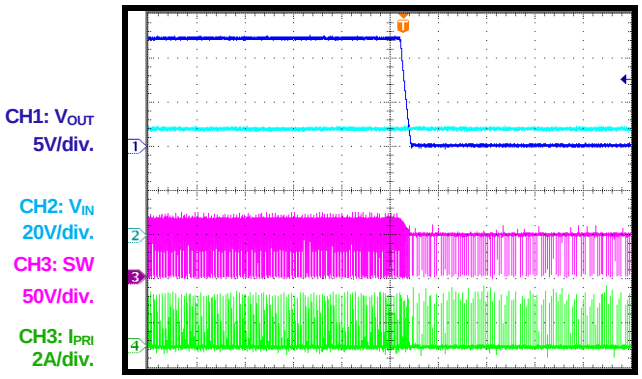
$I_{OUT}$ = 15mA to short




2ms/div.

### SCP Entry

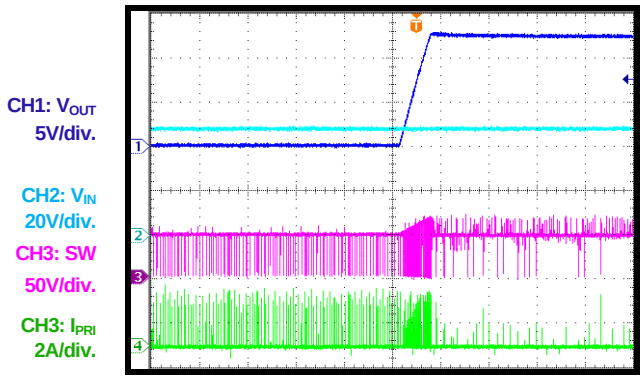
$I_{OUT}$ = 0.92A to short




2ms/div.

### SCP Recovery

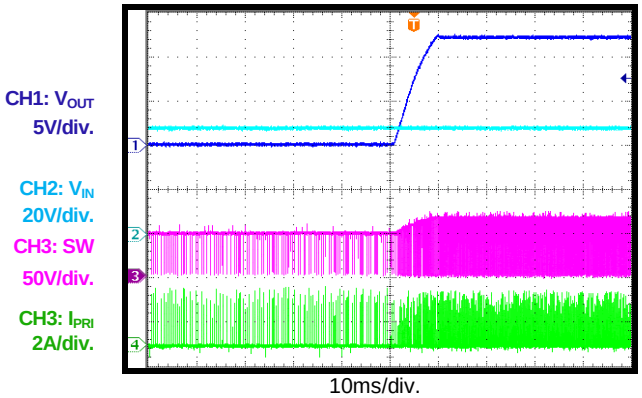
$I_{OUT}$ = short to 15mA




4ms/div.

### SCP Recovery

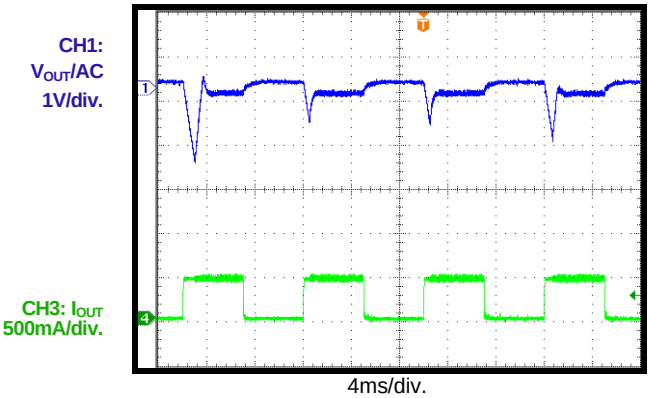
$I_{OUT}$ = short to 0.92A




10ms/div.

### Load Transient

$I_{OUT}$ = 15mA to 0.46A, $I_{RAMP}$ = 25mA/µs



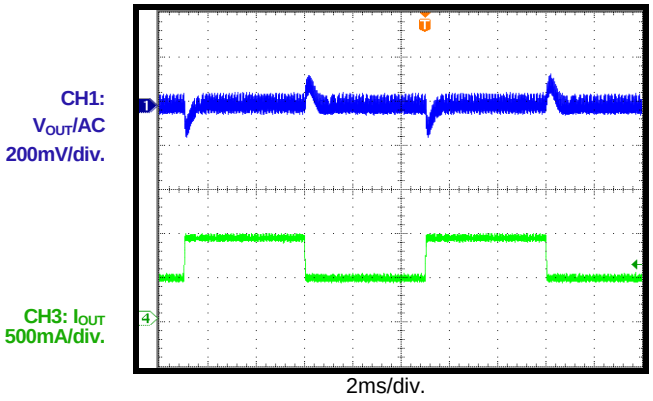

4ms/div.

## TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**$V_{IN}$ = 48V, $V_{OUT}$ = 12V, $P_{OUT}$ = 11W, $T_A$ = 25°C, unless otherwise noted.**

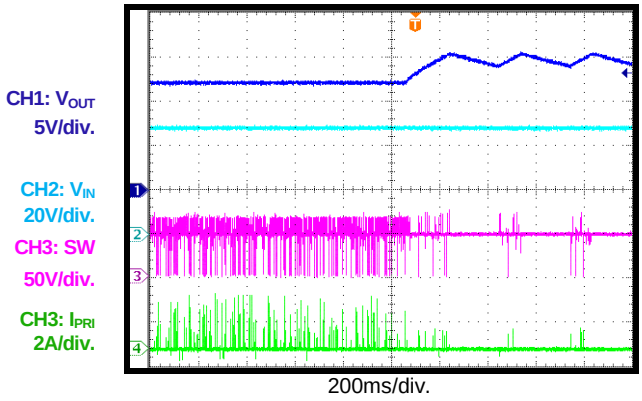
### Load Transient

$I_{OUT}$ = 0.46A to 0.92A, $I_{RAMP}$ = 25mA/µs



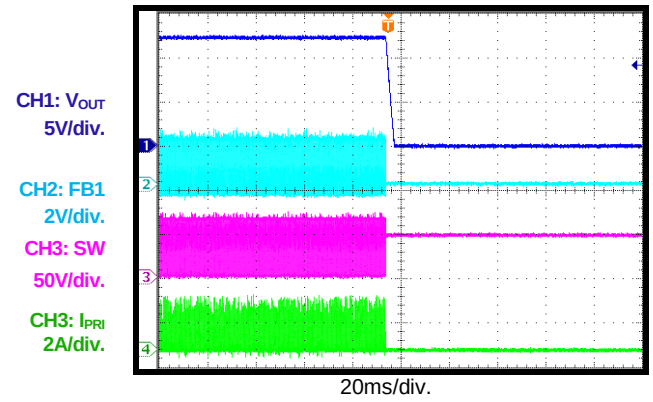

### OVP Entry

$I_{OUT}$ = 100mA to 2mA



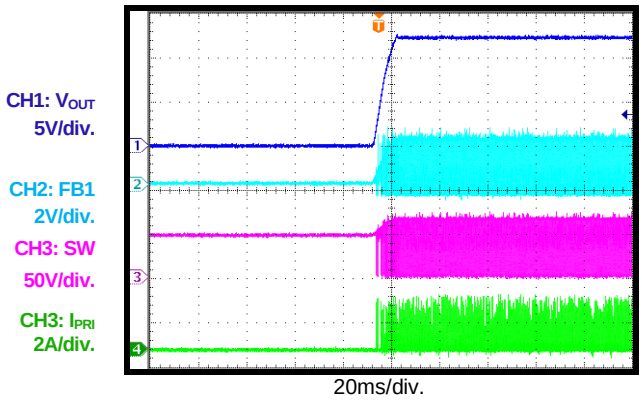

### Open-Circuit entry

$I_{OUT}$ = 0.92A, Short FB1 to GND




### Open-Circuit recovery

$I_{OUT}$ = 0.92A, release FB1 from short condition



## FUNCTIONAL BLOCK DIAGRAM

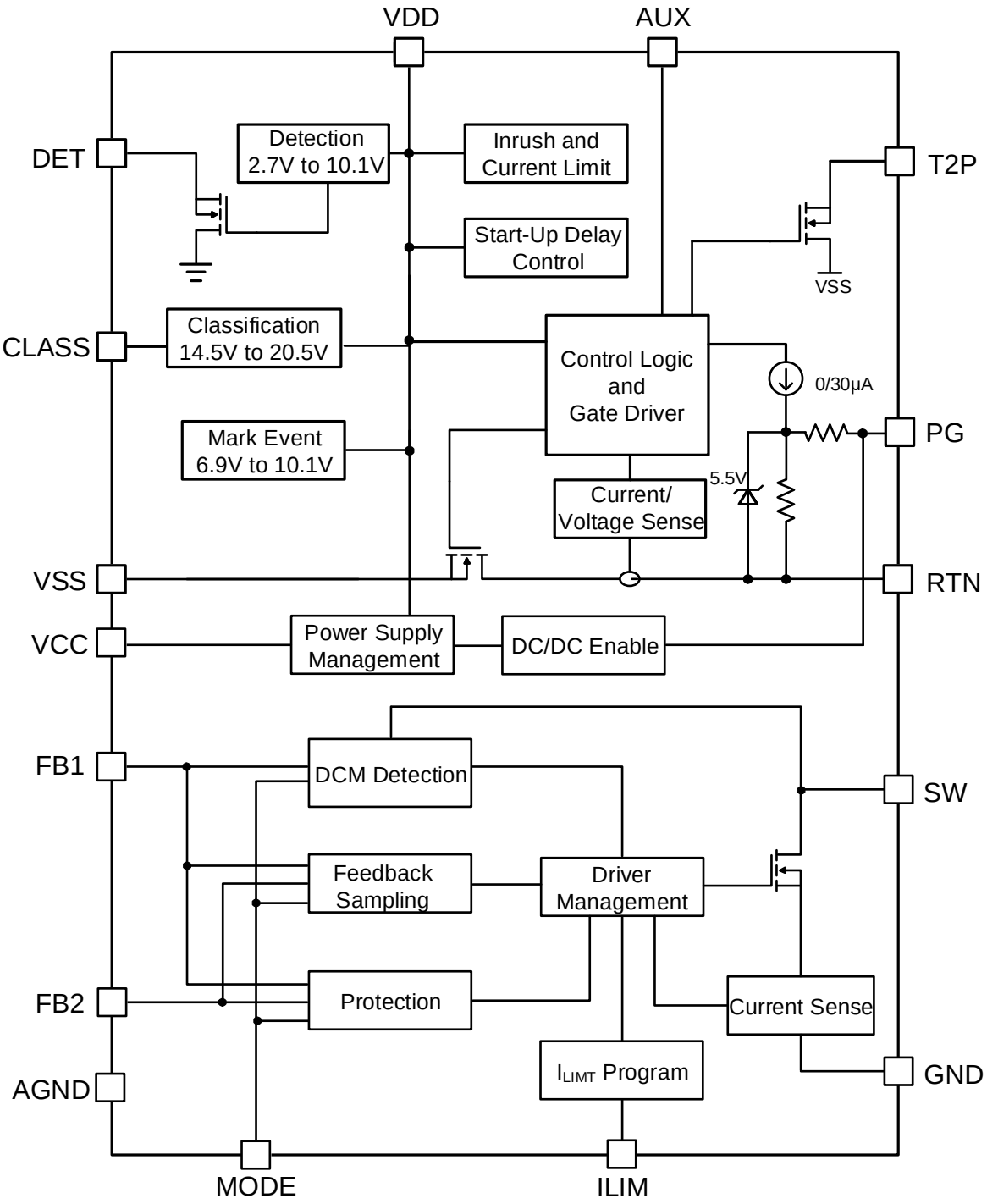



**Figure 1: Functional Block Diagram**

## OPERATION

Compared to the IEEE802.3af, the IEE802.3at standard establishes a higher power allocation for power over Ethernet (PoE) while maintaining backward compatibility with existing IEEE 802.3af systems. Power-sourcing equipment (PSE) and power devices (PD) are distinguished as Type 1 (compliant with IEEE 802.3af power levels) or Type 2 (compliant with IEEE 802.3at power levels). The IEEE 802.3af/at standard offers a method of communication between PD and PSE with detection, classification, and mark events.

The device is an integrated PoE solution with a IEEE 802.3af PD interface and a 13W DC/DC converter.

The PD interface also has 802.3at functionality, but the DC/DC converter only supports 13W output, so the MP8007H is only used for 802.3af power design.

With the PSE, the MP8007H operates as a safety device to supply voltage only when the PSE recognizes a unique, tightly specified resistance at the end of an unknown length of Ethernet cable. After being powered from the PSE, the device regulates the output voltage based on applications with isolated or non-isolated topology. Figure 1 on page 16 shows the device's functional block diagram. Figure 2 shows a typical PD interface power operation sequence.

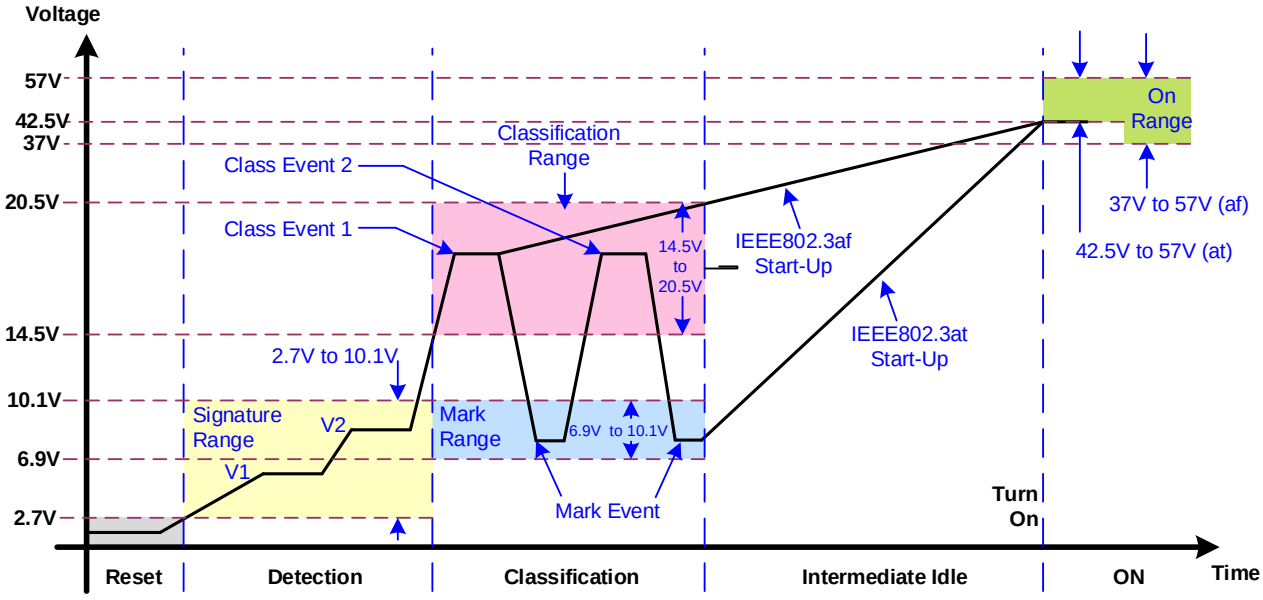



**Figure 2: PD Interface Operation Description**

### Detection

$R_{DET}$ is connected between DET and VDD. It is presented as a load to the PSE in detection mode, when the PSE applies two "safe" voltages between 2.7V and 10.1V while measuring the change in current to determine the load resistance. A 24.9kΩ (±1%) resistor between VDD and DET is recommended to present one correct signature, and the valid signature resistance seen from the power interface (PI) is between 23.7kΩ and 26.3kΩ.

The detection resistance seen from the PI is the result of the input bridge resistance in series with the VDD loading. The input bridge resistance is partially cancelled by the MP8007H's effective leakage resistance during detection.

### Classification

The classification mode can specify to the PSE the device's expected load range while under power. This allows the PSE to intelligently distribute power to as many loads as possible within its maximum current capability. The classification mode is active between 14.5V and 20.5V. Table 1 shows the different classes.

**Table 1: CLASS Resistor Selection**

| Class | Max Input Power to PD (W) | Classification Current (mA) | $R_{CLASS}$ (Ω) |
|---|---|---|---|
| 0 | 12.95 | 2 | 578 |
| 1 | 3.84 | 10.55 | 110 |
| 2 | 6.49 | 18.7 | 62 |
| 3 | 12.95 | 28.15 | 41.2 |
| 4 | 25.5 | 40.4 | 28.7 |

### Two-Event Classification

The MP8007H can be used as a Type 1 PD as Class 0 to 3 (see Table 1). It also distinguishes Class 4 with two-event classification. It is recommended to set the MP8007H in Classes 0 to 3 because the DC/DC converter is not built for more than 13W of power.

In two-event classification, the Type 2 PSE reads the power classification twice. Figure 2 on page 17 shows an example of two-event classification. The first classification event occurs when the PSE presents a voltage between 14.5V and 20.5V to the MP8007H, and the device presents a Class 4 load current. The PSE then drops the input voltage into the mark voltage range of 6.9V to 10.1V, signaling the first mark event. The MP8007H presents a load current between 0.5mA to 2mA in the mark event voltage range.

The PSE repeats this sequence, signaling the second classification and second mark event. The PSE then applies power to the MP8007H, and the device charges up the DC/DC input capacitor $C_{BULK}$ (C1 in the Typical Application Circuit on page 1) with a controlled inrush current. When $C_{BULK}$ is fully charged, the T2P pin presents an active low signal with respect to VSS after $t_{DELAY}$. The T2P output becomes inactive when the MP8007H input voltage ($V_{DD}$) falls below UVLO (see Figure 3). When the MP8007H is set to Classes 0 through 3, two-event classification and T2P can be ignored.

### PD Interface UVLO and Current Limit

When PD is powered by the PSE and $V_{DD}$ exceeds the turn-on threshold, the hot-swap switch start passes a limited current ($I_{INRUSH}$) to charge the downstream DC/DC converter's input capacitor ($C_{BULK}$). The start-up charging current is about 120mA.

If RTN drops below 1.2V, the hot-swap current limit changes to 840mA. After $t_{DELAY}$ from UVLO starting, the MP8007H asserts a PG signal and goes from start-up mode to running mode. If the inrush period elapses, the PG signal can internally enable the downstream DC/DC converter.

If $V_{DD}$ - $V_{SS}$ drops below the falling UVLO, the hot-swap MOSFET and DC/DC converter are both disabled.

If the output current overloads on the internal pass MOSFET, the current limit works and $V_{RTN}$ - $V_{SS}$ rises. If $V_{RTN}$ rises above 10V for longer than 1ms, or rises above 20V, the current limit reverts to the inrush value, and PG is pulled down internally to disable the DC/DC regulator.

Figure 3 shows the current limit, and the PG and T2P work logic during start-up from the PSE power supply.

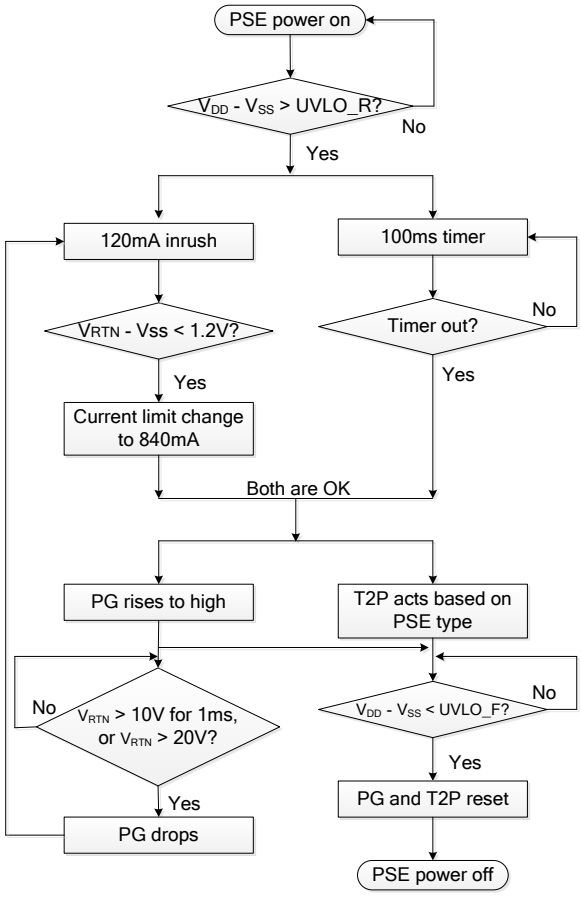



**Figure 3: Start-Up Sequence**

### Wall Power Adapter Detection and Operation

For applications where an auxiliary power source such as a wall adapter powers the device, the MP8007H features wall power adapter detection (see Figure 4). Once the input voltage ($V_{DD}$ - $V_{SS}$) exceeds about 11.5V, the device enables wall adapter detection. The wall power adapter detection resistor divider is connected from VDD to the negative terminal of the adapter, and $D_{ADP3}$ is added for a more accurate hysteresis. There is a -2.3V reference voltage from AUX to VDD for adapter detection. The adapter is detected when the AUX voltage ($V_{AUX}$) triggers, calculated with Equation (1):

$$V_{DD} - V_{AUX} = (V_{ADP} - V_{DADP3}) \times \frac{R_{ADPUP}}{R_{ADPUP} + R_{ADPDOWN}} > 2.3V \quad (1)$$

Where $V_{ADP}$ is the adapter voltage, $V_{DADP3}$ is the Zener voltage, and $R_{ADPUP}$ and $R_{ADPDOWN}$ are the AUX divider resistors from the adapter power.

If the applied adapter voltage exceeds the design adapter voltage, $V_{DD}$ - $V_{AUX}$ is high. If the applied voltage between VDD and AUX exceeds 6.5V, some current may flow out through the AUX pin. Design the external resistor ($R_{ADPUP}$/$R_{ADPDOWN}$ or the RT resistor from the resistor divider to AUX) to limit the AUX pin's current. Assuming $V_{DD}$ - $V_{AUX}$ is 6.5V for the calculation, the current out of the AUX pin should be below 3mA by the external resistor limit.

To ensure the MP8007H works stably with adapter power, place one Schottky diode ($D_{APD1}$) (D4 in Typical Application Circuit on page 1) between the negative terminal of the adapter and VSS. $D_{APD2}$ (D5 in Typical Application Circuit on page 1) blocks the reverse current between the adapter and the PSE power source.

When a wall adapter is detected, the internal MOSFET between RTN and VSS turns off, classification current is disabled, and T2P activates. The PG signal is active when adapter power is detected, so that it can enable the downstream DC/DC converter even when the input hot-swap MOSFET is disabled.

Internal T2P and PG signals only work with input voltages exceeding 11.5V when an adapter is detected.

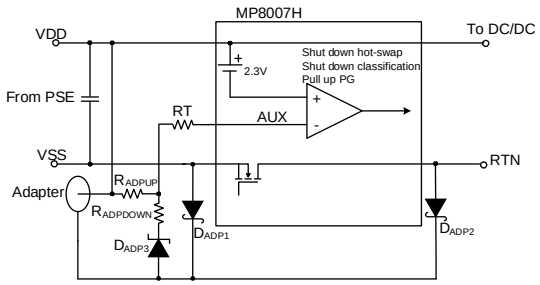



**Figure 4: Adapter Power Detection**

### Power Good Indicator (PG)

The PG signal is driven by the internal current source. After $t_{DELAY}$, when UVLO starts and RTN drops to 1.2V, or a wall power adapter is detected, the PG signal is pulled high to indicate the power condition and enable the downstream DC/DC converter. Figure 3 shows that when powering the PG logic from the PSE, PG will be high if an adapter is detected.

### DC/DC Converter Start-Up and Power Supply

Once the PD input overrides its UVLO, it charges the DC/DC converter's input capacitor (between VDD and RTN) with PD inrush current limit.

The DC/DC converter has an internal start-up circuit. When the voltage between VDD and GND exceeds 4.3V, the capacitor at VCC is charged through the internal LDO. Typically, $V_{CC}$ is regulated at 5.4V (if VDD is high enough). With the exception of the PD interface UVLO, the DC/DC converter has an additional $V_{IN}$ UVLO (11.6V) and $V_{CC}$ UVLO (4.7V). When VDD - GND exceeds the 11.6V UVLO, $V_{CC}$ is charged above the 4.7V UVLO. The PG pin is pulled high by the PD interface, and the DC/DC converter starts switching.

The VCC pin can be powered from the transformer auxiliary winding to save IC power loss (see the VCC Power Supply Setting section on page 24 for more details).

### Flyback and Buck Mode Converter

The DC/DC converter supports both flyback and buck topology applications. Connect MODE to GND to set the DC/DC converter in flyback mode. Float MODE to set the DC/DC converter in buck mode. MODE is pulled up internally to VCC through a 1.5μA current source. Do not connect MODE to VDD externally in buck

mode,and do not place a resistor between MODE and GND in flyback mode.

### Converter Switching Work Principle

After start-up, the DC/DC converter works in discontinuous conduction mode (DCM). The second switching cycle does not start until the inductor current drops to 0A. In each cycle, the internal MOSFET turns on, and the current-sense circuit senses the current ($I_{P(t)}$) internally.

The rate at which the current rises linearly in flyback mode can be calculated with Equation (2):

$$\frac{dI_{P(t)}}{dt} = \frac{V_{IN}}{L_M} \quad (2)$$

When $I_{P(t)}$ rises up to $I_{PK}$, the internal MOSFET turns off (see Figure 5). The energy stored in the primary-side inductance transfers to the secondary side through the transformer.

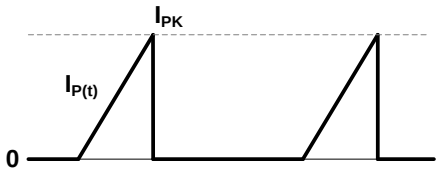



**Figure 5: Primary-Side Current Waveform**

The primary-side inductance ($L_M$) stores energy in each cycle. The energy can be calculated with Equation (3):

$$E = \frac{1}{2} L_M I_{PK}^2 \quad (3)$$

The power transferred from the input to the output can be estimated with Equation (4):

$$P = \frac{1}{2} L_M I_{PK}^2 f_{SW} \quad (4)$$

Where $f_{SW}$ is the switching frequency. When $I_{PK}$ is constant, the output power depends on $f_{SW}$ and $L_M$.

The rate at which the current rises linearly in buck mode can be estimated with Equation (5):

$$\frac{dI_{P(t)}}{dt} = \frac{V_{IN} - V_{OUT}}{L_M} \quad (5)$$

The internal MOSFET turns off when $I_{P(t)}$ rises to $I_{PK}$ (see Figure 6). The output current can be calculated with Equation (6):

$$I_{OUT} = \frac{1}{2} D I_{PK} \quad (6)$$

Where D is the inductor current conducting duty cycle.

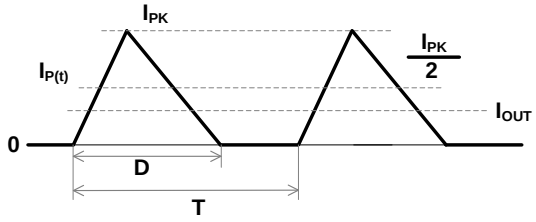



**Figure 6: Inductor Current Waveform**

### Converter Light-Load Control

If the load decreases in flyback mode, the DC/DC converter stretches down the frequency automatically to reduce the power transferred while maintaining $I_{PK}$ in each cycle. An approximate 10kHz minimum frequency is applied to detect the output voltage, even at a light load. During this condition, the switching $I_{PK}$ jumps between 20% and 100% of the normal $I_{PK}$ to reduce power loss while transferring.

Due to the 10kHz minimum frequency, the DC/DC converter still transfers some energy to the output, even if there is no load on the output. Some load is required to keep the output voltage in regulation, or else $V_{OUT}$ rises and triggers OVP.

In buck mode, the DC/DC converter does not have a minimum frequency limit, so it stretches down to a very low frequency and regulates the output automatically, even if there is no load on the output.

### Frequency Control

By monitoring the auxiliary winding voltage in flyback mode or monitoring the SW voltage in buck mode, the DC/DC converter detects and regulates the inductor current in DCM. The frequency is controlled by the peak current, the current ramp slew rate, and the load current.

The maximum frequency occurs when the DC/DC converter runs in critical conduction mode, providing the maximum load power. The DC/DC converter switching frequency must be below 300kHz in the design.

### Output Voltage Control

In flyback application mode, the DC/DC converter detects the auxiliary winding voltage from FB1 during the secondary-side diode conduction period.

Assume the secondary winding is the master, and the auxiliary winding is the slave. When the secondary-side diode conducts, the FB1 voltage can be calculated with Equation (7):

$$V_{FB1} = \frac{N_A}{N_S} \times (V_{OUT} + V_{D1F}) \times \frac{R_2}{R_1 + R_2} \quad (7)$$

Where $V_{D1F}$ is the output diode forward-drop voltage, $V_{OUT}$ is the output voltage, $N_A$ and $N_S$ are the turns of the auxiliary winding and the secondary-side winding, respectively, and R1 and R2 are the resistor dividers for sampling.

The output voltage differs from the secondary-winding voltage due to the current-dependent diode forward voltage drop. If the secondary-winding voltage is always detected at a fixed secondary current, the difference between the output voltage and the secondary-winding voltage is a fixed $V_{D1F}$.

The DC/DC converter samples the auxiliary-winding voltage for 0.48µs after the internal power MOSFET turns off. It finishes the sampling after the secondary-side diode conducts for 1.85µs. This provides good regulation when the load changes. It is recommended to make the secondary diode conducting period longer than 2µs in each cycle for some margin, and the FB1 signal must be smooth within 0.48µs of the switch turning off.

With a buck solution, there is one FB2 pin referred to VDD. It can be used as the reference voltage for the buck application. The output voltage is referred to VDD and does not have the same GND as the input power.

### Programming the Switching Current Limit

The switching converter current limit is set by an external resistor (R3 on the Typical Application Circuit on page 1) from ILIM to ground. The value of R3 can be estimated with Equation (8):

$$I_{LIM} = \frac{100}{R3} + \frac{V_L \times 0.18}{L} \quad (8)$$

Where $I_{LIM}$ is the current limit (in A), $V_L$ is the voltage applied on the inductor when the MOSFET turns on, R3 is the setting resistor in (kΩ), and L is the inductor in (µH).

The current limit cannot be programmed higher than 3A.

If the input voltage is low, the inductor current may increase slowly, and it may take a long time to meet the setting current limit. The MP8007H uses a maximum on time of about 7µs. After the max on time, the MOSFET turns off, even if the inductor current does not meet the setting current limit.

### Converter Leading-Edge Blanking

Transformer parasitic capacitance induces a current spike on the power-switching FET when the power switch turns on. The DC/DC converter includes a 450ns leading-edge blanking period to avoid falsely terminating the switching pulse. During this blanking period, the current-sense comparator is disabled, and the gate driver cannot switch off.

### DC/DC Converter DCM Detection

The DC/DC switching regulator operates in discontinuous conduction mode in both flyback and buck modes.

In flyback mode, the DC/DC converter detects the falling edge of the FB1 voltage in each cycle. The second switching cycle does not start unless the chip detects a 50mV falling edge on FB1.

In buck mode, the DC/DC converter detects the falling edge of the SW voltage in each cycle. The second switching ycle does not start unless the chip detects a 0.14V falling edge between $V_{SW}$ and $V_{DD}$.

### Over-Voltage and Open-Circuit Protection

In flyback mode, the DC/DC converter includes over-voltage protection (OVP) and open-circuit protection. If the voltage at FB1 exceeds 125% of $V_{REF1}$, or FB1's -60mV falling edge cannot be detected because the feedback resistor is removed, the DC/DC converter immediately shuts off the driving signal and enters hiccup mode by recharging the internal capacitor.

The DC/DC converter resumes normal operation when the fault is removed. In buck

mode, if the voltage at FB2 exceeds the reference voltage, the DC/DC converter stops switching immediately.

### Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from thermally running away. The MP8007H has separate temperature monitor circuits for the PD and switching devices. DC/DC converter thermal protection does not affect the PD interface, but PD temperature protection turns off both the PD and the DC converter. When the temperature drops below its recovery threshold, thermal shutdown completes and the chip is enabled.

# APPLICATION INFORMATION

### Detection Resistor

In detection mode, it is required to connect a resistor between the DET and VDD pins as a load to the PSE. The resistance is calculated as ΔV / ΔI, with an acceptable range of 23.7kΩ to 26.3kΩ. A typical value for the detection resistor is 24.9kΩ.

### Classification Resistor

To distribute power to as many loads as possible from the PSE, a resistor placed between the CLASS and VSS pins classifies the PD power level. This draws a fixed current set by the classification resistor. The power supplied to PD is also set by the classification resistor (see Table 1 on page 18). The typical voltage on the CLASS pin is 1.16V in the classification range, and it produces about 33mW of power loss on a class resistor in a Class 3 condition.

### Protection TVS

To limit input transient voltage within the absolute maximum rating, a TVS across the rectified voltage ($V_{DD}$ - $V_{SS}$) must be used. The SMAJ58A, or a similar equivalent, is recommended for general indoor applications. Outdoor transient levels or special applications require additional protection.

### PD Input Capacitor

An input bypass capacitor (from VDD to VSS) of 0.05μF to 0.12μF is needed for IEEE 802.3af/at standard specification. Typically, a 0.1μF, 100V ceramic capacitor is used.

### Wall Power Adapter Detection Circuit

When an auxiliary power source such as a wall power adapter powers the device, the divider resistors $R_{ADPUP}$, $R_{ADPDOWN}$, and $D_{ADP3}$ must be chosen to satisfy Equation (1) for correct wall power adapter detection (see Figure 7).

It is recommended to make $R_{ADPUP}$ 3kΩ to balance the power loss and current leakage discharge from $D_{ADP1}$ and $D_{ADP2}$. The RT resistor is applied to limit the AUX current below 3mA when $V_{ADP}$ is high. The minimum RT resistor can be calculated with Equation (9):

$$RT = \frac{\frac{(V_{ADP} - V_{DADP3}) \times R_{ADPUP}}{R_{ADPUP} + R_{ADPDOWN}} - 6.5}{3} \quad (9)$$

Where RT is in kΩ.

One small package Schottky diode with a 100V voltage rating (such as BAT46W) is recommended for $D_{ADP1}$. The voltage rating of $D_{ADP2}$ must also be above 100V, while the current rating must be above the load current. A low-voltage drop Schottky diode (such as the SS1H10) is recommended to reduce conduction power loss.

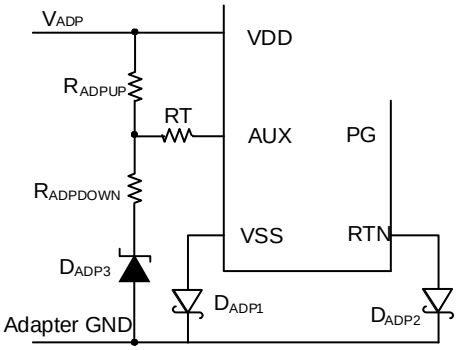



**Figure 7: Wall Power Adapter Detection Circuit**

To prevent the converter from operating at an excessively low adapter voltage, choose a start-up voltage ($V_{START}$) about 80% of the nominal voltage. Assuming that the adapter voltage is 48V, let $R_{ADPUP}$ = 3kΩ, $R_{ADPDOWN}$ = 8.06kΩ and $D_{ADP3}$ = 30V. For more details, see Equation (1). Check the adapter turn-on and turn-off voltage, using Equation (10) and Equation (11), respectively:

$$V_{ADP-ON} = 30 + 2.3 \times \frac{R_{ADPUP} + R_{ADPDOWN}}{R_{ADPUP}} = 38.5V \quad (10)$$

$$V_{ADP-OFF} = 30 + 0.6 \times \frac{R_{ADPUP} + R_{ADPDOWN}}{R_{ADPUP}} = 32.2V \quad (11)$$

### Power Good (PG) Indicator Signal

The MP8007H integrates one PG indicator. The PG pin indicates when the PD inrush period finishes, and enables the DC/DC converter internally. The PG pin is an active-high output with internal driven. It can be floated to enable the DC/DC converter. Pull the PG pin low

externally to disable the MP8007H's DC/DC regulator.

If PG is high, the PG pin is pulled up by an internal 30μA current source while clamped by one 5.5V Zener diode between PG and RTN. If PG is low, an internal 30μA current source is disabled and the PG pin is pulled low by a pull-down resistor (about 460kΩ) between PG and RTN (GND).

Float PG for automatic start-up after the power is connected. The PG pin can be pulled low externally, but the signal sink current capability must be greater than the internal current source. The Zener diode on the PG pin clamps the internal 30μA current. Do not connect an external signal with a voltage above 5.5V to the PG pin.

### T2P Indicator Connection

The T2P pin is an active-low, open-drain output that indicates the presence of a Type 2 PSE, or when AUX is enabled. An optocoupler is typically used as the interface from the T2P pin to circuitry on the output of the converter (see Figure 8). A high-gain optocoupler and a high-impedance (e.g. CMOS) receiver are recommended.

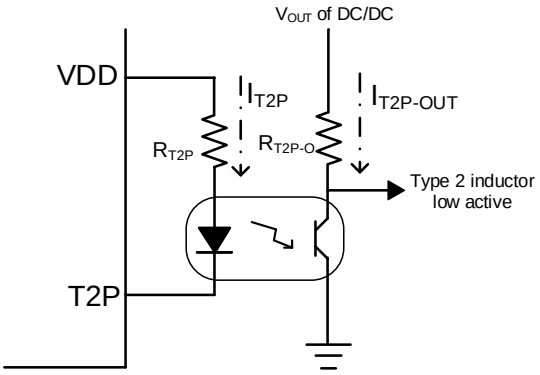



**Figure 8: T2P Indicator Circuit**

Considering the T2P sinking current (typically 2mA), T2P's output low voltage of 0.1V, and the diode forward voltage drop, choose $R_{T2P}$ = 23.7kΩ to match the typical 48V VDD input. If $V_{OUT}$ of the DC/DC converter is 12V, choose $R_{T2P-O}$ = 20kΩ based on the CRT, even if it varies with temperature, LED bias current, and aging.

If lightening an LED from VDD to T2P to indicate T2P's activity, $R_{T2P}$'s resistance must be higher to match the LED's max current and reduce power loss.

### VCC Power Supply Setting

The VCC voltage is charged through the internal LDO by VDD. Normally, $V_{CC}$ is regulated at 5.4V. A capacitor no less than 1μF is recommended for decoupling between $V_{CC}$ and GND.

In flyback mode, $V_{CC}$ can be powered from the transformer auxiliary winding to save the high-voltage LDO power loss.

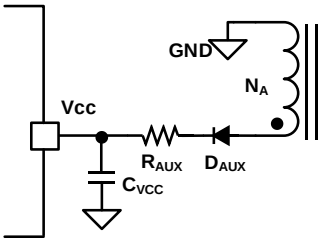



**Figure 9: Supplying $V_{CC}$ from the Auxiliary Winding**

The auxiliary winding supply voltage can be calculated with Equation (12):

$$V_{CC} = \frac{N_A}{N_S} \times (V_{OUT} + V_{D1F}) - V_{DAUXF} \quad (12)$$

Where $N_A$ and $N_S$ are the turns of the auxiliary winding and the output winding, $V_{D1F}$ is the output rectifier diode voltage drop, and $V_{DAUXF}$ is the $D_{AUX}$ voltage drop (see Figure 9).

$V_{CC}$ is clamped at about 6.2V by one internal Zener diode. The clamp current capability is about 1.2mA. If the auxiliary winding power voltage exceeds 6.2V (especially in a heavy-load condition), a series resistor ($R_{AUX}$) must limit the current to $V_{CC}$. For simple applications, supply $V_{CC}$ power directly through the internal LDO.

### Converter Output Voltage Setting

In the DC/DC converter, there are two feedback pins for different application modes.

In flyback mode, the converter detects the auxiliary winding voltage from FB1. R1 and R2 are the resistor dividers for the feedback sampling (see Figure 10).

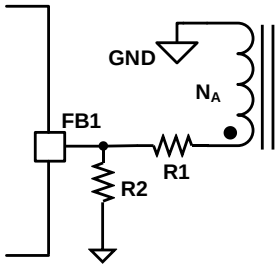



**Figure 10: Feedback in Isolation Application**

When the primary-side power MOSFET turns off, the auxiliary-winding voltage is sampled.

The output voltage can be estimated with Equation (13):

$$V_{OUT} = \frac{V_{REF1} \times (R_1 + R_2)}{R_2} \times \frac{N_S}{N_A} - V_{D1F} \quad (13)$$

Where $N_S$ is the transformer secondary-side winding turns, $N_A$ is the transformer auxiliary winding turns, $V_{D1F}$ is the rectifier diode forward drop, and $V_{REF1}$ is the reference voltage of FB1 (typically 1.99V).

When the primary-side power MOSFET turns on, the auxiliary winding forces a negative voltage to FB1. The FB1 voltage is clamped below -0.7V internally, but the clamp current should remain below -0.5mA by R1. For example, if the auxiliary winding forces -11V to R1, to drop the current flowing from FB1 to R1 below -0.5mA, the R1 resistance must be greater than 22kΩ (if ignoring R2's current).

Select R2 with a 10kΩ to 50kΩ resistor to limit noise while providing an appropriate R1 for the -0.5mA negative current limit.

In buck application mode, the feedback pin is FB2. The output voltage can be estimated with Equation (14):

$$V_{OUT} = -\frac{R_1 + R_2}{R_2} \times V_{REF2} \quad (14)$$

Where $V_{REF2}$ is the reference voltage of FB2 - 1.88V, typically.

### Maximum Switching Frequency

When the DC/DC converter works in DCM, the frequency reaches its maximum value during a full-load condition. The maximum frequency is affected by the peak current limit, the inductance, and the input/output voltage. Generally, design the maximum frequency to remain below 300kHz.

In buck mode, the maximum frequency occurs when the buck runs in critical continuous conduction mode. The frequency can be calculated with Equation (15):

$$f_{SW\_MAX} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{I_{LIM} \times L \times V_{IN}} \quad (15)$$

Where, $I_{LIM}$ is the $I_{PK}$ set by the current-limit resistor.

With a lighter load, the frequency is lower than the maximum frequency.

In flyback mode, design the maximum frequency with the minimum input voltage and the maximum load condition. The frequency can be estimated with Equation (16):

$$f_{SW} \le \frac{1}{t_{ON} + t_{CON} + t_{DELAY}} \quad (16)$$

Where $t_{ON}$ is the MOSFET one pulse turn-on time. $t_{ON}$ can be calculated with Equation (17):

$$t_{ON} = \frac{I_{LIM} \times L_M}{V_{IN}} \quad (17)$$

Where $L_M$ is the transformer primary-winding inductance, and $t_{CON}$ is the rectifier diode current conducting time. $t_{CON}$ can be estimated with Equation (18):

$$t_{CON} = \frac{N_S \times I_{LIM} \times L_M}{N_P \times (V_{OUT} + V_{D1F})} \quad (18)$$

Where $N_S$ is the transformer secondary-side winding turns, and $N_P$ is the transformer primary-side winding turns.

$t_{DELAY}$ is the resonant delay time from when the rectifier diode current drops to 0A and the auxiliary-winding voltage drops to 0V. The resonant time can be tested on the evaluation board (about 0.5μs).

In flyback mode, the DC/DC converter samples the feedback signal within 1.85μs after the primary-side MOSFET turns off. The secondary-side diode conduction time in Equation (18) is generally longer than 2μs to provide some design margin. This time period,

combined with the duty cycle, determines the maximum frequency.

### Converter Input Capacitor Selection

An input capacitor must supply the AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor keeps the noise to the IC at a minimum. Ceramic capacitors are recommended, but tantalum or low ESR electrolytic capacitors also suffice. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency. The ripple is the worst in light-load conditions. The required input capacitance can be estimated with Equation (19):

$$C_1 = \frac{0.5 \times I_{LIM} \times t_{ON}}{V_{INP\_P}} \quad (19)$$

Where $C_1$ is the DC/DC converter input bulk capacitor value, $V_{INP-P}$ is the expected input ripple, and $t_{ON}$ is the MOSFET turn-on time.

In an isolated application, $t_{ON}$ can be calculated with Equation (19):

$$t_{ON} = \frac{I_{LIM} \times L_M}{V_{IN}} \quad (20)$$

In a non-isolated application, $t_{ON}$ can be estimated with Equation (20):

$$t_{ON} = \frac{I_{LIM} \times L}{V_{IN} - V_{OUT}} \quad (21)$$

Where L is the buck's inductance value.

### Converter Output Capacitor Selection

The output capacitor maintains the DC output voltage. For the best results, use ceramic or low-ESR capacitors to minimize the output voltage ripple. For ceramic capacitors, the capacitance dominates the impedance at the switching frequency.

In flyback application mode, the worst output ripple occurs under a light-load condition. The worst output ripple can be estimated with Equation (22):

$$V_{OUTP\_P} = \frac{0.5 \times N_P \times I_{LIM} \times t_{CON}}{N_S \times C2} \quad (22)$$

Where C2 is the output capacitor value and $V_{OUTP\_P}$ is the output ripple.

Normally, a 44µF or greater ceramic capacitor is recommended as the output capacitor. This allows a small $V_O$ ripple and stable operation.

In a buck application, the worst $V_{OUT}$ ripple can be estimated with Equation (23):

$$V_{OUTP\_P} = \frac{0.5 \times I_{LIM}^2 \times L \times (V_{IN} + V_{D1F})}{C2 \times (V_{IN} - V_{OUT}) \times (V_{OUT} + V_{D1F})} \quad (23)$$

### Leakage Inductance

The transformer's leakage inductance decreases system efficiency and affects the output current and voltage precision. Optimize the transformer structure to minimize the leakage inductance. Aim for a leakage inductance below 3% of the primary-winding inductance.

### RCD Snubber for Flyback

The transformer leakage inductance causes spikes and excessive ringing on the MOSFET drain voltage waveform, affecting the output voltage sampling 0.48µs after the MOSFET turns off. The RCD snubber circuit limits the SW voltage spike (see Figure 11).

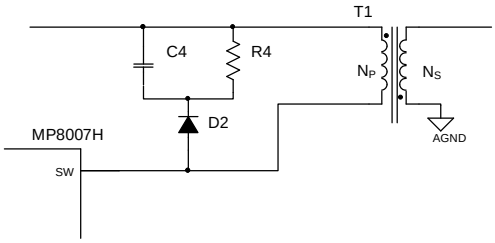



**Figure 11: RCD Snubber**

The power dissipation in the snubber circuit can be estimated with Equation (24):

$$P_{SN} = \frac{1}{2} \times L_K \times I_{LIM}^2 \times f_{SW} \quad (24)$$

Where $L_K$ is the leakage inductance.

Since R4 consumes the majority of the power, R4 can be estimated with Equation (25):

$$R4 = \frac{V_{SN}^2}{P_{SN}} \quad (25)$$

Where $V_{SN}$ is the expected snubber voltage on C4.

The snubber capacitor (C4) can be designed to get an appropriate voltage ripple on the snubber using Equation (26):

$$\Delta V_{SN} = \frac{V_{SN}}{R4 \times C4 \times f_{SW}} \quad (26)$$

Generally, a 15% ripple is acceptable.

### Buck Inductor Selection

The inductor is required to transfer the energy between the input source and the output capacitors. Unlike normal applications where inductors determine the inductor ripple, the DC/DC converter always works in DCM while $V_{IN}$, $V_{OUT}$, and $I_{LIM}$ are constant. The inductor only determines the speed of the current rising and falling, which determines the switching period.

Using the expected maximum frequency, the inductor value can be determined with Equation (27):

$$L \approx \frac{(V_{IN} - V_{OUT}) \times (V_{OUT} + V_{D1F})}{(V_{IN} + V_{D1F}) \times I_{PEAK}} \times \frac{1}{f_{SW}} \quad (27)$$

Where $f_{SW}$ is the expected maximum switching frequency, which should generally be below 300kHz .

### Converter Output Diode Selection

The output rectifier diode supplies current to the output capacitor when the internal MOSFET is off. Use a Schottky diode to reduce loss due to the diode forward voltage and recovery time.

In isolated application, the diode should be rated for a reverse voltage above that can be calculated with Equation (28):

$$V_{D1} = V_{OUT} + \frac{V_{IN} \times N_S}{N_P} + V_{PD1} \quad (28)$$

$V_{PD1}$ can be selected at 40% to 100% of $V_{OUT}$ + $V_{IN}$ x $N_S$ / $N_P$. An RC or RCD snubber circuit for the output diode D1 is recommended.

In buck mode, the diode reverse voltage equates to the input voltage. A 20% to 40% margin is recommended.

In both applications, the current rating should be greater than the maximum output current.

### Converter Dummy Load

When the system operates without a load in flyback mode, the output voltage rises above the normal operation voltage because of the minimum switching frequency limitation. Use a dummy load for good load regulation. A large dummy load decreases efficiency, so the dummy load is a tradeoff between efficiency and load regulation. Figure 14 on page 30 shows that certain applications require a minimum load of about 10mA.

### Design Example

Below is a design example following the application guidelines for the following specifications:

**Table 2: Flyback Design Example**

| | |
|---|---|
| **$V_{DD}$ - $V_{SS}$** | 36V to 57V (PoE supply) |
| **$R_{DET}$** | 24.9kΩ |
| **$R_{CLASS}$** | 41.2Ω |
| **$V_{ADAPTER}$** | 48V |
| **$V_{OUT}$** | 12V |
| **$P_{OUT}$** | 11W |

Figure 14 on page 30 shows the detailed application schematic, and is the basis for the typical performance waveforms. Typically, the device is powered by the PSE ($V_{DD}$ - $V_{SS}$ = 48V). When an adapter voltage above 38.5V is present, the internal MOSFET between RTN and VSS turns off, and the device is powered by the adapter, regardless of the PSE voltage. Refer to the related evaluation board datasheets for more detailed device applications.

## PCB Layout Guidelines

Efficient layout of the PoE front-end and high-frequency switching power supply is critical for stable operation. Poor layout may result in reduced performance, excessive EMI, resistive loss, and system instability. For the best results, refer to Figure 12 and Figure 13, and follow the guidelines below:

***For PD Interface Circuits:***

1. All components must follow the power flow, from RJ-45, the Ethernet transformer, diode bridges, and TVS, to the 0.1μF capacitor and the DC/DC converter input bulk capacitor.
2. Make all leads as short as possible with wide power traces.
3. The spacing between $V_{DD}$ (48V) and $V_{SS}$ must comply with safety standards, such as IEC60950.
4. Place the PD interface circuit ground planes with reference to VSS, and place the switching converter ground planes with reference to RTN/GND.
5. The exposed PAD must be connected to GND. It cannot be connected to VSS.
6. If adapter power detection is enabled, the AUX divider resistor should be close to the AUX pin.
7. Place diode D5 (between VSS and RTN) close to VSS and RTN.

***For Flyback Circuits:***

1. Ensure the input loop between the input capacitor, transformer, SW, and GND plane is as short as possible to minimize noise and ringing.
2. Make the output loop between the rectifier diode, output capacitor, and transformer as short as possible.
3. Keep the clamp loop circuit between D2, C4, and the transformer as small as possible.
4. Place the VCC capacitor close to VCC for optimal decoupling.
5. Place the current-setting resistor (R3) as close to ILIM and AGND as possible.
6. Route the feedback trace far away from noise sources (such as SW).
7. Keep the trace connecting FB1 short.
8. Use a single-point connection between the power GND and signal GND.
9. Place vias around GND and the thermal pad to lower the die temperature.

See the Typical Application Circuit on page 30 for more details.

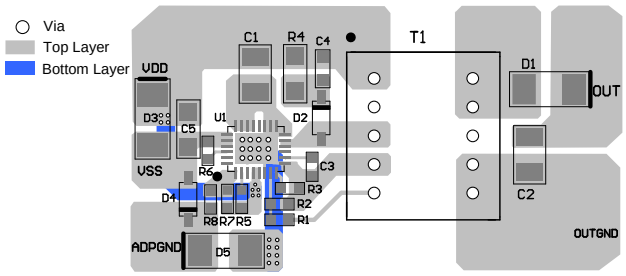



**Figure 12: Recommended Flyback Layout**

***For Buck Circuits:***

1. Ensure the input loop between the input capacitor, rectifier diode, SW, and GND plane is as short as possible for minimal noise and ringing.
2. Keep the output loop between the rectifier diode, the output capacitor, and the inductor as short as possible.
3. Place the VCC capacitor close to VCC for optimal decoupling. The current setting resistor (R3) should be placed as close to ILIM and AGND as possible.
4. Connect the output voltage sense and VDD power supply from the output capacitor with parallel traces.
5. Route the feedback trace far away from noise sources, such as SW.
6. Keep the trace connected to FB2 as short as possible.
7. Ensure the trace for VDD power is sufficiently wide.
8. Use a single-point connection between the power GND and signal GND.
9. Place vias around GND and the thermal pad to lower the die temperature.

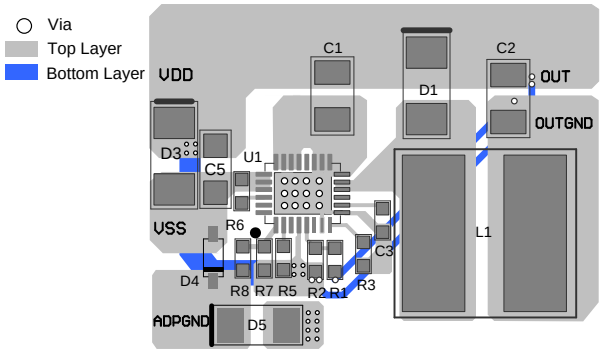



**Figure 13: Recommended Buck Layout**

# TYPICAL APPLICATION CIRCUIT

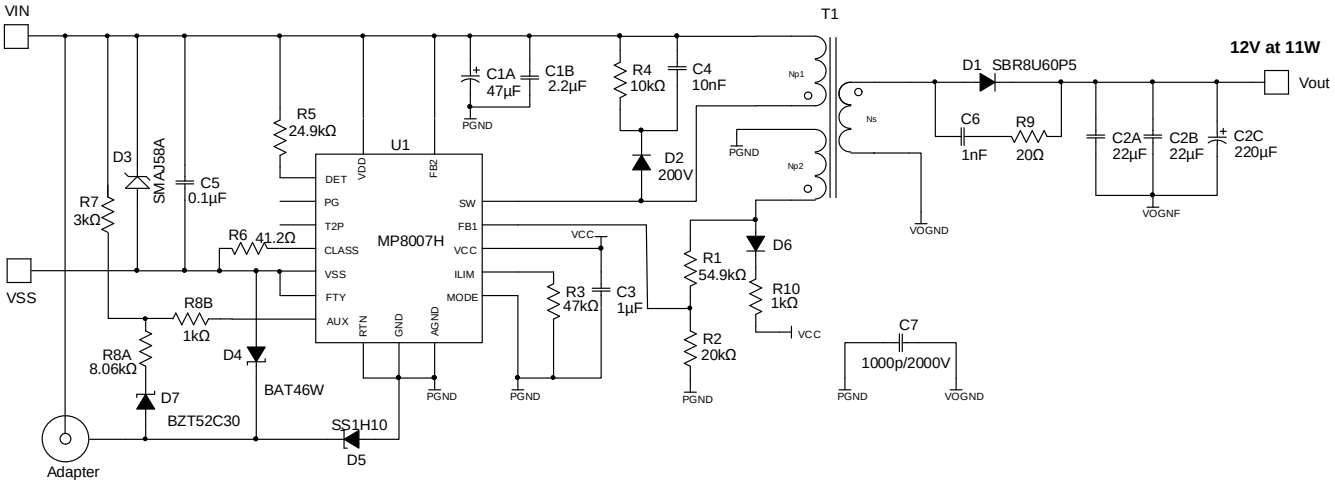
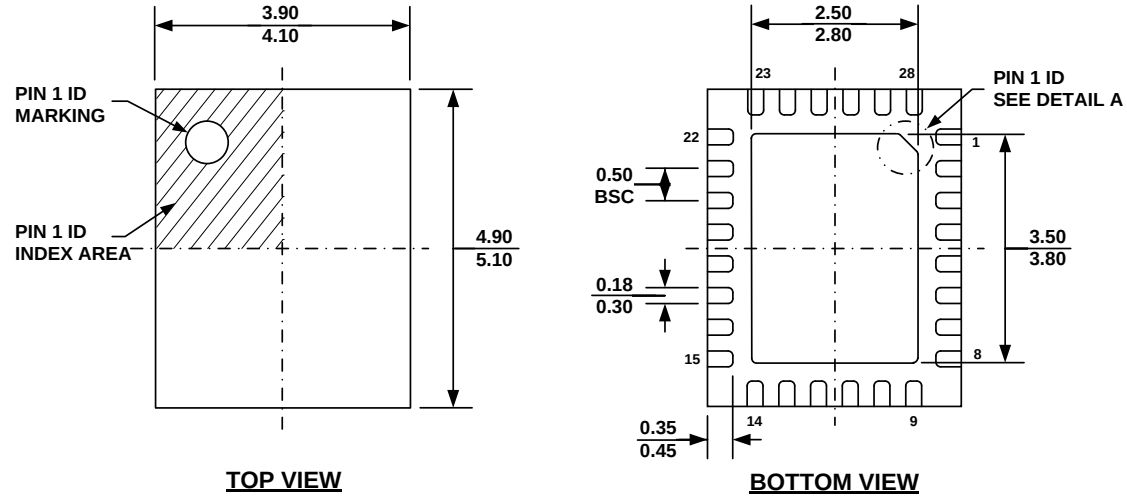



**Figure 14: Flyback Application Circuit, $V_{IN}$ = 36V to 57V, PoE O Ring, 48V Adapter Input, $V_{OUT}$ = 12V at 11W**

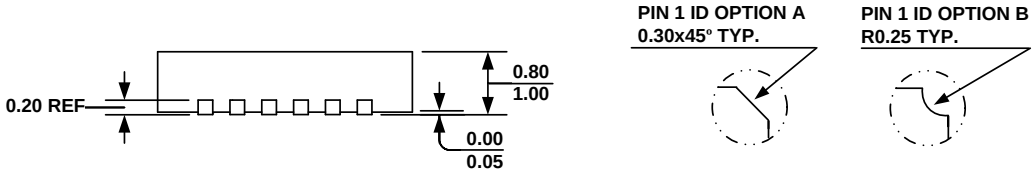
# PACKAGE INFORMATION

## QFN-28 (4mmx5mm)



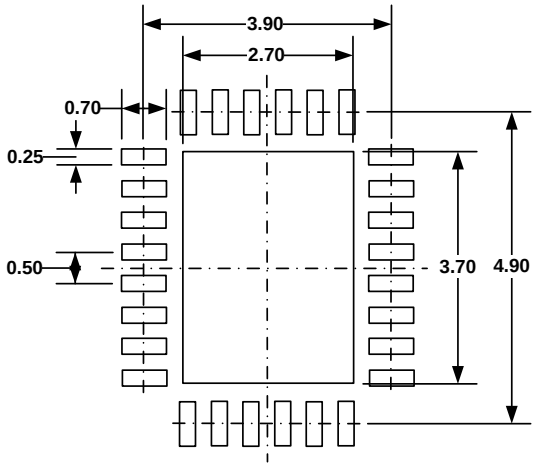

TOP VIEW

BOTTOM VIEW




SIDE VIEW

DETAIL A

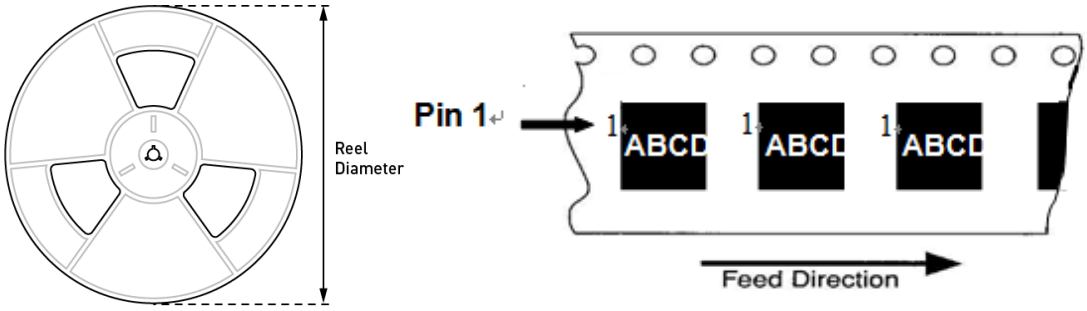



RECOMMENDED LAND PATTERN

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
4) DRAWING CONFORMS TO JEDEC MO-220, VARIATION VGHD-3.
5) DRAWING IS NOT TO SCALE.

## CARRIER INFORMATION




| Part Number | Package Description | Quantity/Reel | Quantity/Tube | Reel Diameter | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|
| MP8007HGV-Z | QFN-28 (4mmx5mm) | 5000 | N/A | 13in | 12mm | 8mm |