



The Future of Analog IC Technology®

MP2317

26V, 1A, 600kHz, High-Efficiency, Synchronous, Step-Down Converter

DESCRIPTION

The MP2317 is a high-efficiency, synchronous, rectified, step-down, switch-mode converter with built-in internal power MOSFETs. It offers a very compact solution that achieves 1A of continuous output current with excellent load and line regulation over a wide input supply range.

The MP2317's switching edge is optimized for low EMI. SW anti-ringing is employed to address high-frequency radiation EMI issues.

Full protection features include over-current protection (OCP) and thermal shutdown.

The MP2317 requires a minimum number of readily available, standard, external components and is available in a space-saving, 6-pin, TSOT23 package.

FEATURES

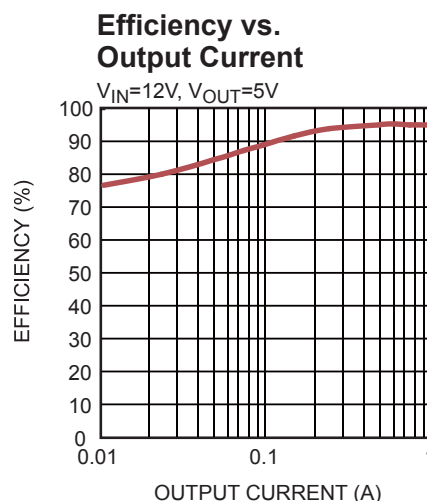
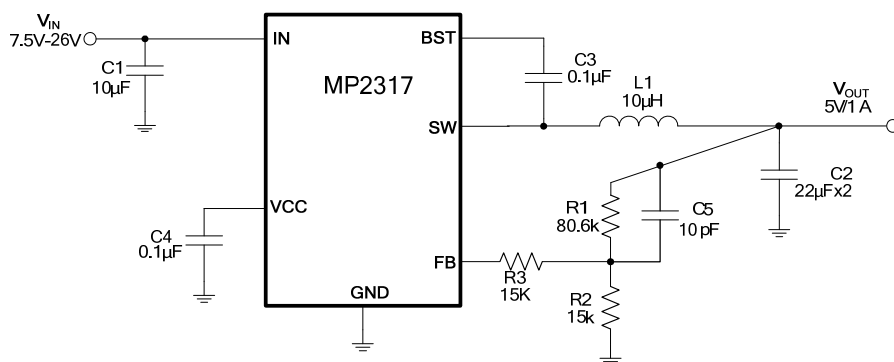
- Wide 7.5V to 26V Operating Input Range
- 1A Load Current
- 100mΩ/50mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- Internal Power-Save Mode for Light Load
- 600kHz Fixed Switching Frequency at CCM
- Optimized for Low EMI
- Internal Soft Start
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 3.3V
- Available in a TSOT23-6 Package

APPLICATIONS

- Stand-By Power Supply
- White Goods
- Flat-Panel Television and Monitors

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TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2317GJ	TSOT23-6	See Below

* For Tape & Reel, add suffix –Z (e.g. MP2317GJ–Z)

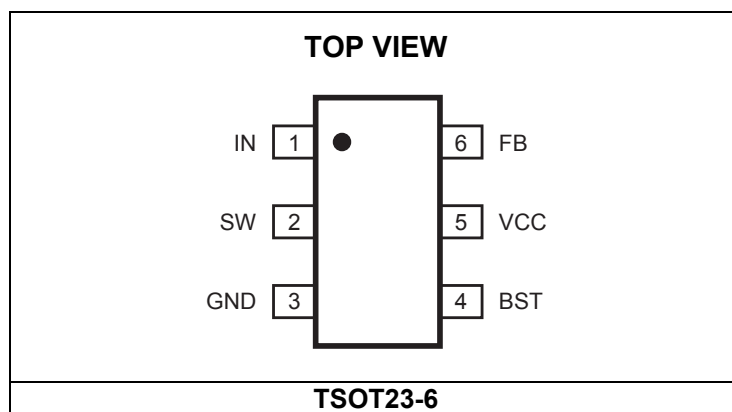
TOP MARKING

1AQR Y

AQR: Product code of MP2317GJ

Y: Year code

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

V_{IN}	-0.3V to +28V
V_{SW}	-0.6V (-5V < 10ns) to +28V (30V < 10ns)
V_{BST}	$V_{SW} + 6V$
All other pins	-0.3V to +6V
Continuous power dissipation ($T_A = +25^{\circ}C$) ⁽²⁾	1.25W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to 150°C

Recommended Operating Conditions ⁽³⁾

Supply voltage (V_{IN})	7.5V to 26V
Output voltage (V_{OUT})	3.3V to $V_{IN} \times D_{MAX}$
Operating junction temp (T_J)....	-40°C to +125°C

Thermal Resistance ⁽⁴⁾	θ_{JA}	θ_{JC}
TSOT23-6.....	100.....	55..... °C/W

NOTES:

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A . The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = $(T_J$ (MAX) - T_A) / θ_{JA} . Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

$V_{IN} = 12V$, $T_J = -40^{\circ}C$ to $125^{\circ}C$ ⁽⁵⁾, unless otherwise noted. Typical value is based on the average value when $T_J = 25^{\circ}C$.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (quiescent)	I_q	$V_{FB} = 1V$		150		μA
HS switch-on resistance	HS_{RDS-ON}	$V_{BST-SW} = 4V$		100		$m\Omega$
LS switch-on resistance	LS_{RDS-ON}	$V_{CC} = 4V$		50		$m\Omega$
Switch leakage	SW_{LKG}				1	μA
Current limit	I_{LIMIT}	Duty cycle = 40%, $T_J = 25^{\circ}C$	1.4	2.2	3	A
Oscillator frequency	f_{SW}	$V_{FB} = 750mV$	500	600	700	kHz
Foldback frequency	f_{FB}	$V_{FB} = 200mV$		0.2		f_{SW}
Maximum duty cycle	D_{MAX}	$V_{FB} = 750mV$		93		%
Minimum on time ⁽⁶⁾	$T_{ON\ MIN}$			90		ns
Feedback voltage	V_{FB}		775	791	807	mV
Feedback current	I_{FB}	$V_{FB} = 820mV$		10	50	nA
V_{IN} under-voltage lockout threshold rising	$INUV_{Vth}$		5.2	6.3	7.5	V
V_{IN} under-voltage lockout threshold hysteresis	$INUV_{HYS}$			500		mV
VCC regulator	V_{CC}			4		V
VCC load regulation		$I_{CC} = 5mA$		1.5		%
Soft-start period	T_{SS}	10% to 90%	0.8	1.5	2.2	ms
Thermal shutdown ⁽⁶⁾	T_{SD}			150		$^{\circ}C$
Thermal hysteresis ⁽⁶⁾	$T_{SD\ HYS}$			20		$^{\circ}C$

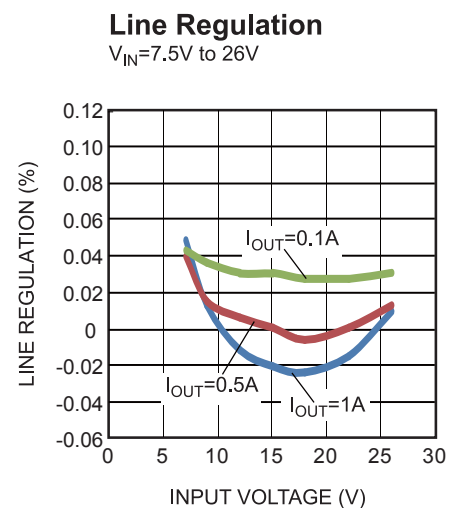
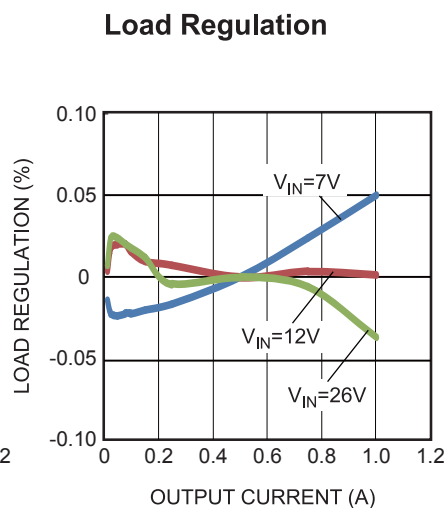
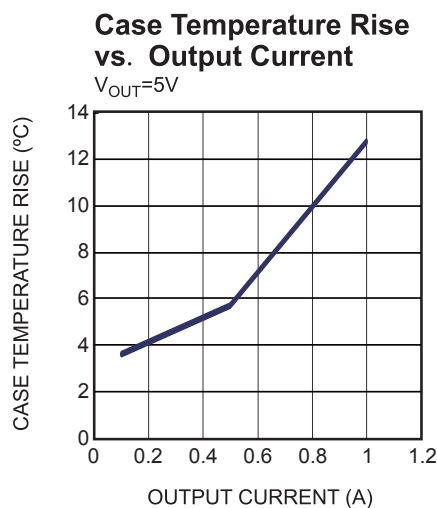
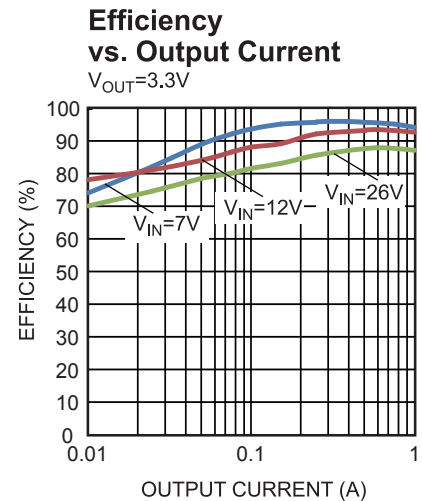
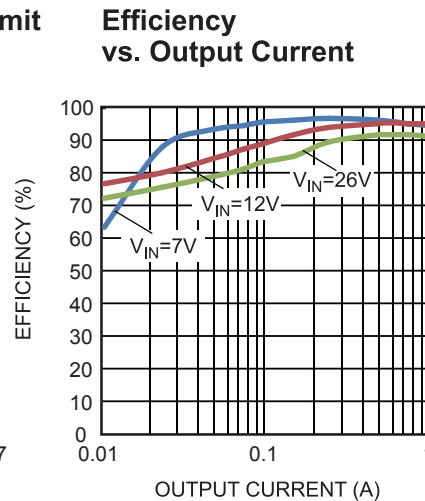
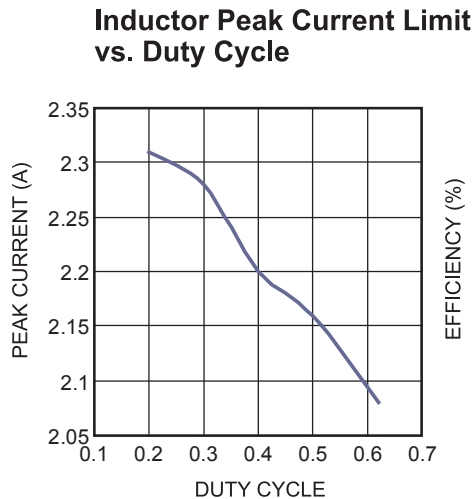
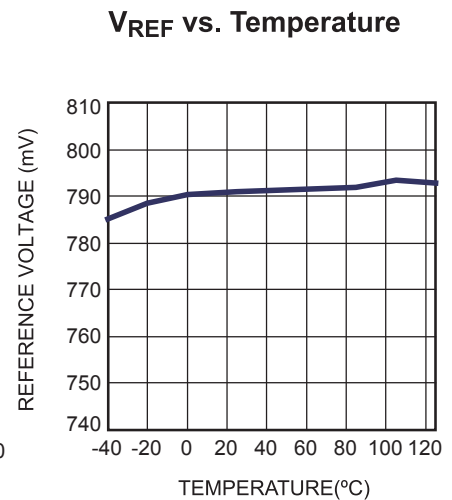
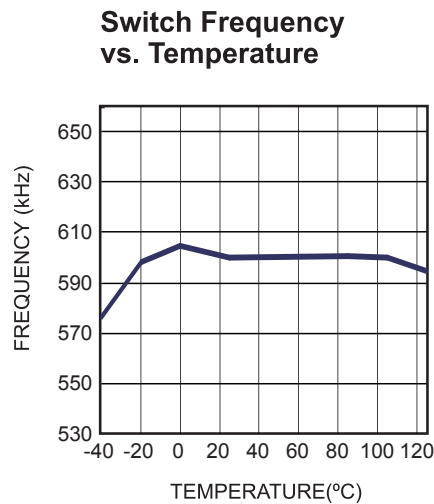
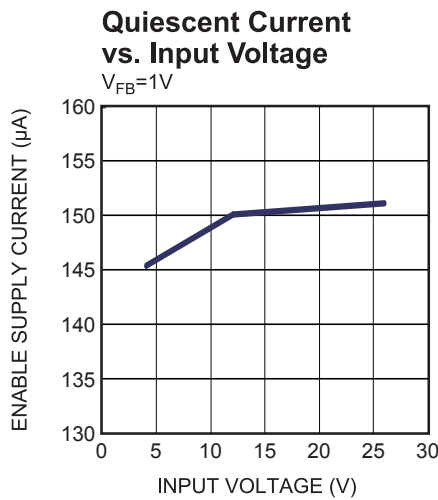
NOTES:

5) Not tested in production and guaranteed by over-temperature correlation.

6) Guaranteed by design and characterization test.

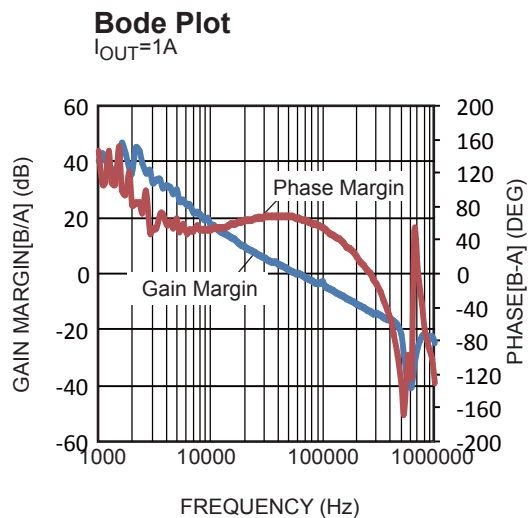
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 10\mu H$, $T_A = 25^\circ C$, unless otherwise noted.



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 10\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

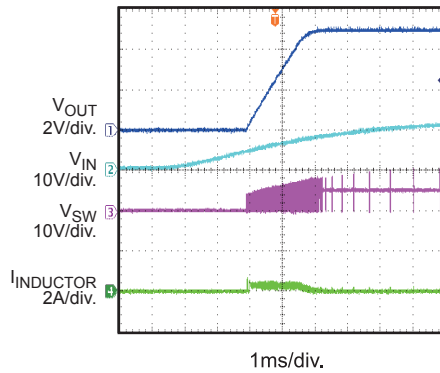


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN} = 12V$, $V_{OUT} = 5V$, $L = 10\mu H$, $T_A = 25^\circ C$, unless otherwise noted.

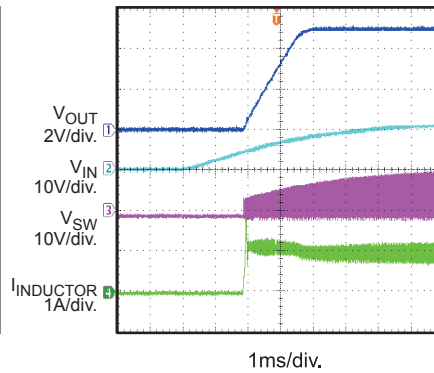
Start-Up through Input Voltage

$I_{OUT}=0A$



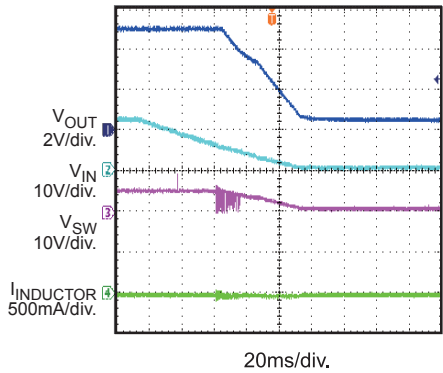
Start-Up through Input Voltage

$I_{OUT}=1A$



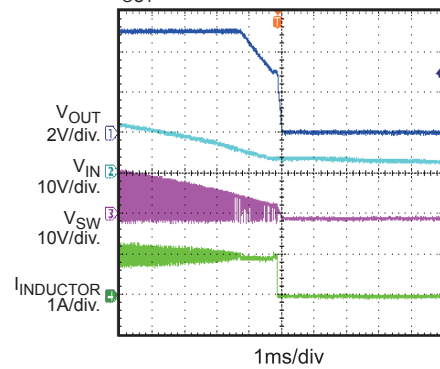
Shutdown through Input Voltage

$I_{OUT}=0A$



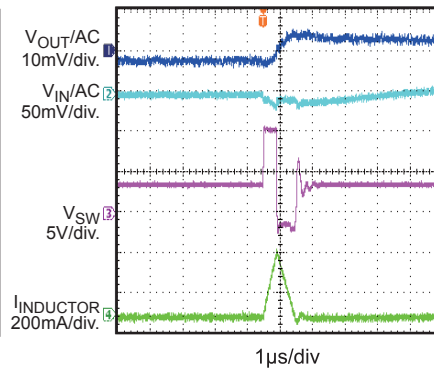
Shutdown through Input Voltage

$I_{OUT}=1A$



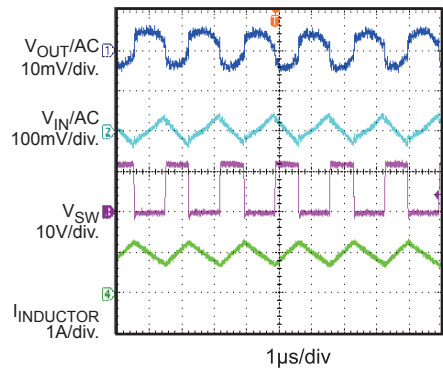
Input/Output Ripple

$I_{OUT}=0A$



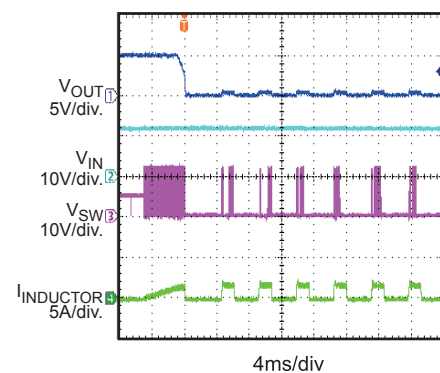
Input/Output Ripple

$I_{OUT}=1A$



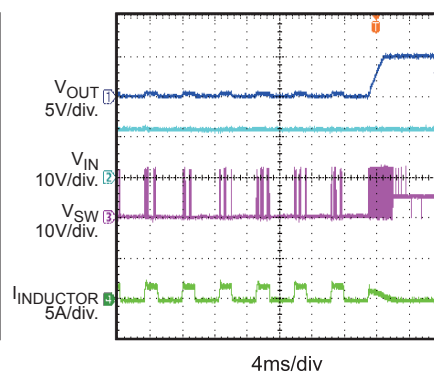
OCP Entry

$I_{OUT}=0A$



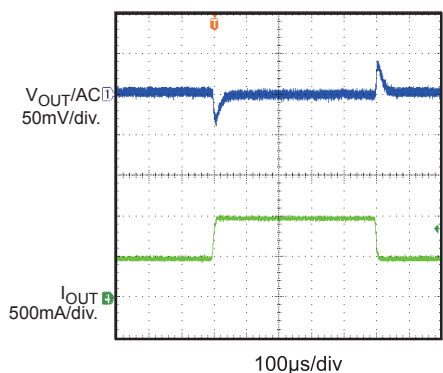
OCP Recovery

$I_{OUT}=0A$



Load Transient Response

$I_{OUT}=0.5A$ to $1A$



PIN FUNCTIONS

Package Pin #	Name	Description
1	IN	Supply voltage. The MP2317 operates from a +7.5V to +26V input rail. C1 is needed to decouple the input rail. Connect using wide PCB traces.
2	SW	Switch output. Connect using wide PCB traces.
3	GND	System ground. GND is the reference ground of the regulated output voltage. GND requires special consideration during PCB layout. Connect GND with copper traces and vias.
4	BST	Bootstrap. Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver.
5	VCC	Internal LDO output. Decouple VCC with a 0.1 μ F - 0.22 μ F capacitor. VCC can be biased by an external 5V output voltage through a diode.
6	FB	Feedback. An external resistor divider from the output to GND tapped to FB sets the output voltage. To prevent a current-limit runaway during a short-circuit fault condition, the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 396mV.

BLOCK DIAGRAM

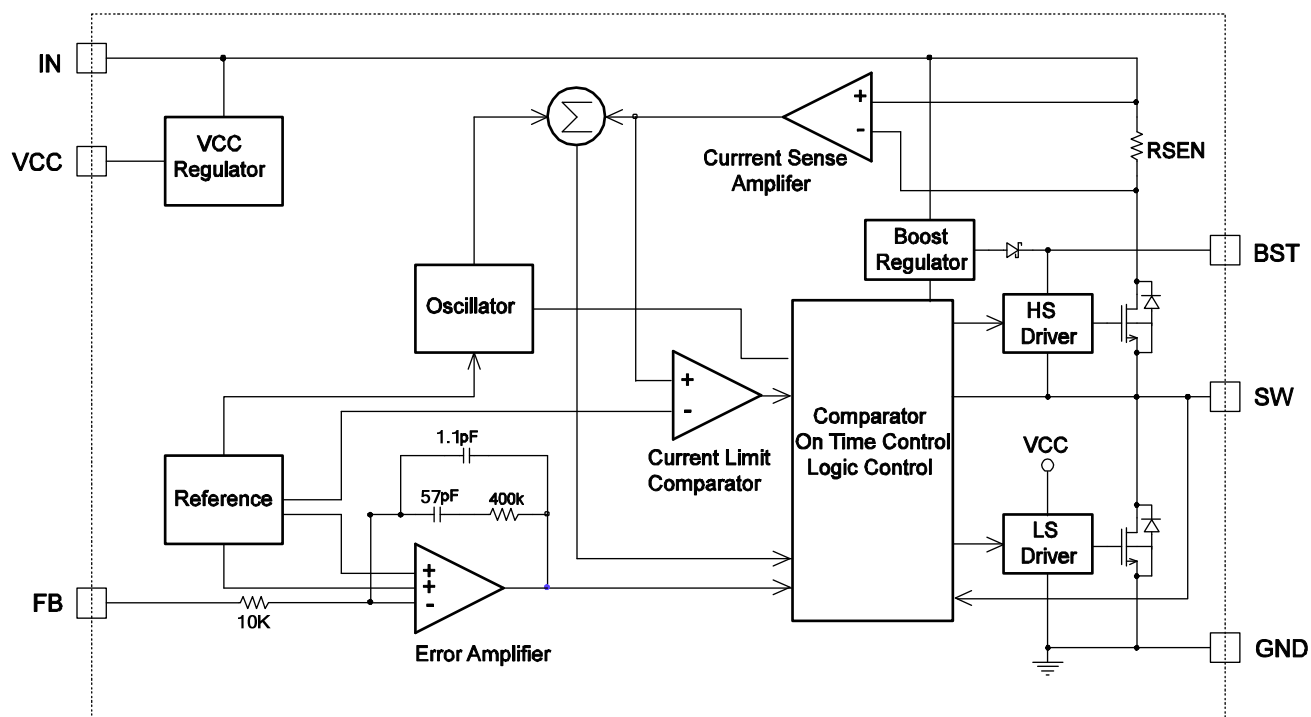


Figure 1: Functional Block Diagram

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, the entire chip shuts down. When the temperature is below its lower threshold, typically 130°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, C3, L1, and C2 (see Figure 3). If $V_{IN} - V_{SW}$ is more than 4V, U2 regulates M3 to maintain a 4V BST voltage across C3.

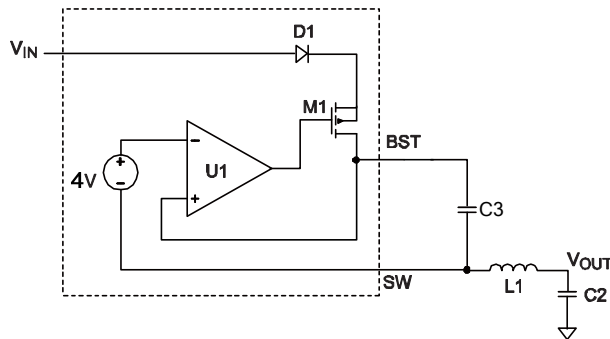


Figure 3: Internal Bootstrap Charging

Circuit Start-Up and Shutdown

If V_{IN} is higher than its UVLO threshold, the chip starts up. The reference block starts first, generating a stable reference voltage and current, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

In the shutdown procedure, the signaling path is first blocked to prevent any fault triggering. V_{COMP} and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the Typical Application on page 1). The feedback resistor (R1) also sets the feedback loop bandwidth with the external compensation capacitor. Calculate R2 with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.791V} - 1} \quad (1)$$

Table 1 lists the recommended resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages

V _{OUT} (V)	R1 (kΩ)	R2 (kΩ)	Lo (μH)
3.3	80.6	25.5	10
5	80.6	15	10

Selecting the Inductor

A 1μH to 22μH inductor with a DC current rating at least 25% percent higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 30mΩ. For most designs, the inductance value can be derived from Equation (2):

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor current to be approximately 30% of the maximum load current. The maximum inductor peak current can be calculated with Equation (3):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Under light-load conditions below 100mA, a larger inductance is recommended for improved efficiency.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, and therefore requires a capacitor to supply AC current to the step-down converter while maintaining the DC input voltage. For best performance, use low ESR capacitors. Ceramic capacitors with X5R or

X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22μF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, a small, high-quality ceramic capacitor (i.e.: 1μF) should be placed as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_s \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right) \quad (7)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance, which mainly causes the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L_1 \times C_2} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (8)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2317 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

An optional, external diode may enhance the efficiency of the regulator. The conditions of the external diode are applied when the output voltage is 5V.

In this case, it is recommended to connect an external BST diode from V_{OUT} to BST (see Figure 4).

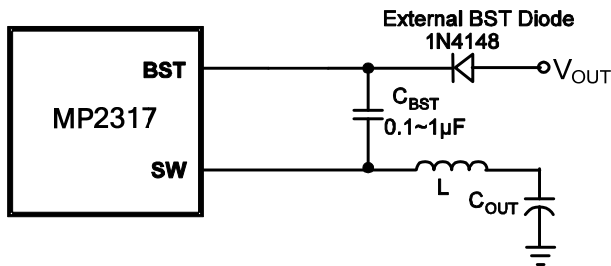


Figure 4: Optional External Bootstrap Diode Added to Enhance Efficiency

External VCC Diode

When V_{OUT} is 5V, an external optional diode from V_{OUT} to VCC may enhance the efficiency of the regulator (see Figure 5).

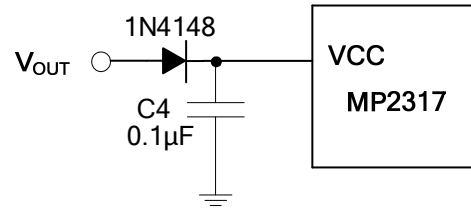


Figure 5: Optional External Diode Added to Enhance Efficiency

PCB Layout Guidelines⁽⁷⁾

Efficient PCB layout is critical for stable operation. For best results, refer to Figure 6 and follow the guidelines below.

1. Keep the connection of the input ground and GND as short and wide as possible.
2. Connect the ground of the VCC capacitor to the IC's GND through multiple vias or wide traces.
3. Keep the connection of the input capacitor and IN as short and wide as possible.
4. Ensure that all feedback connections are short and direct.
5. Place the feedback resistors and compensation components as close to the chip as possible.
6. Route SW away from sensitive analog areas such as FB.

NOTE:

- 7) The recommended layout is based on Figure 8: Typical Application Circuit.

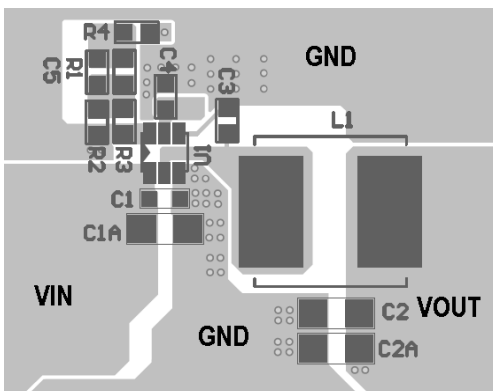
Design Example

Table 2 is a design example following the application guidelines for the specifications below:

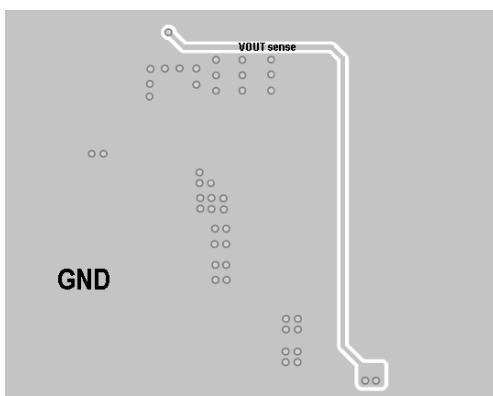
Table 2: Design Example

V_{IN}	12V
V_{OUT}	5V
I_O	1A

The detailed application schematics are shown in Figure 7 and Figure 8. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.



Top Layer



Bottom Layer

Figure 6: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

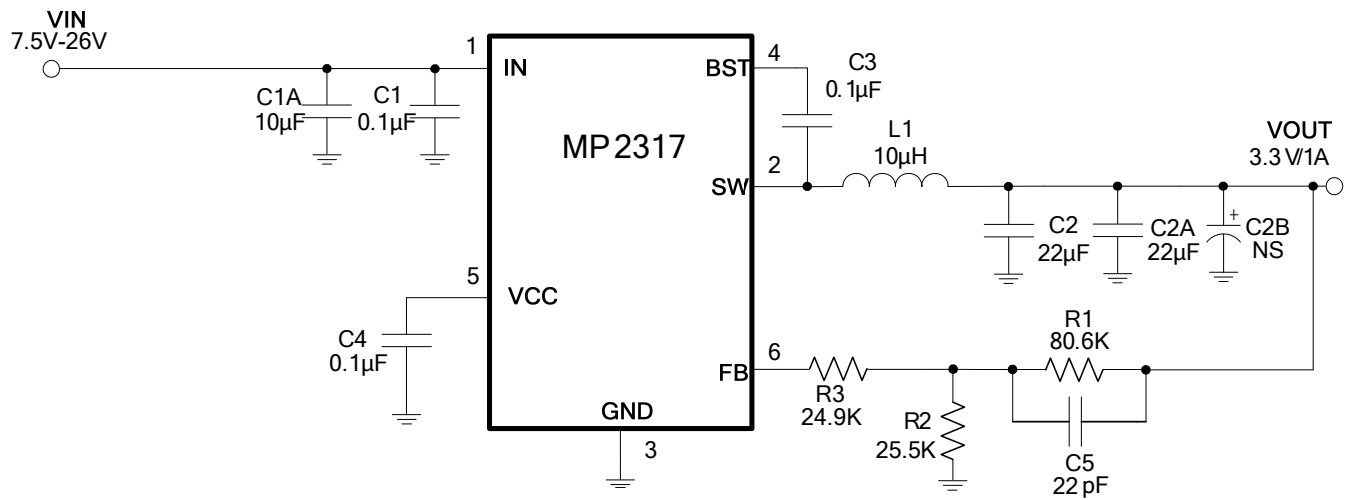


Figure 7: 3.3V/1A Output

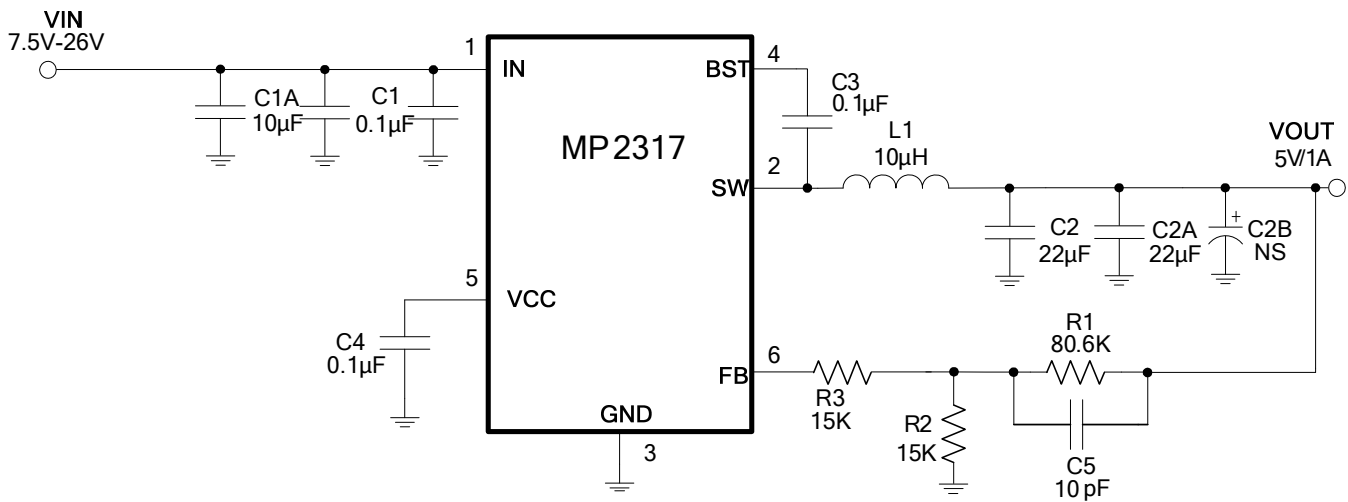
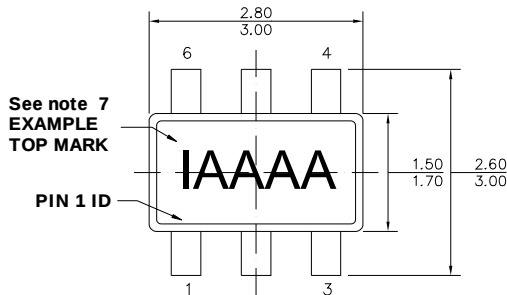


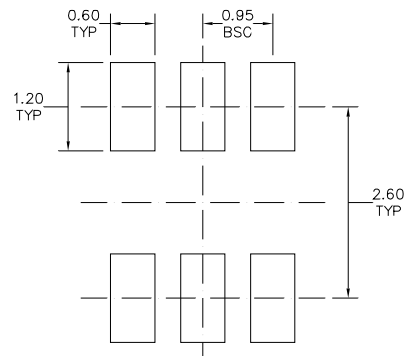
Figure 8: 5V/1A Output

PACKAGE INFORMATION

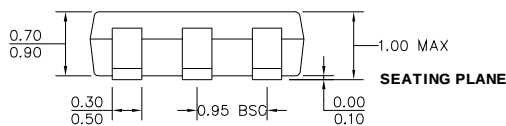
TSOT23-6



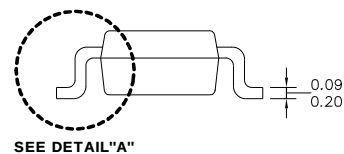
TOP VIEW



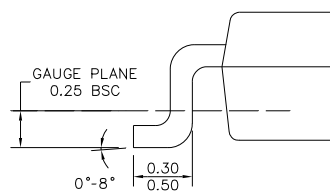
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH PROTRUSION OR GATE BURR
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
- 5) DRAWING CONFORMS TO JEDEC MO193, VARIATION AB
- 6) DRAWING IS NOT TO SCALE
- 7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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