700V Half Bridge MOSFET/IGBT Gate Driver

Description

The IRS21814STR is a high voltage, high speed power MOSFET drivers with dependent high and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700 V.

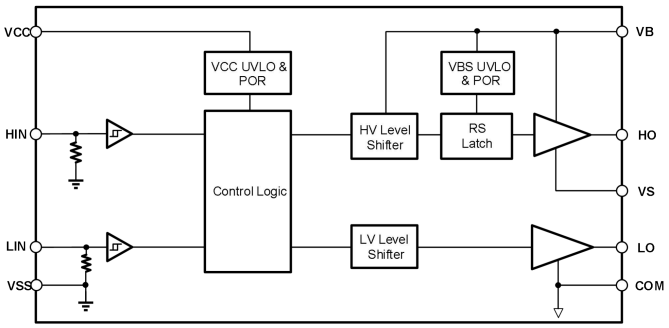
Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +700 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Undervoltage lockout for both channels
  --UVLO forward 8.9V
  --UVLO reverse 8.2V
- Turn-on/Turn-off propagation delay -
  - Ton/Toff =130ns/130ns
- Matched propagation delay for both channels
- Typically output Source/Sink current capability: 4A/4A

Functional Block Diagram



Function Pin Description

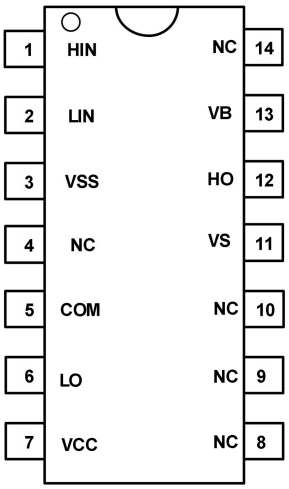


Figure7-1 14-Pin SOIC14 Top view

Table7-1 Lead Definitions

Number	Symbol	Description
1	HIN	Logic input for high side gate driver output (HO), in phase
2	LIN	Logic input for low side gate driver output (LO), in phase
3	VSS	Logic ground
4	NC	No connect
5	COM	Low side return
6	LO	Low side gate drive output
7	VCC	Low side and logic fixed supply
8	NC	No connect
9	NC	No connect
11	VS	High side floating supply return
12	HO	High side gate drive output
13	VB	High side floating supply
14	NC	No connect

Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to COM and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	725	V
V_S	High side floating supply return	V_B - 25	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	25	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input（HIN, LIN）	V_{SS}-0.3	V_{SS}+5	
V_{SS}	Logic ground	V_{CC}-25	V_{CC}+0.3	
dV_S/dt	dV/dt noise Immunity		50	V/ns
ESD	HBM Model	1.5		kV
	Machine Model	500		V
P_D	Package Power Dissipation @ TA ≤25°C		0.625	W
Rth_{JA}	Thermal Resistance, Junction to Ambient		200	°C /W
T_J	Junction Temperature		150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)		300	

Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and COM are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to COM and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	VS + 10	VS + 20	V
V_S	High side floating supply return	-9	700	
V_{HO}	High side gate drive output	V_S	V_B	
V_{CC}	Low side and main power supply	10	20	
V_{LO}	Low side gate drive output	0	VCC	
V_{IN}	Logic input of HIN & LIN	0	VCC	
V_{SS}	Logic ground	-5	5	
T_A	Ambient temperature	-40	125	°C

Electrical Characteristics

Valid for temperature range at T_A= 25ºC, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

Symbol	Definition	MIN	TYP	MAX	Units	Test Condition
t_{ON}	Turn-on propagation delay		130	220	ns	VS=0
t_{OFF}	Turn-off propagation delay		130	220		VS=0V or 700V
t_{sd}	Shut-down propagation delay		130	220		
t_R	Turn-on rise time		40	60		VS=0V
t_F	Turn-off fall time		20	35		
MT	Matched propagation time delay			50		
V_{CCUV+}	VCC supply UVLO threshold	8	8.9	9.8	V	
V_{CCUV-}		7.4	8.2	9.0		
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	0.7	—		
V_{BSUV+}	VBS supply UVLO threshold	8	8.9	9.8		
V_{BSUV-}		7.4	8.2	9.0		
$V_{BSUVHYS}$	hysteresis of V_{BS} UVLO	—	0.7	—		
I_{LK}	High-side floating supply leakage current	—	—	50	μA	VB=VS=700V
I_{QBS}	Quiescent VB supply current	—	50	100		VIN=0V or 5V
I_{QCC}	Quiescent VCC supply current	—	150	240		
V_{IH}	Logic “1” input voltage	2.5	—	—	V	VCC=10~20V
V_{IL}	Logic “0” input voltage	—	—	0.8		
V_{OH}	High level output voltage, VBIAS - VO	—	—	1.4		IO=0A
V_{OL}	Low level output voltage, VO	—	—	0.1		IO=20mA
I_{IN+}	Logic “1” Input bias current	—	25	60	μA	LIN=5V,
I_{IN-}	Logic “0” Input bias current	—	—	2		LIN=0V,
I_{O+}	Output high short circuit pulsed current	3.0	4.0	—	A	Vo=0V PW≤10μs
I_{O-}	Output low short circuit pulsed current	3.0	4.0	—		Vo=15V P

Function Description

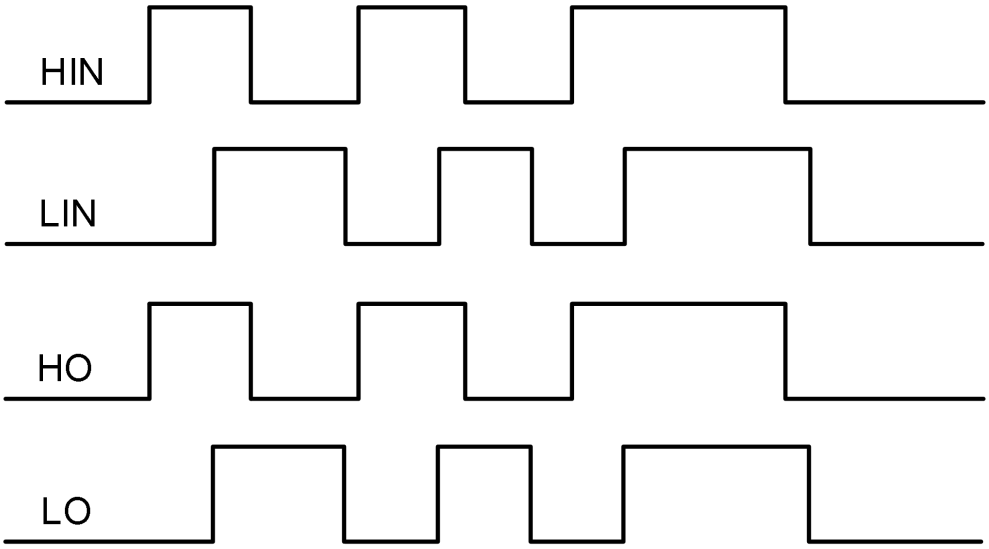


Figure 1. IRS21814STR Input and output timing waveform

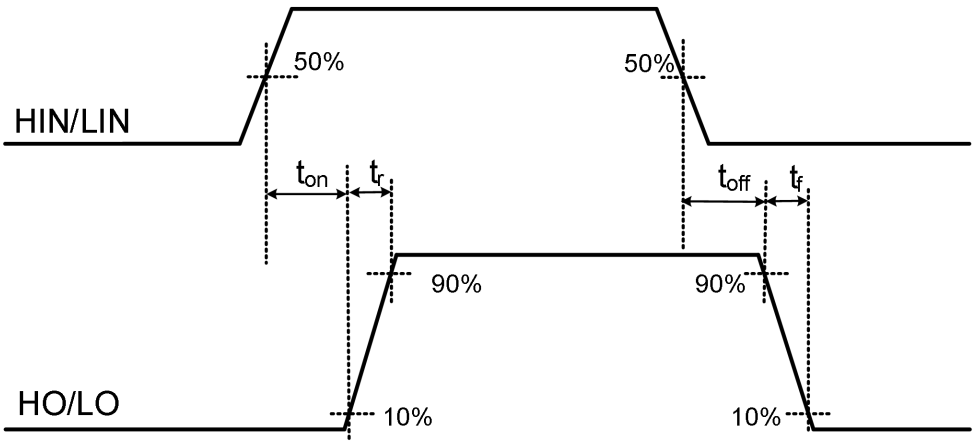


Figure 2. Propagation Time Waveform Definition

Waveform of Parameter

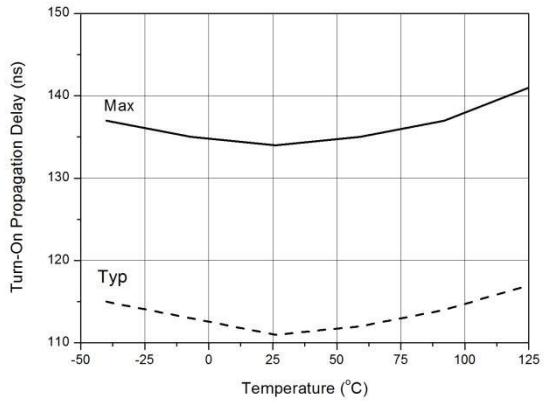


Figure 3A. Turn-On Propagation Delay vs. Temperature

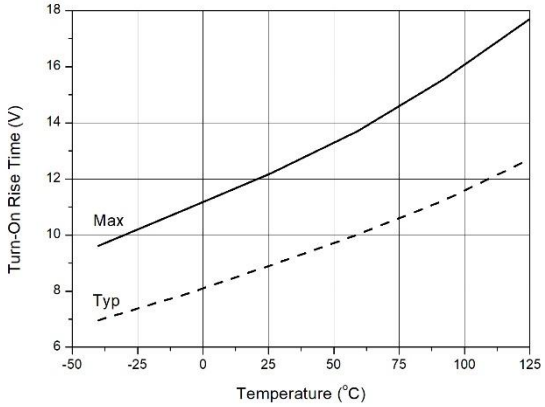


Figure 5A.Turn-On Rise Time vs. Temperature

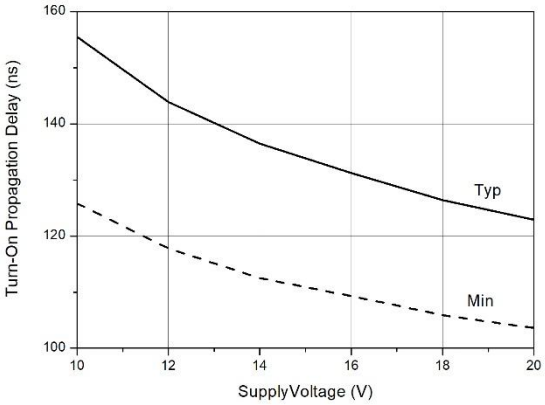


Figure 3B. Turn-on Propagation Delay vs. Supply Voltage

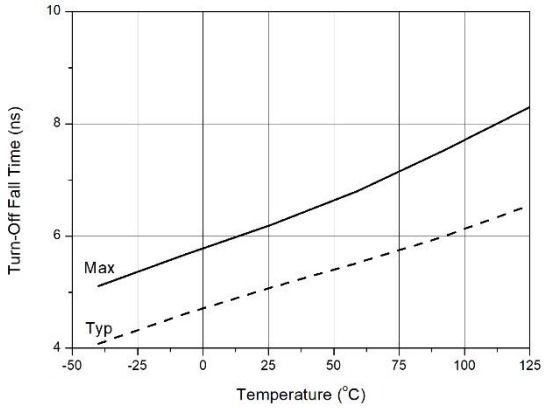


Figure 6A.Turn-Off Fall Time vs. Temperature

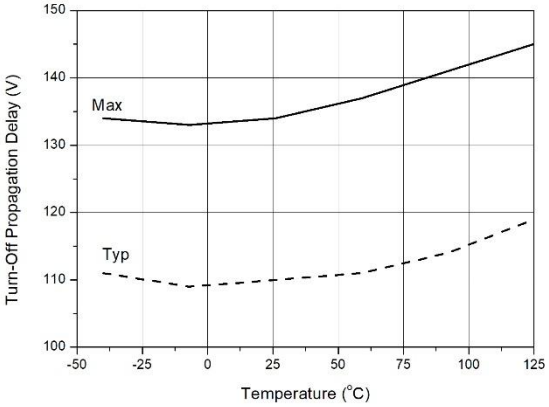


Figure 4A. Turn-Off Propagation Delay vs. Temperature

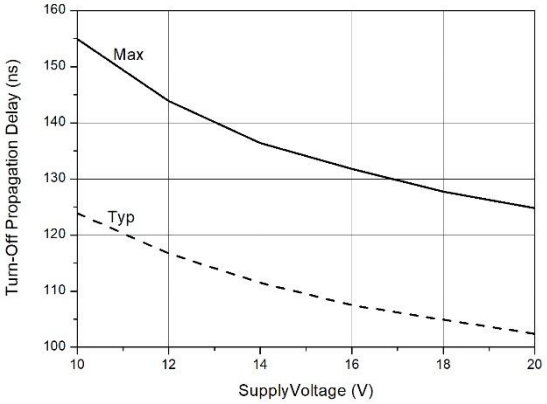


Figure 4B. Turn-off Propagation Delay vs. Supply Voltage

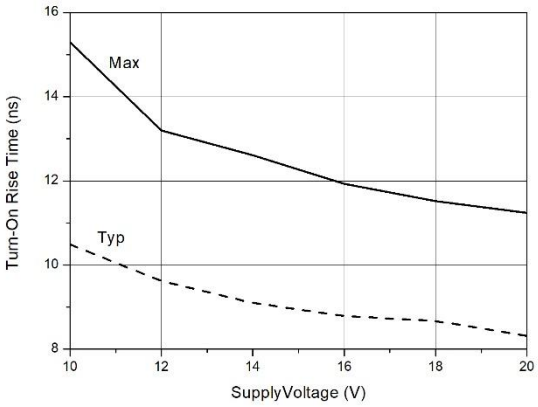


Figure 5B.Turn-On Rise Time vs. Supply Voltage

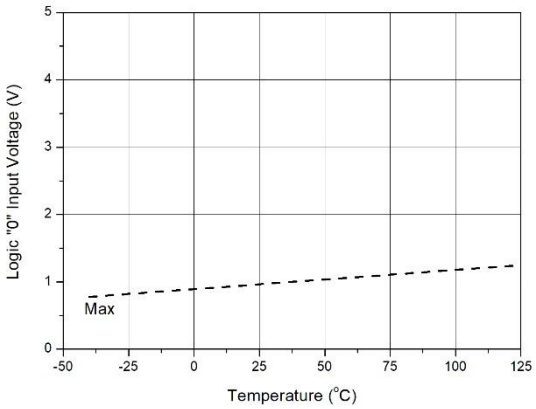


Figure 8A. Logic "0" Input Voltage vs. Temperature

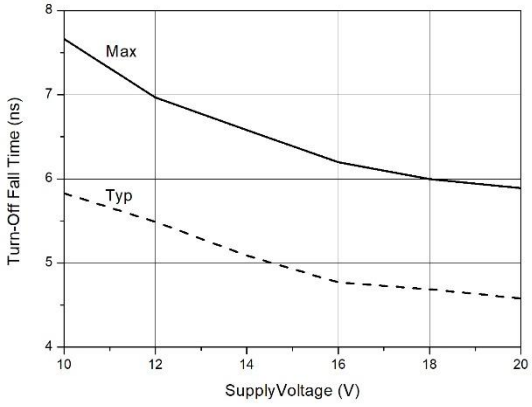


Figure 6B.Turn-Off Fall Time vs. Supply Voltage

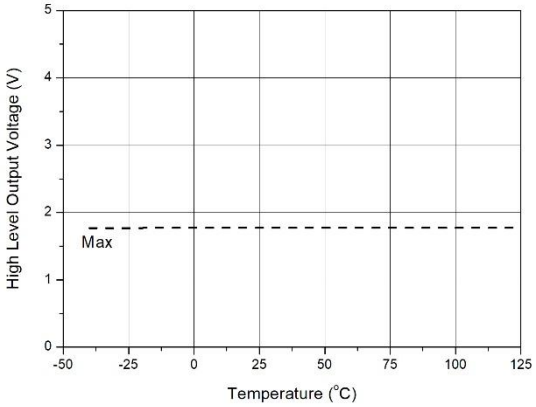


Figure 9A. High Level Output Voltage vs. Temperature (Io = 0mA)

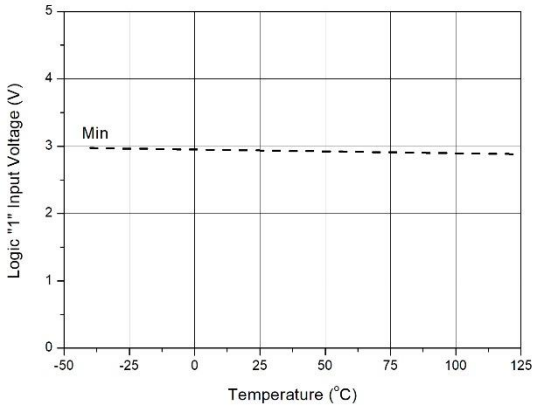


Figure 7A. Logic "1" Input Voltage vs. Temperature

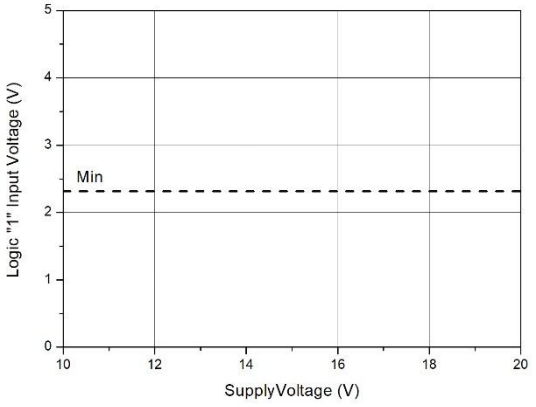


Figure 7B. Logic "1" Input Voltage vs. Supply Voltage

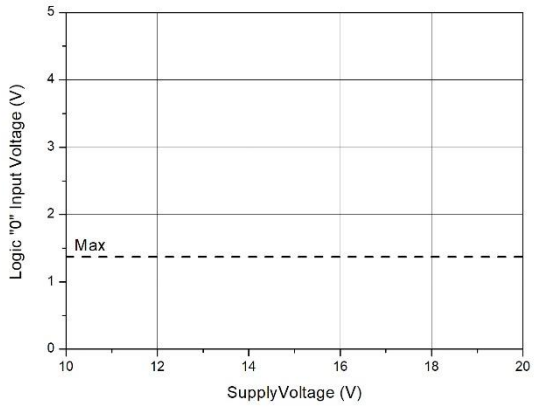


Figure 8B. Logic "0" Input Voltage vs. Supply Voltage

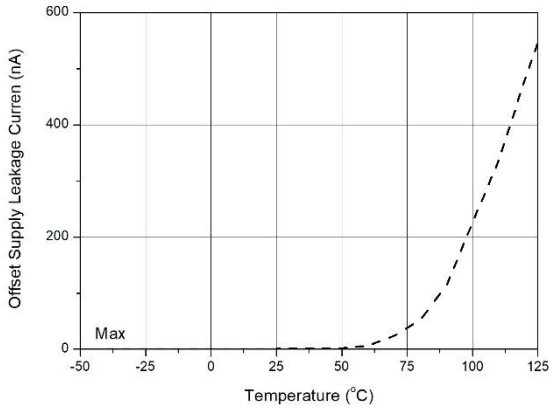


Figure 11A. Offset Supply Leakage Current vs. Temperature

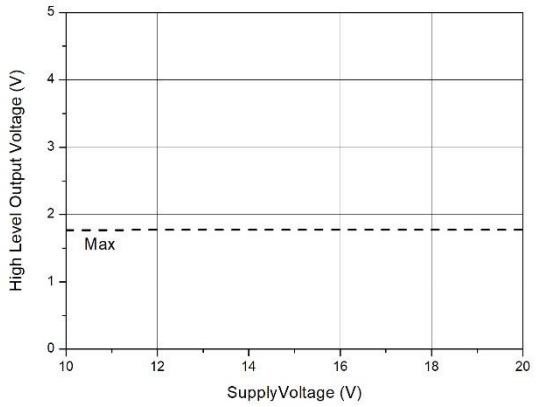


Figure 9B. High Level Output Voltage vs. Supply Voltage (Io = 0mA)

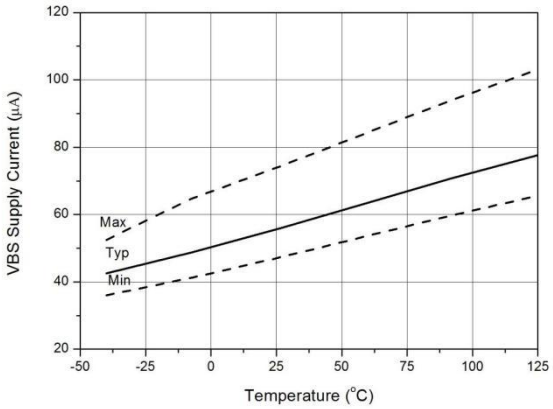


Figure 12A. VBS Supply Current vs. Temperature

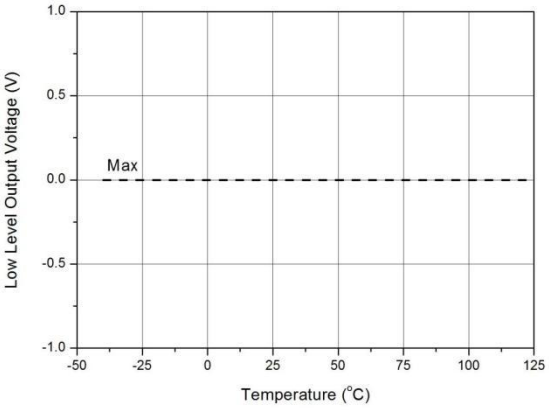


Figure 10A. Low Level Output vs. Temperature

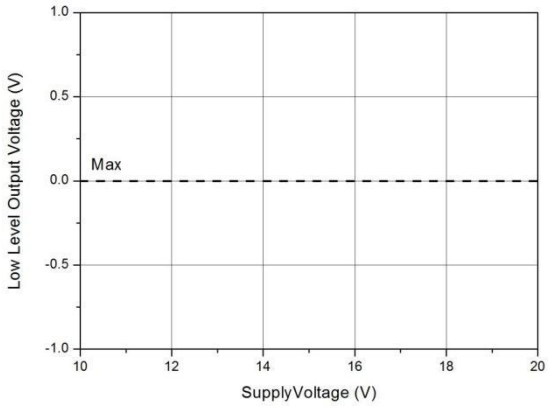


Figure 10B. Low Level Output vs. Supply Voltage

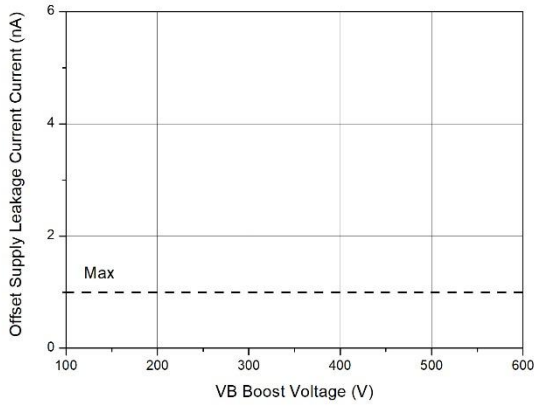


Figure 11B. Offset Supply Leakage Current vs. VB Boost Voltage

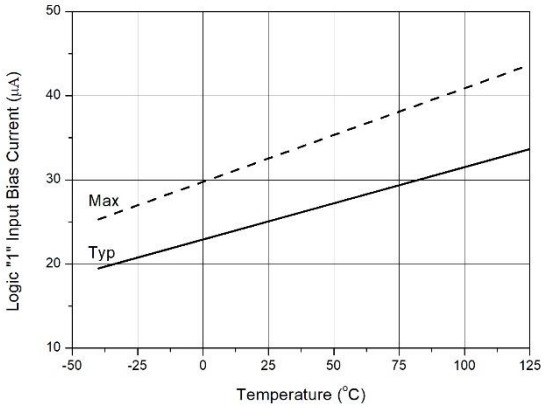


Figure 14A. Logic "1" Input Bias Current vs. Temperature

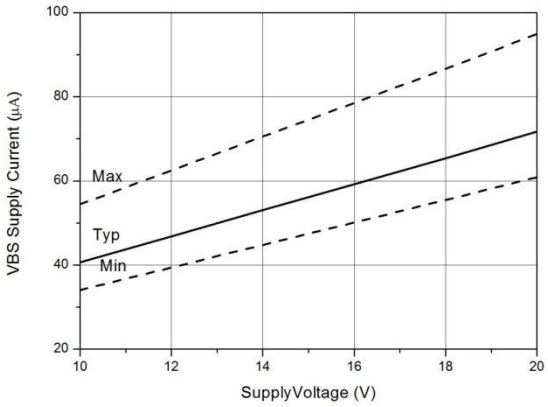


Figure 12B. VBS Supply Current vs. VBS Floating Supply Voltage

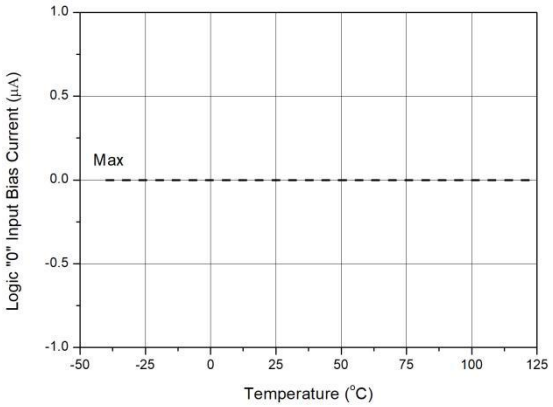


Figure 15A. Logic "0" Input Bias Current vs. Temperature

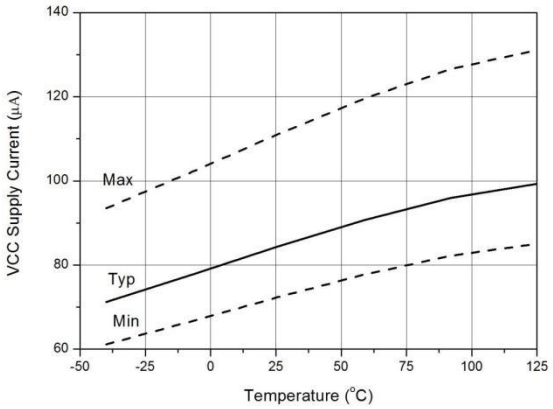


Figure 13A. VCC Supply Current vs. Temperature

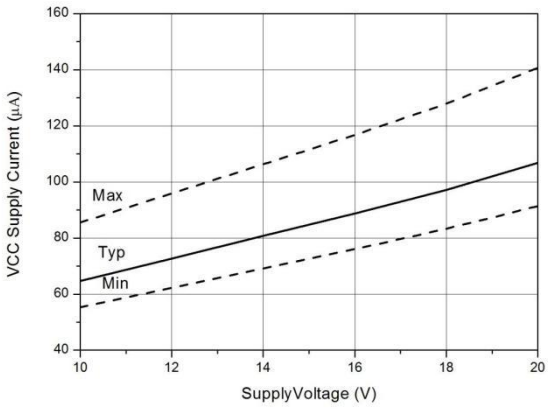


Figure 13B. VCC Supply Current vs. Supply Voltage

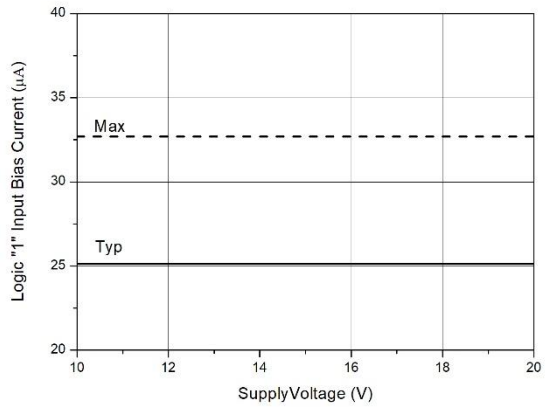


Figure 14B. Logic "1" Input Bias Current vs. Supply Voltage

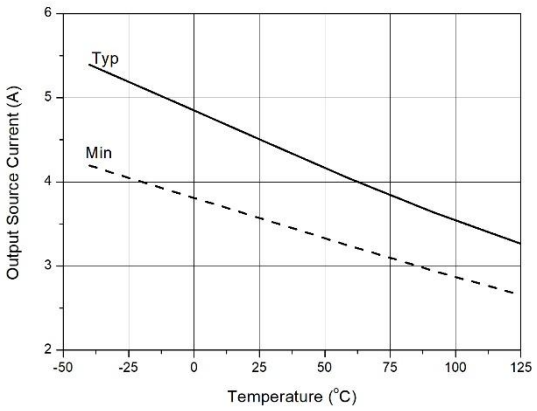


Figure 18A. Output Source Current vs. Temperature

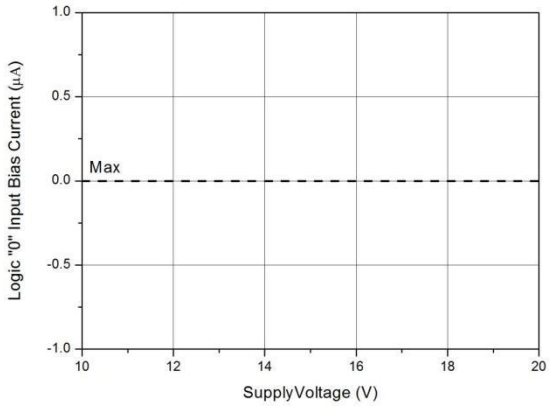


Figure 15B. Logic "0" Input Bias Current vs. Supply Voltage

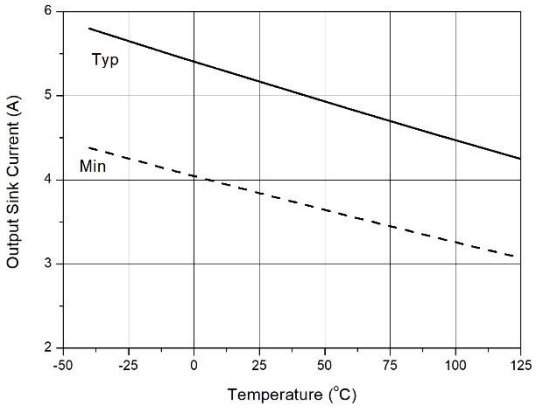


Figure 19A. Output Sink Current vs. Temperature

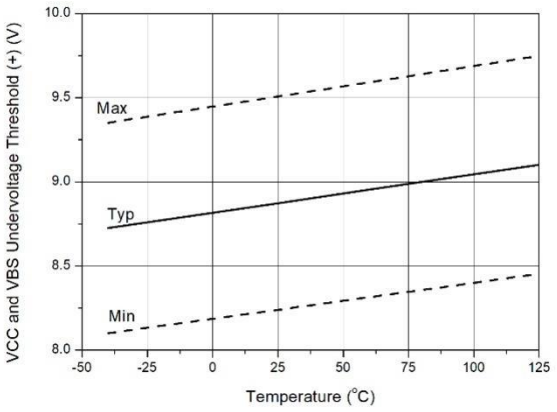


Figure 16. VCC and VBS Undervoltage Threshold (+) vs. Temperature

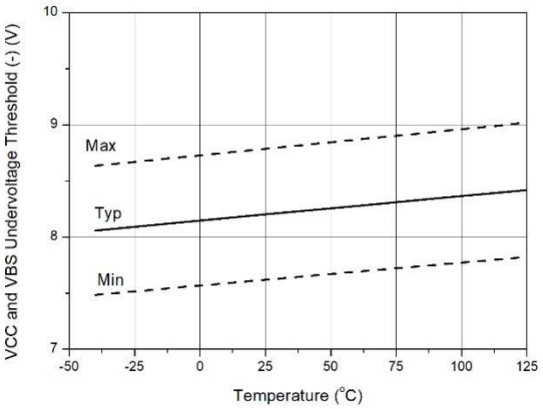


Figure 17. VCC and VBS Undervoltage Threshold (-) vs. Temperature

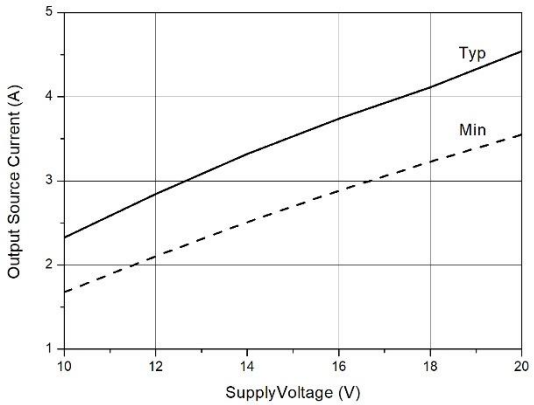


Figure 18B. Output Source Current vs. Supply Voltage

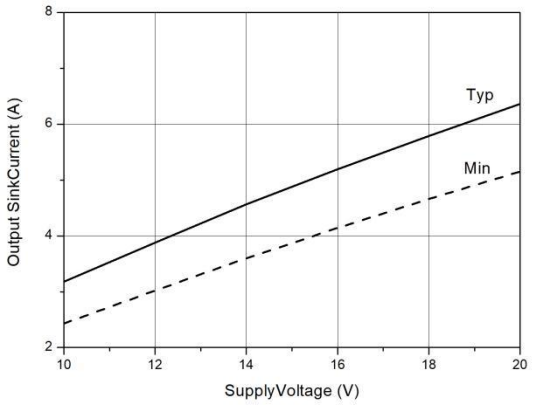


Figure 19B. Output Sink Current vs. Supply Voltage

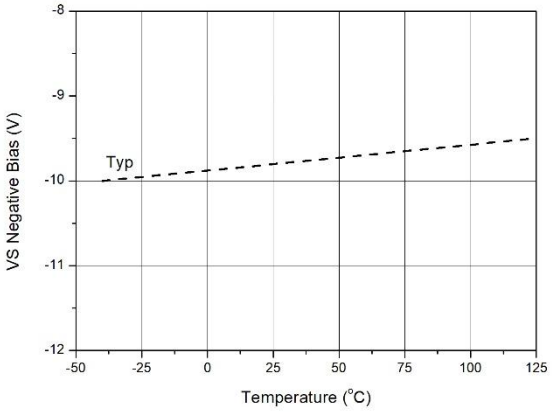


Figure 20. VS Negative Bias vs. Temperature

Function Block Diagram

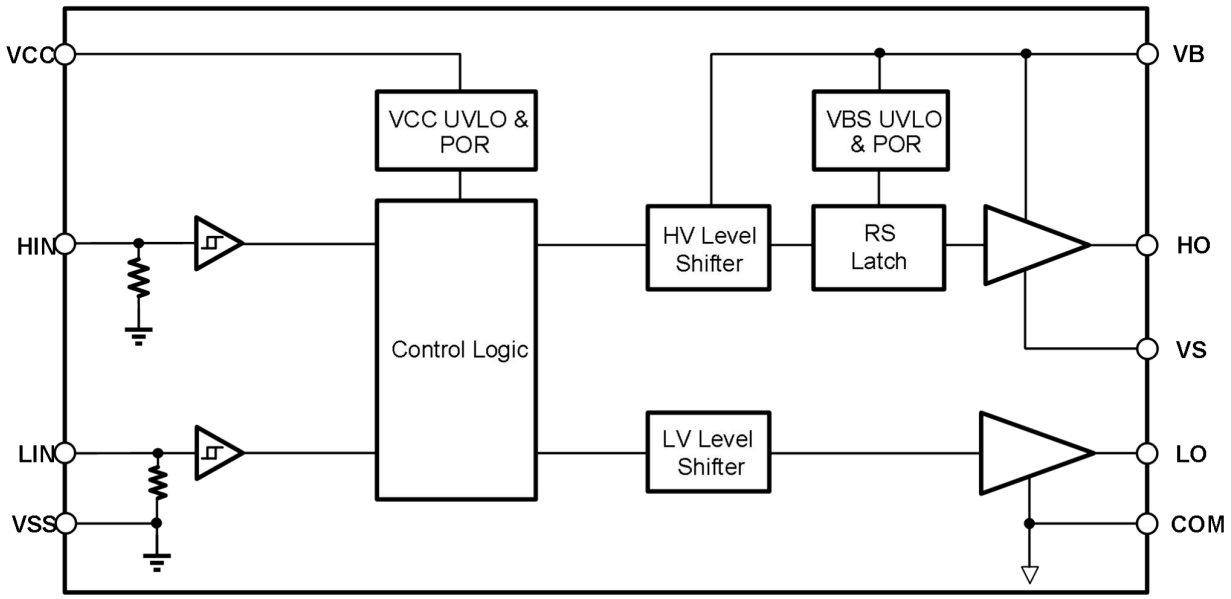


Figure 21. Function Block Diagram of IRS21814STR

Application message

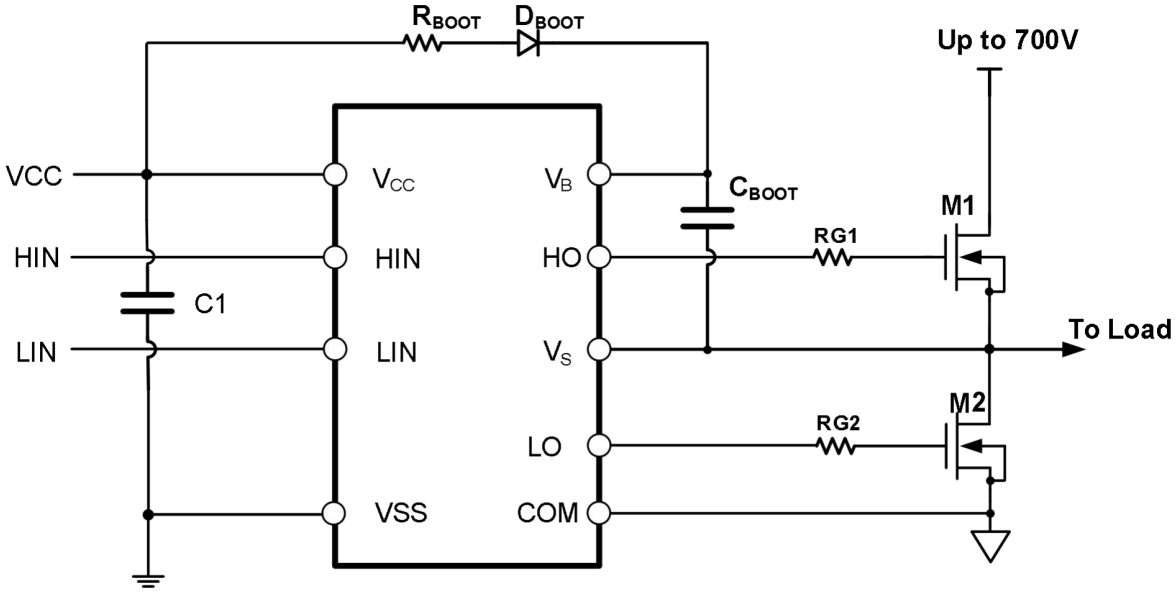
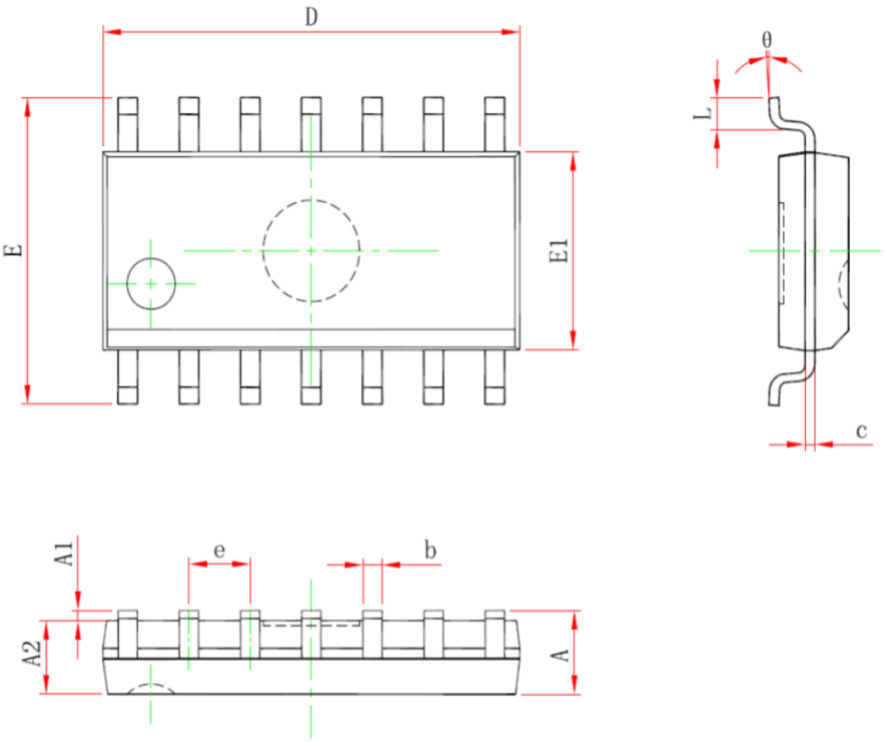


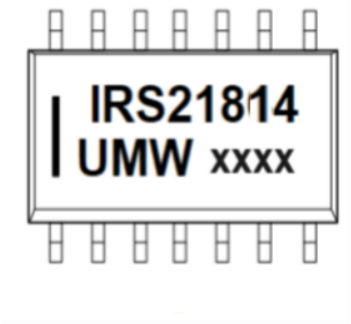
Figure 22. Typical application circuit of IRS21814STR

SOP-14



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.750	— —	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	— —	0.049	— —
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	8.450	8.850	0.333	0.348
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRS21814STR	SOP-14	2500	Tape and reel