

IPB60R090CFD7-VB Datasheet

N-Channel 600V (D-S) Super Junction Power MOSFET With Fast Diode

PRODUCT SUMMARY

V_{DS} (V) at T_J max.	600	
$R_{DS(on)}$ at 25 °C (Ω)	$V_{GS} = 10$ V	0.090

FEATURES

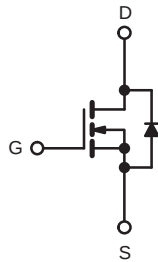
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Ultra-fast body diode
- Reduced switching and conduction losses
- Ultra low gate charge (Q_g)
- Avalanche energy rated (UIS)

**RoHS****APPLICATIONS**

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial

TO-263

Top View



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT	
Drain-Source Voltage			V_{DS}	600	V	
Gate-Source Voltage			V_{GS}	± 30		
Continuous Drain Current ($T_J = 150$ °C)	V_{GS} at 10 V	$T_C = 25$ °C	I_D	31	A	
		$T_C = 100$ °C		19		
Pulsed Drain Current ^a			I_{DM}	93		
Linear Derating Factor				1.67	W/°C	
Single Pulse Avalanche Energy ^b			E_{AS}	1400	mJ	
Maximum Power Dissipation			P_D	170	W	
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C	
Drain-Source Voltage Slope	$T_J = 125$ °C		dV/dt	50	V/ns	
Reverse Diode dV/dt ^d				15		
Soldering Recommendations (Peak Temperature) ^c			for 10 s	260	°C	

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature.
 b. $V_{DD} = 100$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω , $I_{AS} = 8$ A.
 c. 1.6 mm from case.
 d. $I_{SD} \leq I_D$, $dI/dt = 100$ A/ μ s, starting $T_J = 25$ °C.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.57	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static								
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$		600	-	-	V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C , $I_D = 1\text{ mA}$		-	0.70	-	V/°C	
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.5	-	4.5	V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA	
		$V_{GS} = \pm 30\text{ V}$		-	-	± 1	μA	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=600\text{ V}, V_{GS}=0\text{ V}$		-	-	1	μA	
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ °C}$		-	-	100		
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$	-	0.090	-	Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 30\text{ V}, I_D = 10\text{ A}$		-	5.6	-	S	
Dynamic								
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V},$ $V_{DS} = 100\text{ V},$ $f = 1\text{ MHz}$		-	3300	-	pF	
Output Capacitance	C_{oss}			-	80	-		
Reverse Transfer Capacitance	C_{rss}			-	4	-		
Effective Output Capacitance, Energy Related ^a	$C_{o(er)}$	$V_{DS} = 0\text{ V to } 520\text{ V}, V_{GS} = 0\text{ V}$		-	63	-		
Effective Output Capacitance, Time Related ^b	$C_{o(tr)}$			-	213	-		
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 8\text{ A}, V_{DS} = 520\text{ V}$	-	82	-	nC	
Gate-Source Charge	Q_{gs}			-	15	-		
Gate-Drain Charge	Q_{gd}			-	19	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 520\text{ V}, I_D = 8\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 9.1\text{ }\Omega$		-	18	25	ns	
Rise Time	t_r			-	24	55		
Turn-Off Delay Time	$t_{d(off)}$			-	80	-		
Fall Time	t_f			-	12	-		
Gate Input Resistance	R_g	$f = 1\text{ MHz}, \text{ open drain}$		-	0.8	-	Ω	
Drain-Source Body Diode Characteristics								
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	31	A	
Pulsed Diode Forward Current	I_{SM}			-	-	93		
Diode Forward Voltage	V_{SD}	$T_J = 25\text{ °C}, I_S = 8\text{ A}, V_{GS} = 0\text{ V}$		-	-	1.5	V	
Reverse Recovery Time	t_{rr}	$T_J = 25\text{ °C}, I_F = I_S = 8\text{ A},$ $dI/dt = 100\text{ A}/\mu\text{s}, V_R = 400\text{ V}$		-	475	-	ns	
Reverse Recovery Charge	Q_{rr}			-	5.8	-	μC	
Reverse Recovery Current	I_{RRM}			-	30	-	A	

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .
 b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

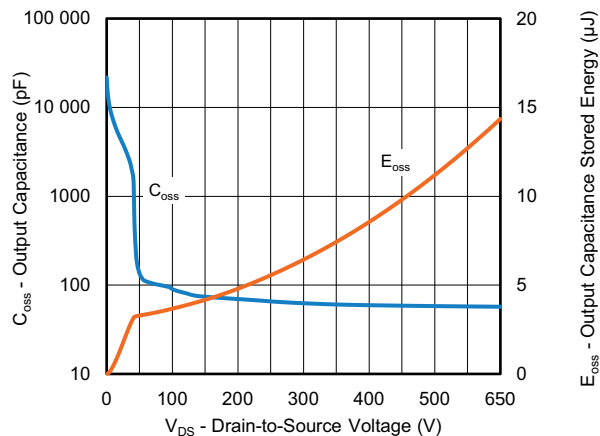
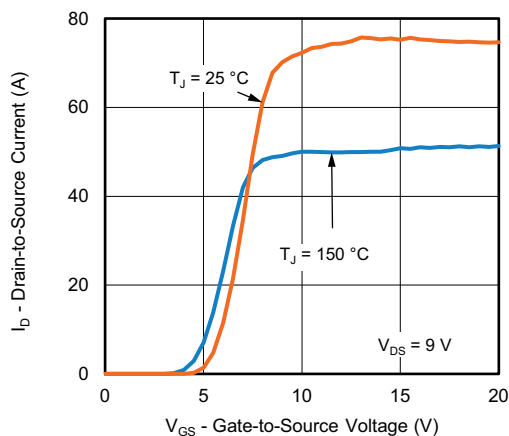
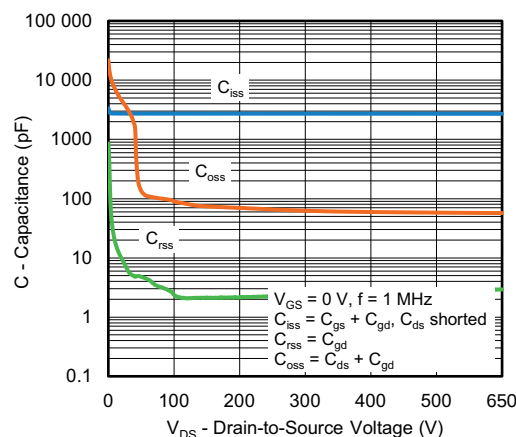
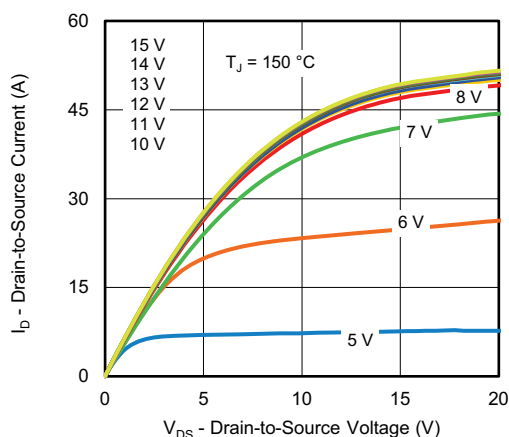
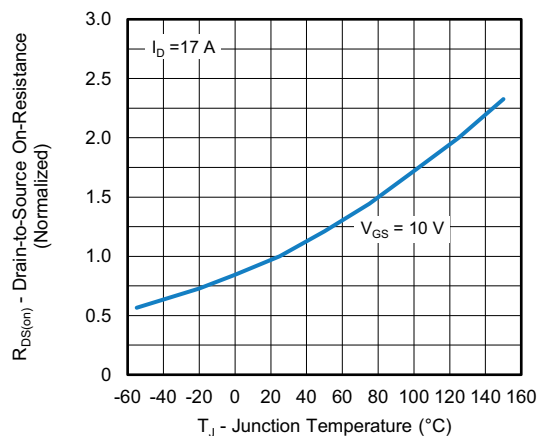




Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage



Fig. 10 - Maximum Drain Current vs. Case Temperature



Fig. 8 - Typical Source-Drain Diode Forward Voltage



Fig. 11 - Temperature vs. Drain-to-Source Voltage



Fig. 9 - Maximum Safe Operating Area

Note

- a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

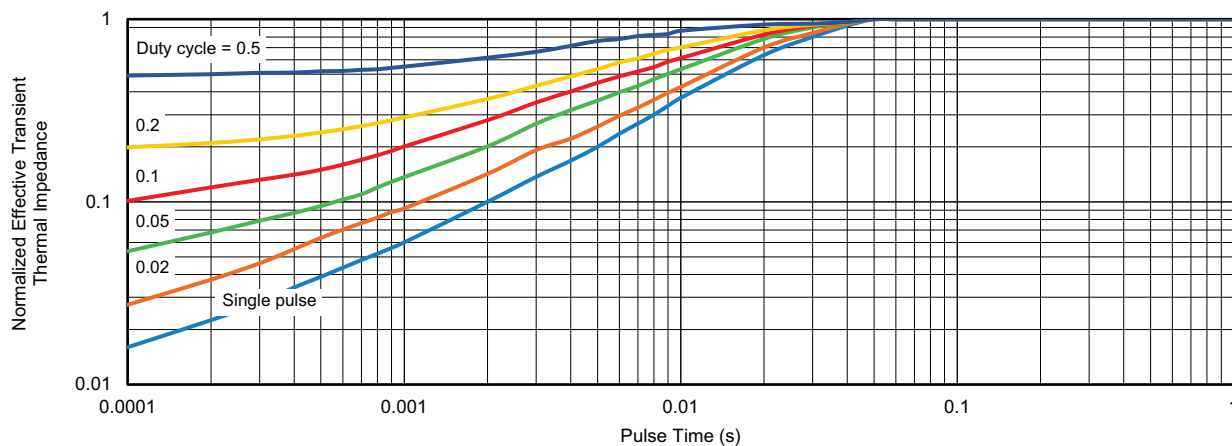


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

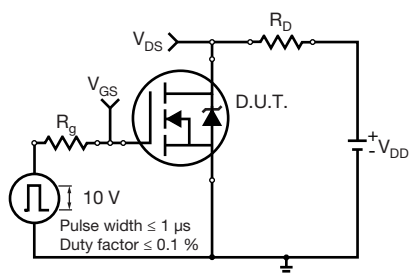


Fig. 13 - Switching Time Test Circuit

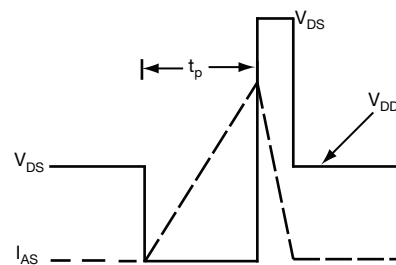


Fig. 16 - Unclamped Inductive Waveforms

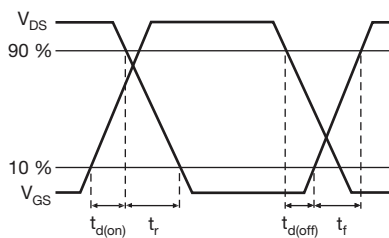


Fig. 14 - Switching Time Waveforms

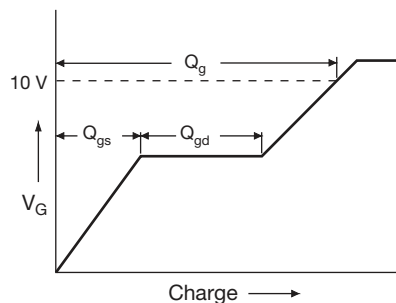


Fig. 17 - Basic Gate Charge Waveform

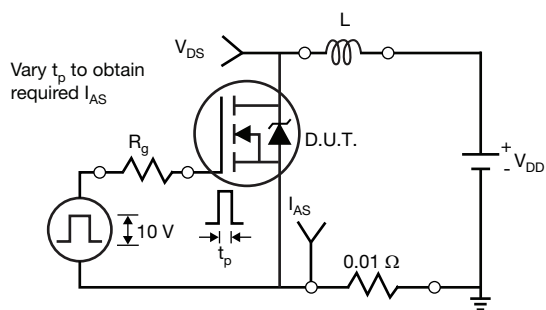


Fig. 15 - Unclamped Inductive Test Circuit

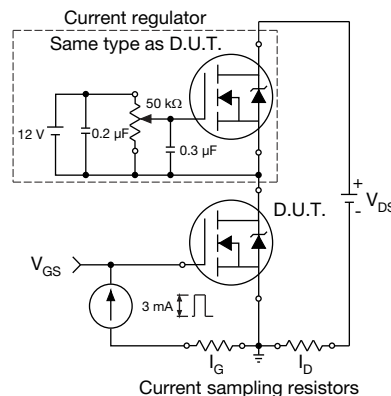
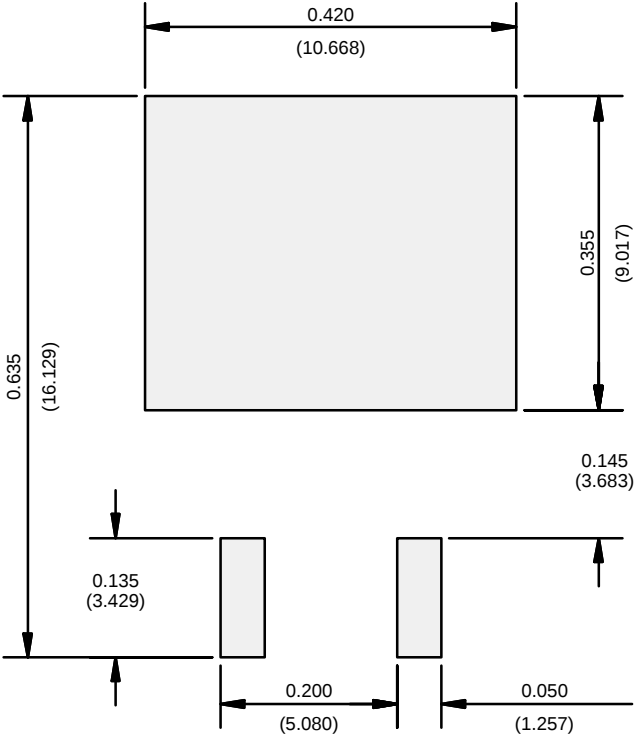


Fig. 18 - Gate Charge Test Circuit

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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