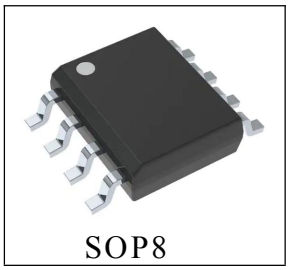
D1302
Trickle Charge Timekeeping Circuit

General Description

The D1302 Trickle Charge Timekeeping Chip contains an RTC/calendar and 31 bytes of static RAM. It communicates with a microprocessor via a simple serial interface. The RTC/calendar provides seconds, minutes, hours, day, date, month, and year information. The end of the month date is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in either the 24-hour or 12-hour format with an AM/PM indicator.


SOP8

Interfacing the D1302 with a microprocessor is simplified by using synchronous serial communication. Only three wires are required to communicate with the clock/RAM: 1) RST (reset), 2) I/O (data line), and3) SCLK (serial clock). Data can be transferred to and from the clock/RAM 1 byte at a time or in a burst of up to 31 bytes. The D1302 is designed to operate on very low power and retain data and clock information on less than 1 microwatt.

The D1302 is available in standard SOP8 package.

Features

- Real-time clock (RTC) counts seconds, minutes hours, date of the month, month, day of the week, and year with leap-year compensation valid up to 2100
- 31-byte, battery-backed, nonvolatile (NV) RAM for data storage
- Serial I/O for minimum pin count
- 2.0V to 5.5V full operation
- Uses less than 300nA at 2.0V
- Burst mode for reading/writing successive addresses in clock/RAM
- Simple 3-wire interface
- TTL-compatible (V_{CC} = 5V)
- Optional temperature range: -40℃ to +85℃

Package Information

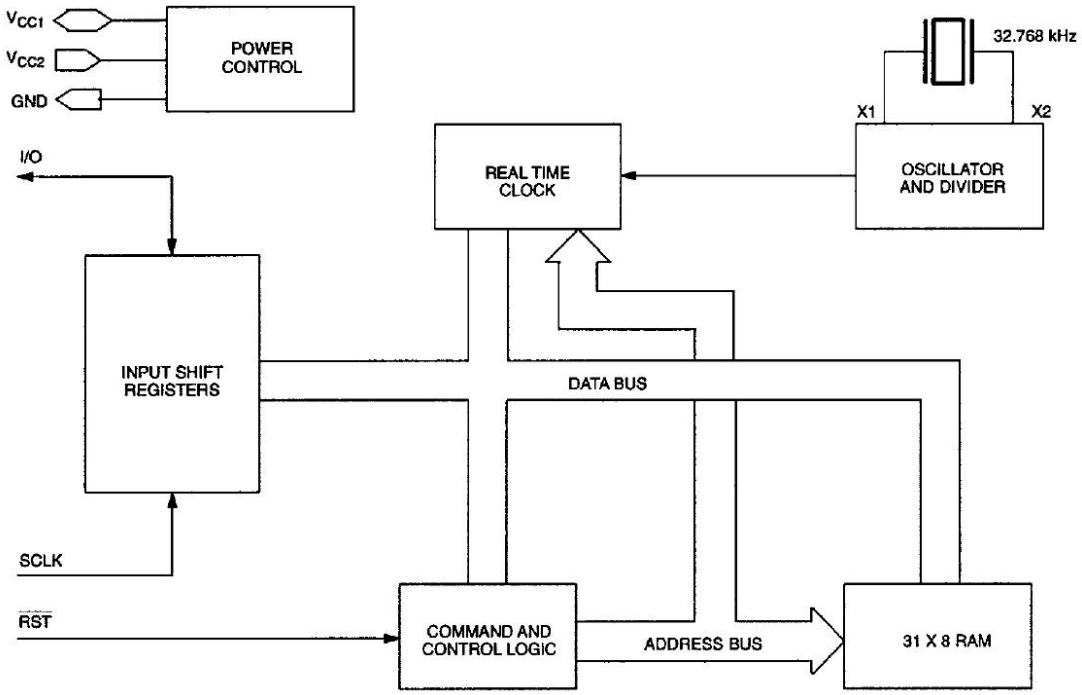
PART NO.	PACKAGE DESCRIPTION	PACKAGE MARKING	PACKAGE OPTION
D1302F	SOP8	CHMC D1302F SXXXX	100/Tube 4000/Reel

CHMC:Trademark D1302F:Part NO. SXXXX:Lot NO.

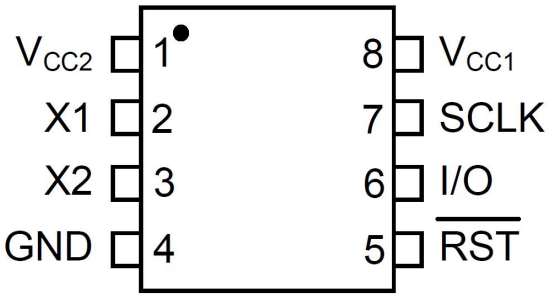
Applications

- Clock Chip
- Mobile Telephone
- Portable Instruments

Functional Block Diagram



Pin Configuration



D1302(SOP8)

Pin Description

Pin Number	Pin Name	Function Description
1	V_{CC2}	V_{CC2} is the primary power supply pin in a dual-supply configuration.V_{CC1} is connected to a backup source to maintain the time and date in the absence of primary power. The D1302 will operate from the larger of V_{CC1} or V_{CC2}. When V_{CC2} is greater than V_{CC1}+0.2V, V_{CC2} will power the D1302.When V_{CC2} is less than V_{CC1}, V_{CC1} will power the D1302.
2,3	X_1,X_2	Connections for a standard 32.768kHz quartz crystal. The internal oscillator is designed for operation with a crystal having a specified load capacitance of 6pF. The D1302 can also be driven by an external 32.768kHz oscillator. In this configuration, the X_1 pin is connected to the external oscillator signal and the X_2 pin is floated.
4	GND	Ground
5	$\overline{RST}$	Reset. The reset signal must be asserted high during a read or a write. This pin has a 40kΩ internal pull-down resistor
6	I/O	Data Input/Output. The I/O pin is the bi-directional data pin for the 3-wire interface. This pin has a 40kΩ internal pull-down resistor.
7	SCLK	Serial Clock Input. SCLK is used to synchronize data movement on the serial interface. This pin has a 40kΩ internal pull-down resistor.
8	V_{CC1}	V_{CC1} provides low-power operation in single supply and battery-operated systems as well as low-power battery backup. In systems using the trickle charger, the rechargeable energy source is connected to this pin. UL recognized to ensure against reverse charging current when used in conjunction with a lithium battery.

Absolute Maximum Ratings

Parameter Name	Symbol	Value	Unit
Voltage on Any Pin Relative to Ground	Vpin	-0.5～+7.0	V
Storage Temperature	Tstg	-55～+125	℃
Soldering Temperature (10Sec)	Tjm	260	℃
Optional Temperature Range	Topr	-40～+85	℃

*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Recommended DC Operating Conditions

Parameter Name	Symbol	Conditions	Min	Max	Unit
Supply Voltage *1	V_{CC1} ,V_{CC2}		2.0	5.5	V
Logic 1 Input	V_{IH}		2.0	Vcc+0.3	V
Logic 0 Input	V_{IL}	V_{CC}=2.0V	-0.3	+0.3	V
		V_{CC}=5.0V	-0.3	+0.8	

***1** V_{CC} = V_{CC2} , when V_{CC2} > V_{CC1} + 0.2V;V_{CC} = V_{CC1} , when V_{CC1} > V_{CC2} .

DC Electrical Characteristics

Parameter Name		Symbol	Test Conditions	Min	Typ	Max	Unit
Input Leakage *3		I_{LI}				+500	μA
I/O Leakage *3		I_{LO}				+500	μA
Logic 1 Output	I_{OH} = -0.4mA	V_{OH}	V_{CC} =2.0V	1.6			V
	I_{OH} = -1.0mA		V_{CC} =5V	2.4			
Logic 0 Output	I_{OL} = 1.5mA	V_{OL}	V_{CC} =2.0V			0.4	V
	I_{OL} = 4.0mA		V_{CC} =5V			0.4	
Active Supply Current *2,9		I_{CC1A}	V_{CC} =2.0V			0.4	mA
			V_{CC}=5V			1.2	
Timekeeping Current (OSC On) *1,9		I_{CC1T}	V_{CC} =2.0V			0.3	μA
			V_{CC} =5V			1	
Standby Current (OSC Off) *7,8,9		I_{CC1S}	V_{CC}=2.0V			100	nA
			V_{CC} =5V			100	
			IND			200	
Active Supply Current *2,10		I_{CC2A}	V_{CC2} =2.0V			0.425	mA
			V_{CC2} =5.0V			1.28	
Timekeeping Current (OSC On) *1,10		I_{CC2T}	V_{CC2} =2.0V			25.3	μA
			V_{CC2} =5.0V			81	
Standby Current (OSC Off) *7,10		I_{CC2S}	V_{CC2} =2.0V			25	μA
			V_{CC2} =5.0V			80	
Trickle Charge Resistors		R_1			2		kΩ
		R_2			4		
		R_3			8		
Trickle Charge Diode Voltage Drop		V_{TD}			0.7		V

Capacitance (Ta=25℃)

Parameter Name	Symbol	Min	Typ	Max	Unit
Input Capacitance	C_I		10		pF
I/O Capacitance	$C_{I/O}$		15		pF
Crystal Capacitance	C_X		6		pF

AC Electrical Characteristics

Parameter Name	Symbol	Test conditions	Min	Typ	Max	Unit
Data to CLK Setup *4	t_{DC}	V_{CC}=2.0V	200			ns
		V_{CC}=5V	50			
CLK to Data Hold *4	t_{CDH}	V_{CC}=2.0V	280			ns
		V_{CC}=5V	70			
CLK to Data Delay *4,5,6	t_{CDD}	V_{CC}=2.0V			800	ns
		V_{CC}=5V			200	
CLK Low Time *4	t_{CL}	V_{CC}=2.0V	1000			ns
		V_{CC}=5V	250			
CLK High Time *4	t_{CH}	V_{CC}=2.0V	1000			ns
		V_{CC}=5V	250			
CLK Frequency *4	t_{CLK}	V_{CC}=2.0V			0.5	MHz
		V_{CC}=5V	DC		2.0	
CLK Rise and Fall *4	t_R , t_F	V_{CC}=2.0V			2000	ns
		V_{CC}=5V			500	
$\overline{RST}$ to CLK Setup *4	t_{CC}	V_{CC}=2.0V	4			μs
		V_{CC}=5V	1			
CLK to $\overline{RST}$ Hold *4	t_{CCH}	V_{CC}=2.0V	240			ns
		V_{CC}=5V	60			
$\overline{RST}$ Inactive Time *4	t_{CWH}	V_{CC}=2.0V	4			μs
		V_{CC}=5V	1			
$\overline{RST}$ to I/O High-Z *4	t_{CDZ}	V_{CC}=2.0V			280	ns
		V_{CC}=5V			70	
SCLK to I/O High-Z *4	t_{CCZ}	V_{CC}=2.0V			280	ns
		V_{CC}=5V			70	

*1. I_{CC1T} and I_{CC2T} are specified with I/O open, $\overline{RST}$ set to a logic 0, and clock halt flag = 0 (oscillator enabled).

*2. I_{CC1A} and I_{CC2A} are specified with the I/O pin open, RST high, SCLK=2MHz at V_{CC} = 5V; SCLK = 500kHz, V_{CC} = 2.0V, and clock halt flag = 0 (oscillator enabled).

*3. $\overline{RST}$, SCLK, and I/O all have 40kΩ pull-down resistors to ground.

*4. Measured at V_{IH} = 2.0V or V_{IL} = 0.8V and 10ns maximum rise and fall time.

*5. Measured at V_{OH} = 2.4V or V_{OL} = 0.4V.

*6. Load capacitance = 50pF.

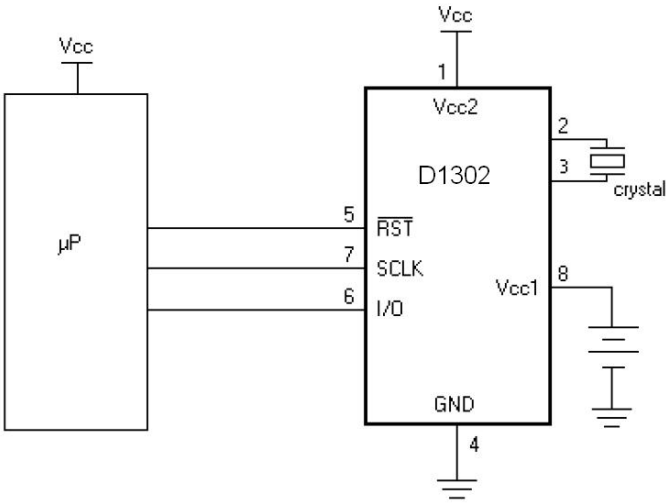
*7. I_{CC1S} and I_{CC2S} are specified with $\overline{RST}$, I/O, and SCLK open. The clock halt flag must be set to logic one (oscillator disabled).

*8 Typical values are at 25°C.

*9. V_{CC2} = 0V.

*10. V_{CC1} = 0V.

Typical Application



Application Information

Clock Accuracy

The accuracy of the clock is dependent upon the accuracy of the crystal and the accuracy of the match between the capactive load of the oscillator circuit and the capacitive load for which the crystal was trimmed. Additional error will be added by crystal frequency drift caused by temperature shifts. External circuit noise coupled into the oscillator circuit may result in the clock running fast.

Command Byte

The command byte is shown in table below. Each data transfer is initiated by a command byte. The MSB(Bit 7) must be a logic 1. If it is 0, writes to the D1302 will be disabled. Bit 6 specifies clock/calendar data if logic 0 or RAM data if logic 1. Bits 1 through 5 specify the designated registers to be input or output, and the LSB (bit 0) specifies a write operation (input) if logic 0 or read operation (output) if logic1. The command byte is always input starting with the LSB (bit 0).

Address/Command Byte

7	6	5	4	3	2	1	0
1	$RAM / \overline{CK}$	A4	A3	A2	A1	A0	$RD / \overline{W}$

Reset and Clock Control

All data transfers are initiated by driving the $\overline{RST}$ input high. The $\overline{RST}$ input serves two functions. First, $\overline{RST}$ turns on the control logic, which allows access to the shift register for the address/command sequence. Second, the $\overline{RST}$ signal provides a method of terminating either single byte or multiple byte data transfer.

A clock cycle is a sequence of a falling edge followed by a rising edge. For data inputs, data must be valid during the rising edge of the clock and data bits are output on the falling edge of clock. If the $\overline{RST}$ input is low all data transfer terminates and the I/O pin falling edge of clock. If the $\overline{RST}$ input is low all data transfer terminates and the I/O pin goes to a high impedance state. At power-up, RST must be a logic 0 until V_{CC}> 2.0V. Also SCLK must be at a logic 0 when $\overline{RST}$ is driven to a logic 1 state.

Data Input

Following the eight SCLK cycles that input a write command byte, a data byte is input on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored should they inadvertently occur. Data is input starting with bit 0.

Data Output

Following the eight SCLK cycles that input a read command byte, a data byte is output on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted occurs on the first falling edge after the last bit of the command byte is written. Additional SCLK cycles retransmit the data bytes should they inadvertently occur so long as $\overline{RST}$ remains high. This operation permits continuous burst mode read capability. Also, the I/O pin is tri-stated upon each rising edge of SCLK. Data is output starting with bit 0.

Burst Mode

Burst mode may be specified for either the clock/calendar or the RAM registers by addressing location 31 decimal (address/command bits 1 through 5 = logic 1). As before, bit 6 specifies clock or RAM and bit 0 specifies read or write. There is no data storage capacity at locations 9 through 31 in the Clock/Calendar Registers or location 31 in the RAM registers. Reads or writes in burst mode start with bit0 of address 0.

When writing to the clock registers in the burst mode, the first eight registers must be written in order for the data to be transferred. However, when writing to RAM in burst mode it is not necessary to write all 31 bytes for the data to transfer. Each byte that is written to will be transferred to RAM regardless of whether all 31 bytes are written or not.

Clock/Calendar

The clock/calendar is contained in seven write/read registers. Data contained in the clock/ calendar registers is in binary coded decimal format (BCD).

Clock Halt Flag

Bit 7 of the seconds register is defined as the clock halt flag. When this bit is set to logic 1, the clock oscillator is stopped and the D1302 is placed into a low-power standby mode with a current drain of less than 100 nanoamps. When this bit is written to logic 0, the clock will start. The initial power on state is not defined.

AM-PM/12-24 Mode

Bit 7 of the hours register is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic high being PM. In the24-hour mode, bit 5 is the second 10-hour bit (20–23 hours).

Write Protect Bit

Bit 7 of the control register is the write-protect bit. The first seven bits (bits 0–6) are forced to 0 and will always read a 0 when read. Before any write operation to the clock or RAM, bit 7 must be0. When high, the write protect bit prevents a write operation to any other register. The initial power on state is not defined. Therefore the WP bit should be cleared before attempting to write to the device.

Trickle Charge Register

This register controls the trickle charge characteristics of the D1302.The simplified schematic of Figure 5 shows the basic components of the trickle charger. The trickle charge select (TCS) bits(bits 4–7) control the selection of the trickle charger. In order to prevent accidental enabling, only a pattern of 1010 will enable the trickle charger. All other patterns will disable the trickle charger. The D1302 powers up with the trickle charger disabled. The diode select (DS) bits (bits 2–3) select whether one diode or two diodes are connected between V_{CC2} and V_{CC1} . If DS is 01, one diode is selected or if DS is 10, two diodes are selected. If DS is 00 or 11, the trickle charger is disabled independently of TCS. The RS bits (bits 0–1) select the resistor that is connected between V_{CC2} and V_{CC1}. The resistor selected by the resistor select (RS) bits is as follows:

RS Bits	Resistor	Typical Value
00	None	None
01	R1	2kΩ
10	R2	4kΩ
11	R3	8kΩ

If RS is 00, the trickle charger is disabled independently of TCS.

Diode and resistor selection is determined by the user according to the maximum current desired for battery or super cap charging. The maximum charging current can be calculated as illustrated in the following example. Assume that a system power supply of 5V is applied to V_{CC2} and a super cap is connected to V_{CC1}. Also assume that the trickle charger has been enabled with one diode and resistor R1 between V_{CC2} and V_{CC1} . The maximum current I_{MAX} would, therefore, be calculated as follows:

I_{MAX} = (5.0V - diode drop)/R1≈(5.0V - 0.7V) / 2kΩ≈2.2mA

As the super cap charges, the voltage drop between V_{CC1} and V_{CC2} will decrease and, therefore, the charge current will decrease.

Clock/Calendar Burst Mode

The clock/calendar command byte specifies burst mode operation. In this mode the first eight clock/calendar registers can be consecutively read or written starting with bit 0 of address 0.

If the write protect bit is set high when a write clock/calendar burst mode is specified, no data transfer will occur to any of the eight clock/calendar registers (this includes the control register). The trickle charger is not accessible in burst mode.

At the beginning of a clock burst read, the current time is transferred to a second set of registers. The time information is read from these secondary registers, while the clock may continue to run. This eliminates the need to re-read the registers in case of an update of the main registers during a read.

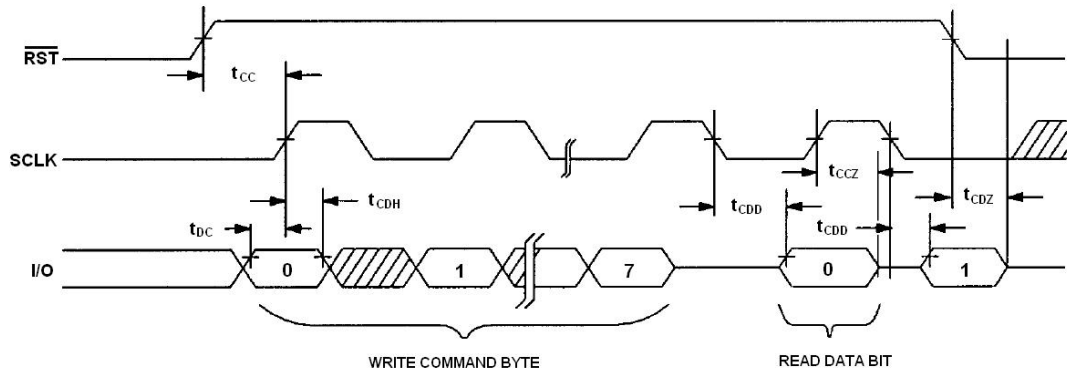
Ram

The static RAM is 31 x 8 bytes addressed consecutively in the RAM address space.

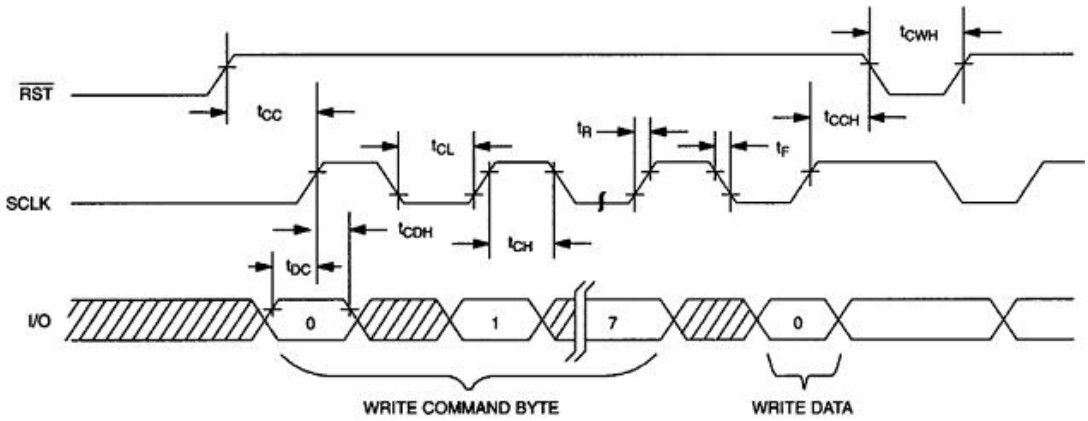
Ram Burst Mode

The RAM command byte specifies burst mode operation. In this mode, the 31 RAM registers can be consecutively read or written (See Figure 4) starting with bit 0 of address 0.

Timing Diagram: Read Data Transfer

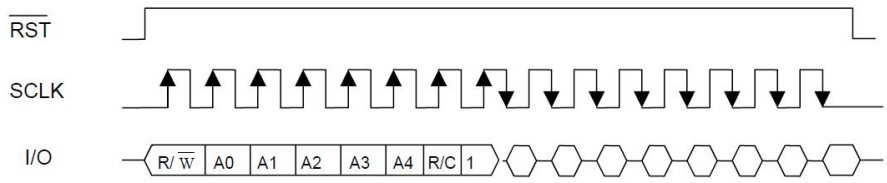


Timing Diagram: Write Data Transfer

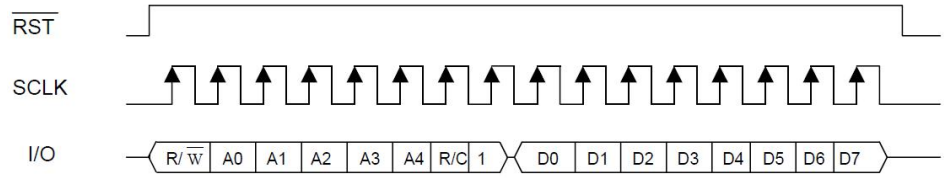


Data Transfer Summary

Single Byte Read

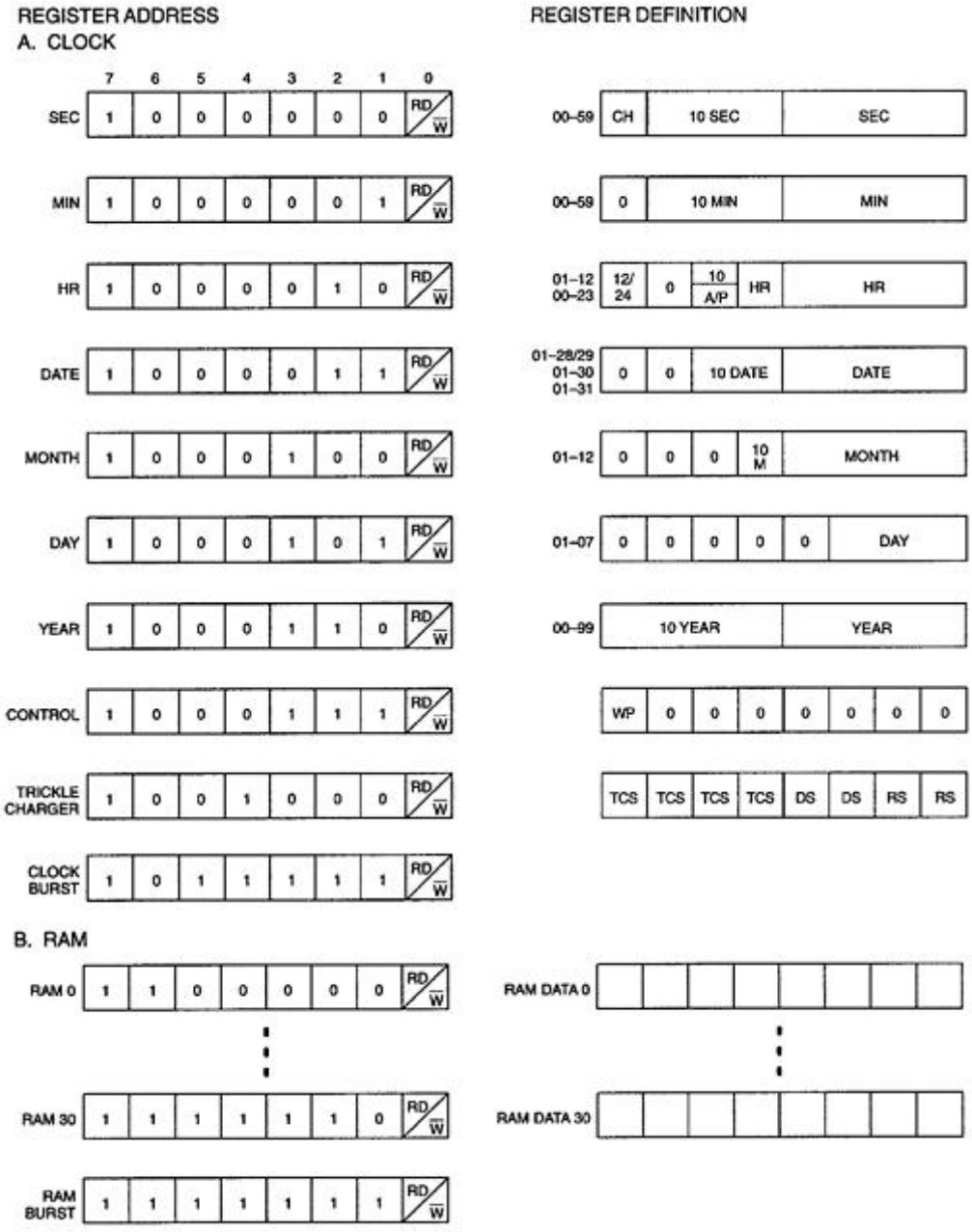


Single Byte Write

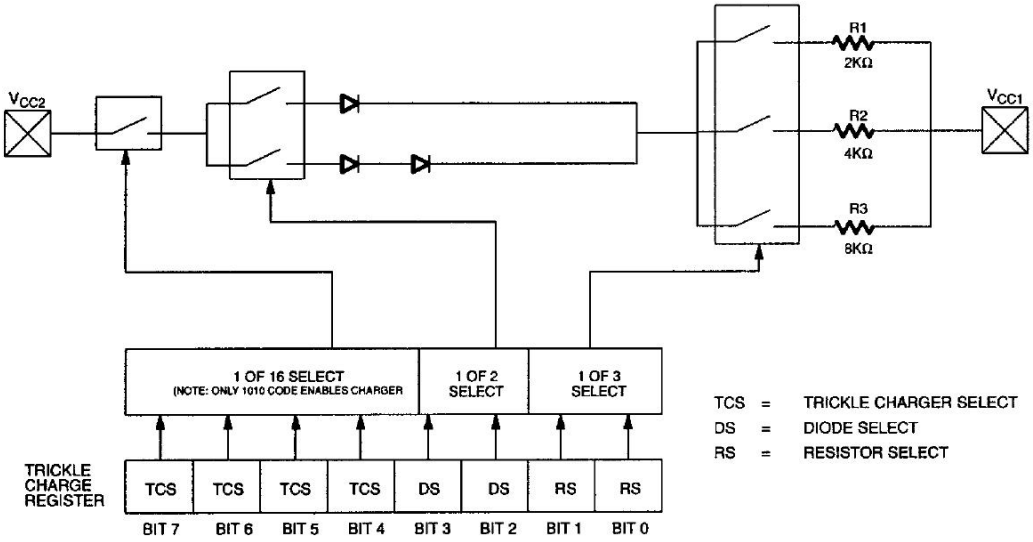


In burst mode, $\overline{RST}$ is kept high and additional SCLK cycles are sent until the end of the burst.

Register Address/Definition

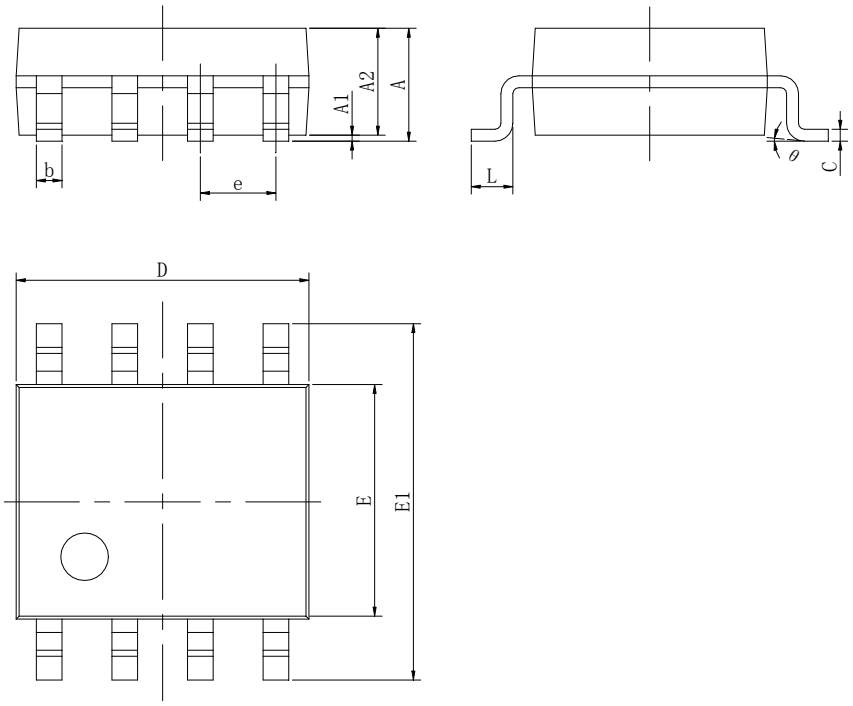


Programmable Trickle Charger



Outline Dimensions

SOP8 Unit:mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.800	0.053	0.071
A1	0.010	0.250	0.0003	0.010
A2	1.250	1.550	0.053	0.061
b	0.300	0.510	0.011	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Statements

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