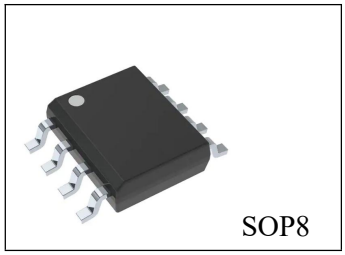
Silicore
芯谷科技

D8632

470μA 6MHz Rail-to-Rail I/O CMOS Operational Amplifier

General Description


SOP8

The D8632F(quad) is low noise, low voltage, and low power operational amplifier, that can be designed into a wide range of applications. The D8632F have a high gain-bandwidth product of 6MHz, a slew rate of 3.7V/μs, and a quiescent current of 470μA/ amplifier at 5V.

The D8632F is designed to provide optimal performance in low voltage and low noise systems. It provide s rail-to-rail output swing into heavy loads. The input common-mode voltage range includes ground, and the maximum input offset voltage are 3.5m V for D8632F.

It is specified over the extended industrial temperature range (-40℃ to + 125 ℃). The operating range is from 2.5V to 5.5V.

D8632F is available in sop8 package.

Features

- Low Cost
- Rail-to-Rail Input and Output: 0. 8m V Typical VOS
- High Gain- Bandwidth Product: 6 MHz
- High Slew Rate: 3.7V/μs
- Settling Time to 0.1% with 2V Step: 2.1μs
- Overload Recovery Time: 0.9μs
- Low Noise : 12nV/ √Hz
- Operates on 2. 5V to 5 . 5V Supplies
- Input Voltage Range = -0.1V to + 5 .6V with VS = 5.5V
- Low Power: 470μA/Amplifier Typical Supply Current

Package Information

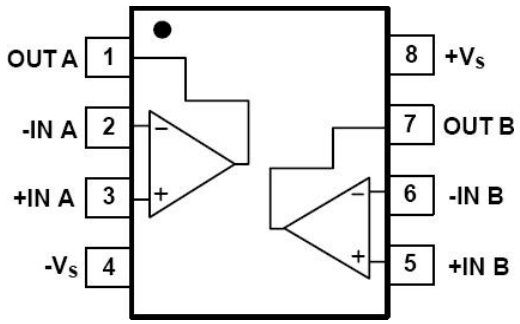
Part NO.	Package Description	Package Marking	Package Option
D8632F	SOP8	CHMC D8632F SXXXX	100/Tube 4000/Reel

CHMC:Trademark D8632F:Part NO. SXXXX:Lot NO.

Applications

- Sensors
- Audio
- Active Filters
- A/D Converters
- Communications
- Test Equipment
- Cellular and Cordless Phones
- Laptops and PDAs
- Photodiode Amplification
- Battery-Powered Instrumentation

Pin Connection



D8632F(SOP8)

Absolute Maximum Ratings

Characteristic		Value	Unit
Supply Voltage		7.5	V
Common- Mode Input Voltage		(-Vs)-0.5V～(+Vs)+0.5V	V
Operating Temperature		-55 ～+150	°C
Storage Temperature		-65 ～+150	°C
Junction Temperature		160	°C
Lead Temperature Range (soldering 10sec)		260	°C
ESD Susceptibility	HBM	1500	V
	MM	400	V

Electrical Characteristics

(unless otherwise specified: V_S =+ 5 V, V_{CM} = V_S /2,R_L =600 Ω,T_A =25 °C)

Characteristics	Symbol	Test conditions	Min	Typ	Max	Unit
Input Characteristics						
Input Offset Voltage	V_{OS}			0.8	3.5	mV
Input Bias Current	I_B			1		pA
Input Offset Current	I_{OS}			1		pA
Common-Mode Voltage	V_{CM}	Vs=5.5V	-0.1 to +5.6(typ.)			V
Common-Mode Rejection Ratio	CMRR	Vs=5.5V,V_{CM} =-0.1V to 4V	75	90		dB
		Vs=5.5V,V_{CM} =-0.1V to 5.6V		83		dB
Open-Loop Voltage Gain	A_{OL}	R_L=600Ω,V_O=0.15V to 4.85V	90	97		dB
		R_L=10kΩ,V_O=0.05V to 4.95V		108		dB
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2.4		μV/℃
Output Characteristics						
Output Voltage Swing from Rail		R_L=600Ω		0.1		V
		R_L=10kΩ,		0.015		V
Output Current	I_{OUT}		49	53		mA
Closed-Loop Output Impedance		f= 200 kHz, G= 1		3		Ω
Power- down Disable						
Turn-on Time				4		μs
Turn-off Time				1.2		μs
$\overline{\text{DISABLE}}$ Voltage-off					0.8	V
DISABLE Voltage-on			2			V
Power Supply						
Operating Voltage Range			2.5		5.5	V
Power Supply Rejection Ratio	PSRR	Vs=+2.5V to +5.5 V V_{CM} =(-Vs)+0.5V	80	91		dB
Quiescent Current/Amplifier	I_Q	I_{OUT} =0		470	590	μA
Dynamic Performance						
Gain-Bandwidth Product	GBP	R_L=10kΩ		6		MHz
Phase Margin	φ_O			60		degress
Full Power Bandwidth	BWp	<1% distortion, R_L=600Ω		250		kHz
Slew Rate	SR	G=+1.2V Step, R_L=10kΩ		3.7		V/μs
Setting Time to 0.1%	ts	G=+1.2V Step, R_L=600Ω		2.1		μs
Overload Recovery Time		V_{IN} ·Gain= Vs, R_L=600Ω		0.9		μs
Noise Performance						
Voltage Noise Density	e_n	f=1kHz		12		$nV/\sqrt{Hz}$
Current Noise Density	i_n	f=1kHz		3		$fA/\sqrt{Hz}$

Applications Summary

Driving Capacitive Loads

The D8632F can directly drive 1000pF in unity- gain without oscillation. The unity-gain follower (buffer) is the most sensitive configuration to capacitive loading. Direct capacitive loading reduces the phase margin of amplifiers and this results in ringing or even oscillation.

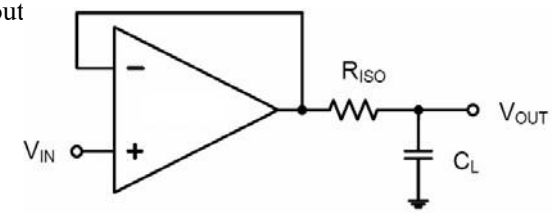


Figure 1. Indirectly Driving Heavy Capacitive Load

Applications that require greater capacitive drive capability should use an isolation resistor between the output and the capacitive load like the circuit in Figure 1.

The isolation resistor R_{ISO} and the load capacitor C_L form a zero to increase stability. The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. Note that this method results in a loss of gain accuracy because R_{ISO} forms a voltage divider with the R_{LOAD} .

An improvement circuit is shown in Figure 2. It provides DC accuracy as well as AC stability. RF provides the DC accuracy by connecting the inverting signal with the output. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving phase margin in the overall feedback loop.

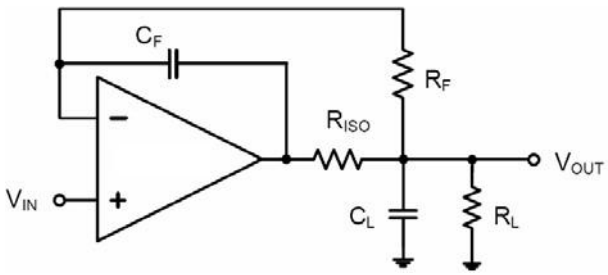


Figure 2. Indirectly Driving Heavy Capacitive Load with DC Accuracy

For no-buffer configuration, there are two others ways to increase the phase margin: (a) by increasing the amplifier's gain or (b) by placing a capacitor in parallel with the feedback resistor to counteract the parasitic capacitance associated with inverting node.

Power-Supply Bypassing and Layout

The D8632F family operates from either a single +2. 5 V to +5.5V supply or dual ±1.25V to ±2.75V supplies. For single-supply operation, bypass the power supply V_{DD} with a 0.1μ F ceramic capacitor which should be placed close to the V_{DD} pin. For dual-supply operation, both the V_{DD} and the V_{SS} supplies should be bypassed to ground with separate 0. 1μF ceramic capacitors. 2. 2μF tantalum capacitor can be added for better performance.

Good PC board layout techniques optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize trace lengths and widths by placing external components as close to the device as possible. Use surface-mount components whenever possible.

For the operational amplifier, soldering the part to the board directly is strongly recommended. Try to keep the high frequency big current loop area small to minimize the EMI (electromagnetic interfacing).

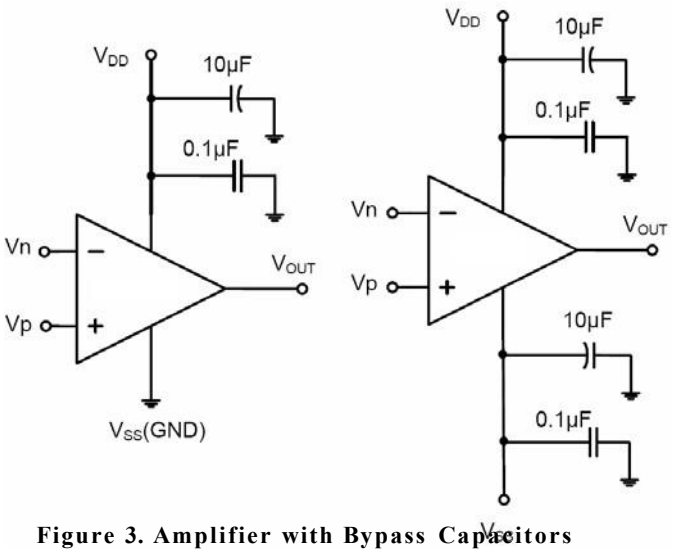


Figure 3. Amplifier with Bypass Capacitors

Grounding

A ground plane layer is important for D8632F circuit design. The length of the current path speed currents in an inductive ground return will create an unwanted voltage noise. Broad ground plane areas will reduce the parasitic inductance.

Input-to-Output Coupling

To minimize capacitive coupling, the input and output signal traces should not be parallel. This helps reduce unwanted positive feedback.

Differential Amplifier

The circuit shown in Figure 4 performs the difference function. If the resistors ratios are equal ($R_4/R_3 = R_2/R_1$), then $V_{OUT} = (Vp - Vn) \times R_2/R_1 + V_{REF}$.

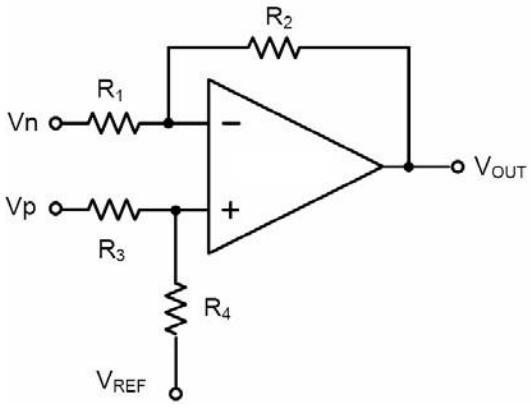


Figure 4. Differential Amplifier

Instrumentation Amplifier

The circuit in Figure 5 performs the same function as that in Figure 4 but with the high input impedance.

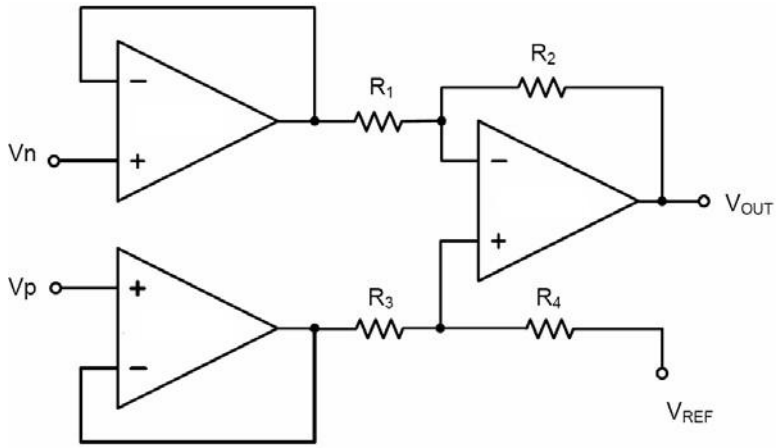


Figure 5. Instrumentation Amplifier Low Pass Active Filter

Low Pass Active Filter

The low pass filter shown in Figure 6 has a DC gain of($-R_2/R_1$) and the –3dB corner frequency is $1/2\ \pi\ R_2 C$. Make sure the filter is within the bandwidth of the amplifier. The Large values of feedback resistors can couple with parasitic capacitance and cause undesired effects such as ringing or oscillation in high- speed amplifiers. Keep resistors value as low as possible and consistent with output loading consideration.

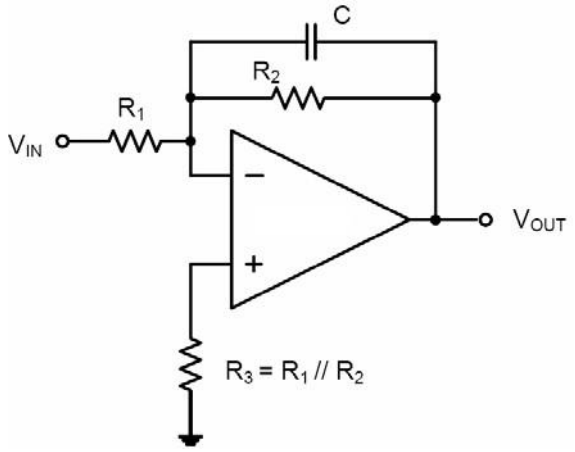
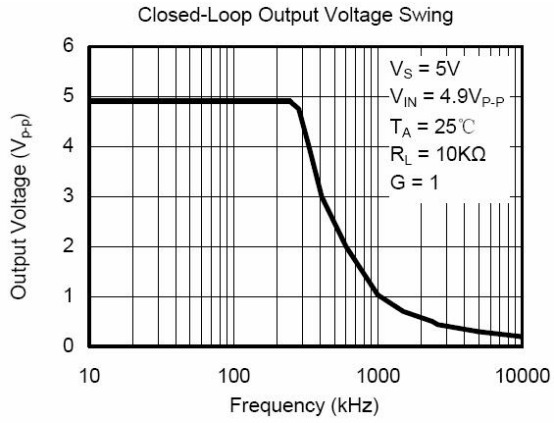
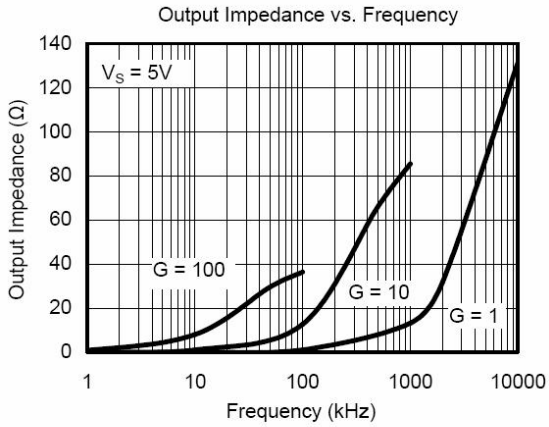


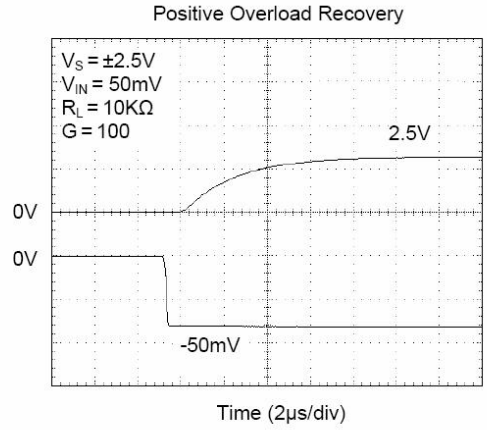
Figure 6. Low Pass Active Filter

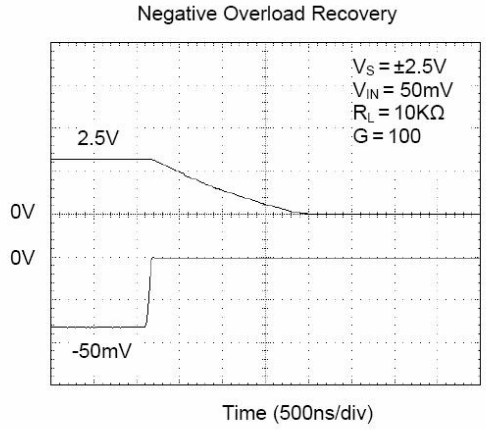
Typical Curve

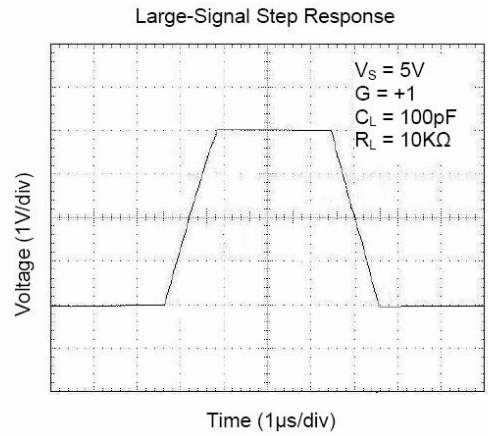
(At T_A =25 °C, V_{CM} = V_S /2,R_L =600 Ω,unless otherwise noted)

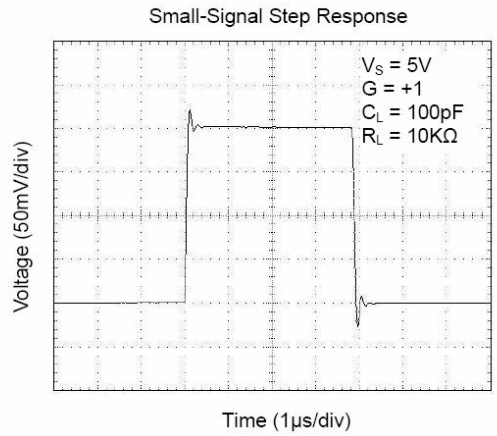




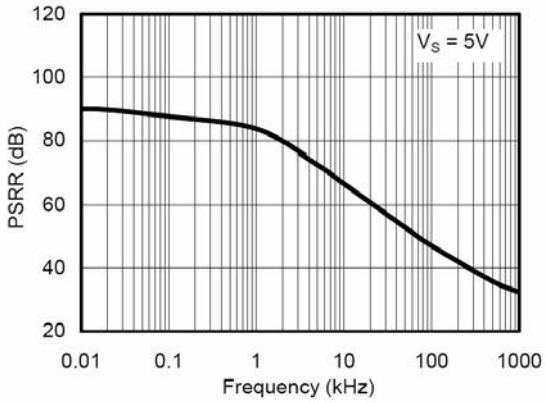




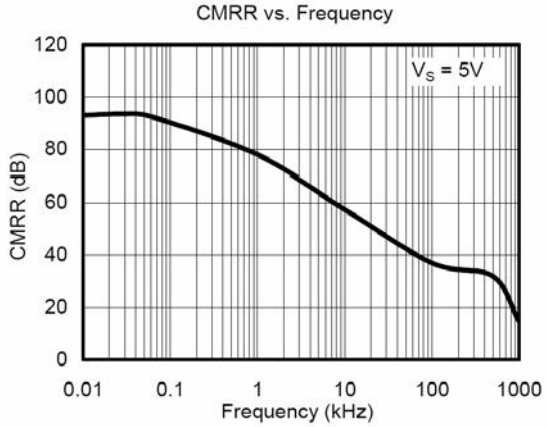




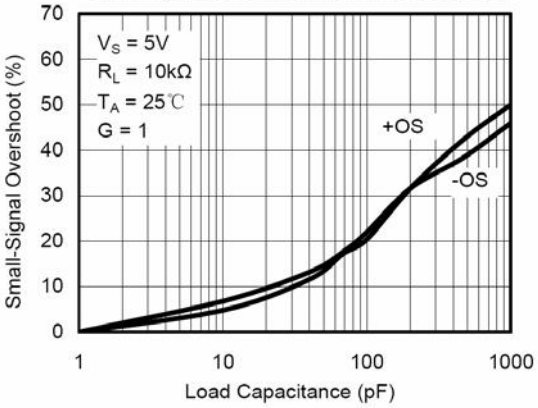
PSRR vs. Frequency



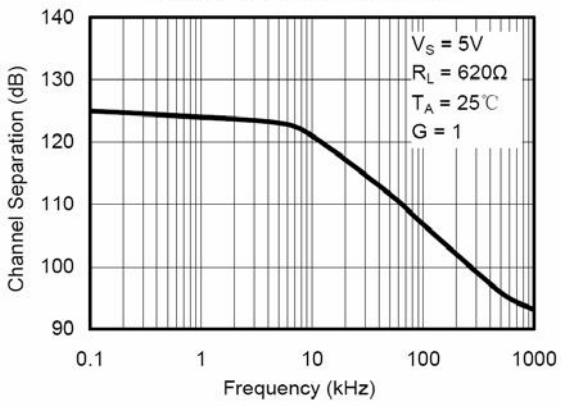
CMRR vs. Frequency



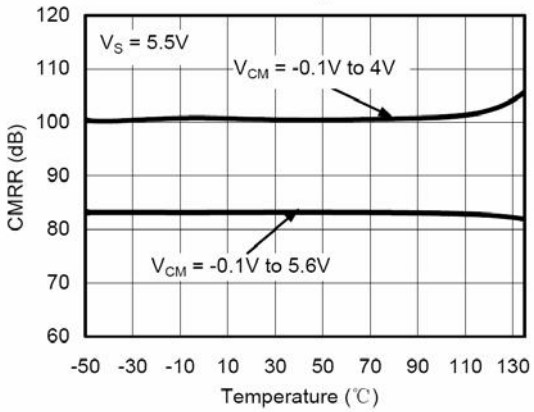
Small-Signal Overshoot vs. Load Capacitance



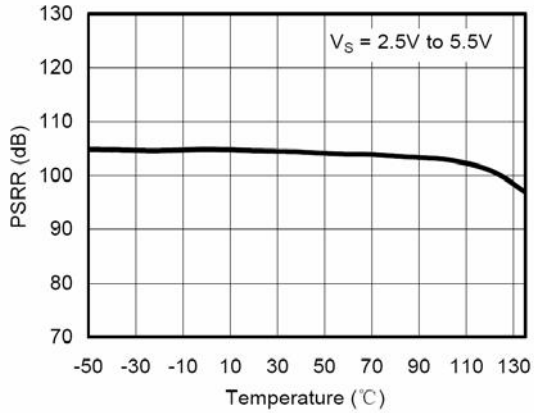
Channel Separation vs. Frequency



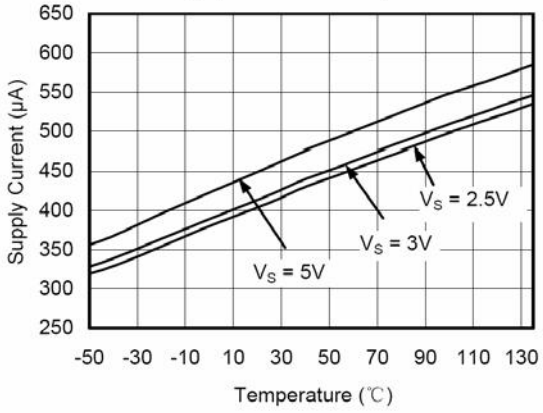
CMRR vs. Temperature



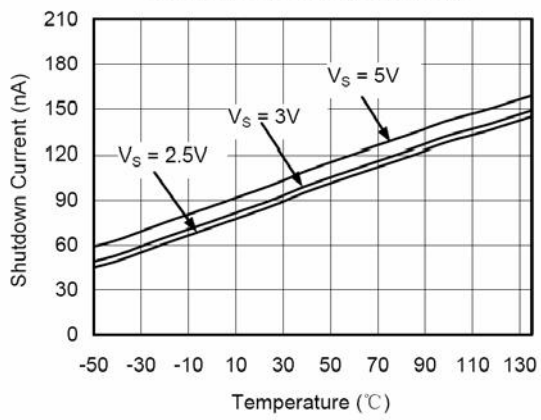
PSRR vs. Temperature



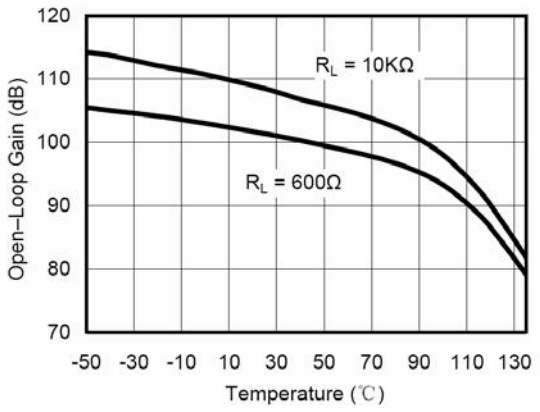
Supply Current vs. Temperature



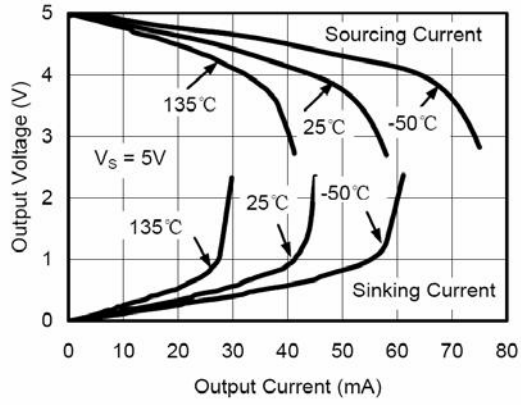
Shutdown Current vs. Temperature



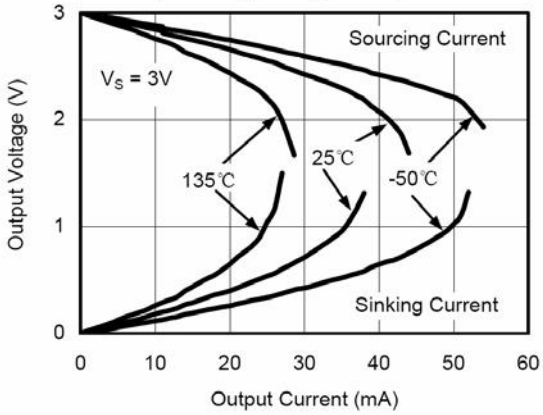
Open-Loop Gain vs. Temperature



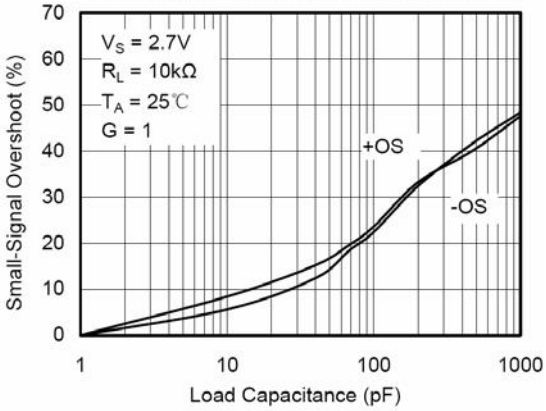
Output Voltage Swing vs. Output Current



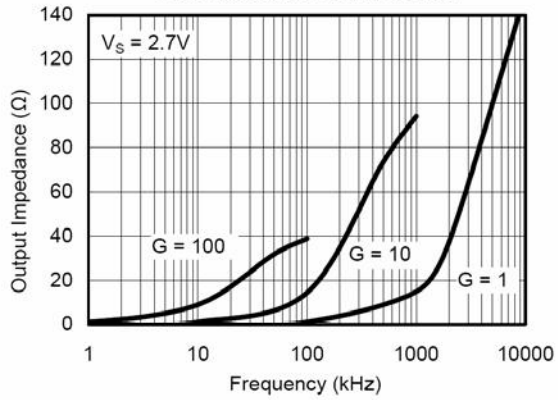
Output Voltage Swing vs. Output Current



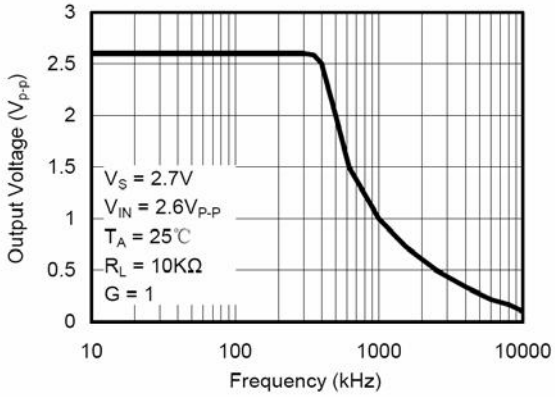
Small-Signal Overshoot vs. Load Capacitance



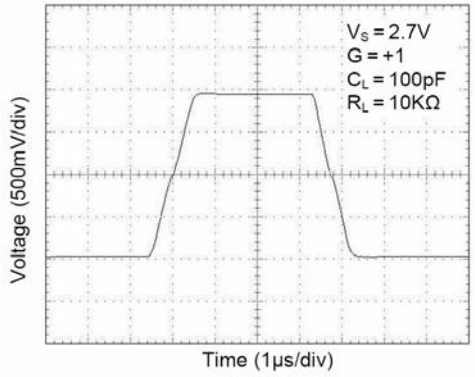
Output Impedance vs. Frequency



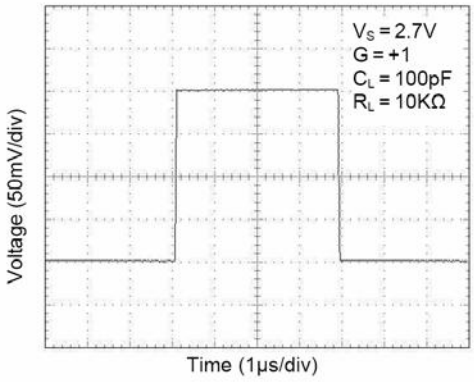
Closed-Loop Output Voltage Swing



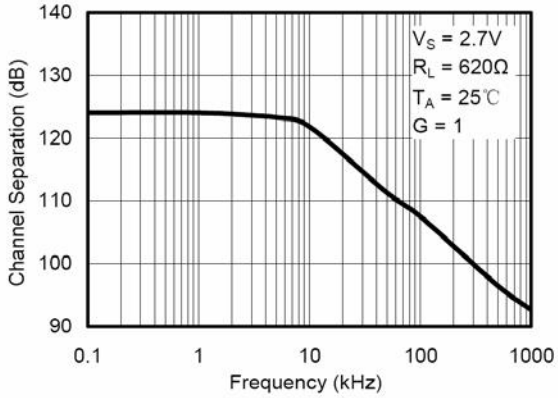
Large-Signal Step Response



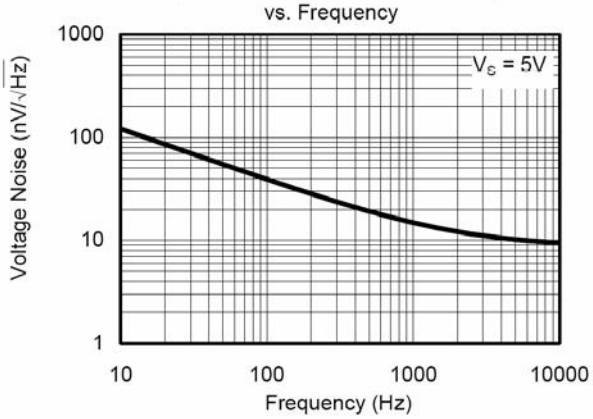
Small-Signal Step Response



Channel Separation vs. Frequency

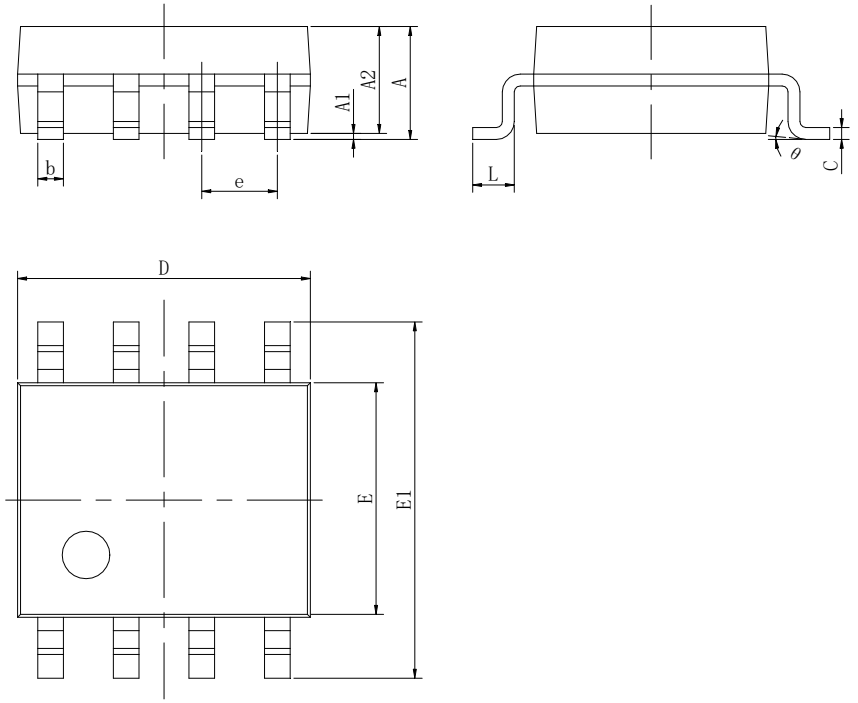


Input Voltage Noise Spectral Density vs. Frequency



Outline Dimensions

SOP8 Unit:mm



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.800	0.053	0.071
A1	0.000	0.250	0.000	0.010
A2	1.250	1.550	0.053	0.061
b	0.300	0.510	0.011	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.201
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Statements

- Silicore Technology reserves the right to make changes without further notice to any products or specifications herein. Before customers place an order, customers need to confirm whether datasheet obtained is the latest version, and to verify the integrity of the relevant information.

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