18V, 5A, High Efficiency Synchronous Step-Down Converter in DFN2x2-6

DESCRIPTION

ETA1656 is a wide input range, high efficiency and high frequency DC to DC step-down switching regulator, capable of delivering up to 5A of output current.

It adopts an Adaptive COT control scheme that enables very fast transient response and provides a very smooth transition when the output varies from light load to heavy load. During light load, ETA1656 goes into a PFM mode that saves switching loss achieving high efficiency. The adaptive COT control also maintains a constant switching frequency across line and load. An OVP function protects the IC itself and its downstream system against input voltage surges.

ETA1656 is available in a DFN2x2-6 package.

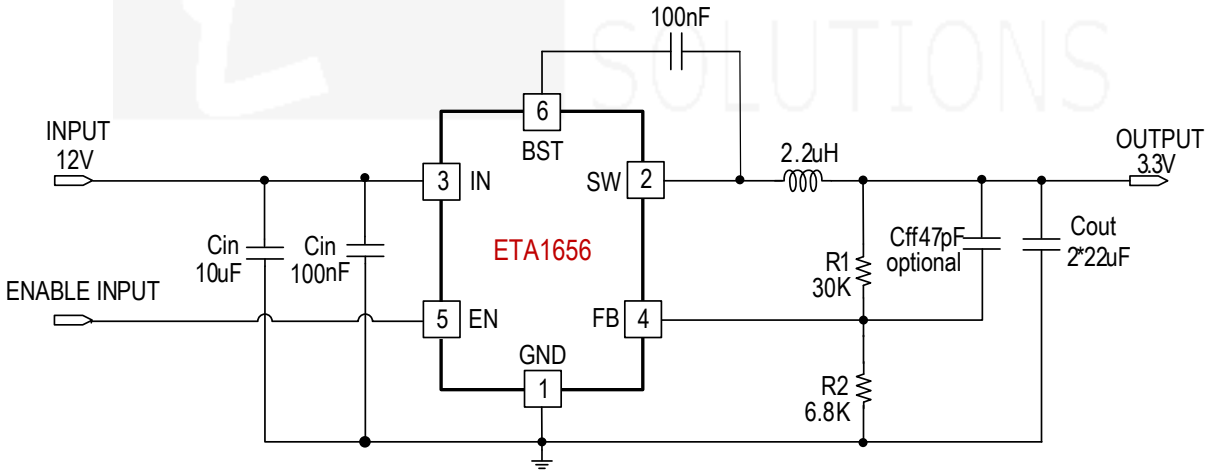
FEATURES

- Wide Input Range: 4.5V-18V
- Adaptive COT Control
- Ultra-Fast Load Transient Response
- High Efficiency PFM Mode at Light Load
- Low Rdson Internal Power FETs
- Capable of Delivering up to 5A
- Thermal Shutdown and UVLO
- Available in DFN2x2-6

APPLICATIONS

- 5G CPE
- Set Top Box
- LCD TV

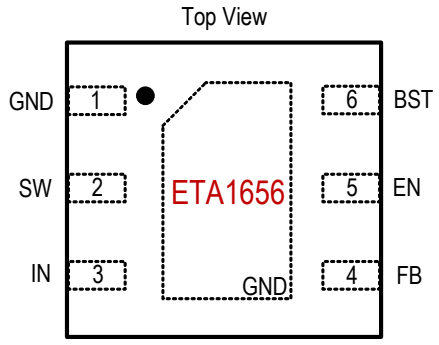
TYPICAL APPLICATION



ORDERING INFORMATION

PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA1656D2G	DFN2x2-6	TXYW	3000

PIN CONFIGURATION



DFN2x2-6

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

IN, SW, EN Voltage ……..–0.3V to 19V
BST Voltage.....–0.3V to SW+6V
FB Voltage .....–0.3V to 6V
Operating Temperature Range …….. –40°C to 85°C
Storage Temperature Range ..... –55°C to 150°C

Thermal Resistance	θ_{JA}	θ_{JC}
DFN2x2-6(1)…….....57.2…..…20.4…….	°C /W	

Lead Temperature (Soldering,10 sec)…..…..260°C

Note:

(1) Measured on 1OZ two-layer ETA evaluation board, T_A=25°C; the top of DFN2x2-6 package is the position where θ_{JC} measured.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{OUT} = 3.3V, unless otherwise specified. Typical values are at T_A = 25°C.)

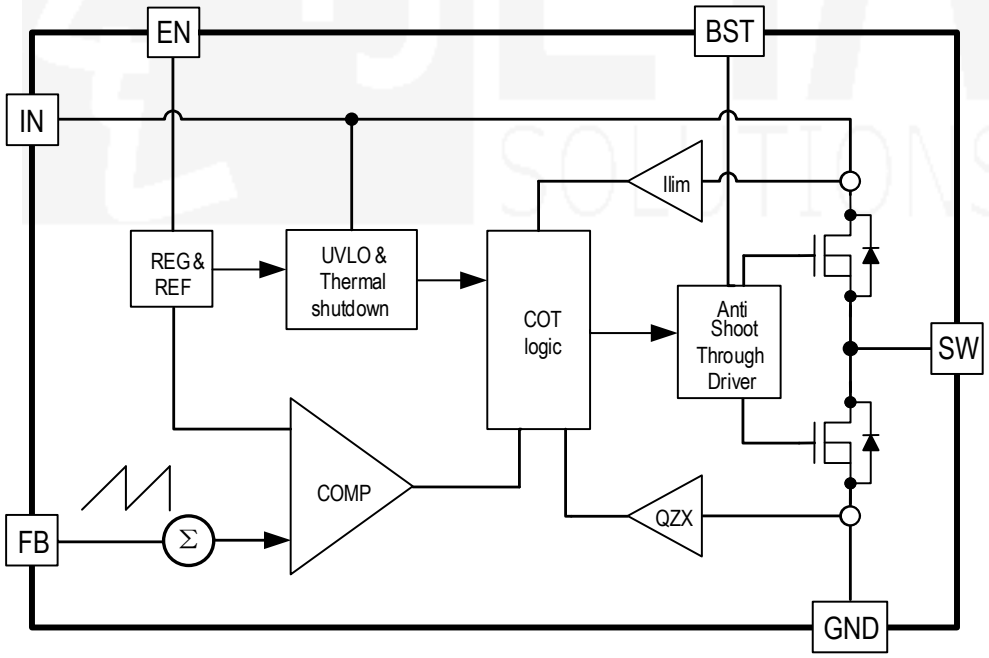
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range		4.5		18	V
Input Under Voltage Lock Output	V_{IN} Rising		4.05		V
UVLO Hysteresis	V_{IN} Falling		300		mV
IN Over Voltage Protection Threshold	V_{IN} Rising		19		V
OVP Hysteresis	V_{IN} Falling		0.9		V
Output Voltage Range		0.6		5	V
Quiescent Current	EN = 2V		230		μA
Shutdown Current	EN = 0V		7	17	μA
FB Pin Regulation Voltage			0.6		V
FB Input Current			0	1	uA
Switching Frequency	CCM mode		600		KHz
Maximum Duty Cycle			97		%
Short Circuit Hiccup Time	On Time		2		ms
	Off Time		6		ms
FB out-of Hiccup Threshold	V_{OUT} rising		75		%
FB under voltage hysteresis	V_{OUT} falling		50		mV
High Side Switch On Resistance	I_{SW}=1A		75		mΩ
Low Side Switch On Resistance	I_{SW}=1A		31		mΩ
SW Leakage Current	V_{IN}=V_{SW}=12V			10	uA
Peak inductor protection current	High Side ON		8.8		A
Lowside current limit protection			5		A
Reverse Current Protection			200		mA
EN Rising Threshold			1.15		V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
EN Threshold Hysteresis			100		mV
EN Input Current			2	6	uA
Thermal Shutdown			155		°C
Thermal Hysteresis			40		°C

PIN DESCRIPTION

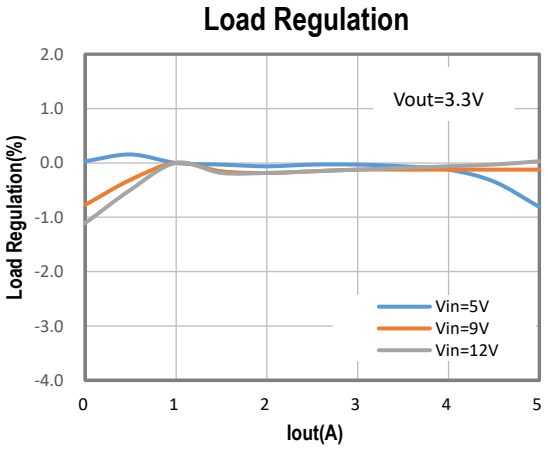
PIN #	PIN NAME	DESCRIPTION
1	GND	Ground
2	SW	Inductor Connection. Connect an inductor Between SW and the regulator output.
3	IN	Supply Voltage. Bypass with a 100nF HF filter plus a 10µF ceramic capacitor to GND.
4	FB	Feedback Input. Connect an external resistor divider from the output to FB and GND to set VOUT.
5	EN	Enable pin for the IC. Drive this pin high to enable the part, low or floating to disable.
6	BST	Bootstrap pin. Connect a 100nF capacitor from this pin to SW.

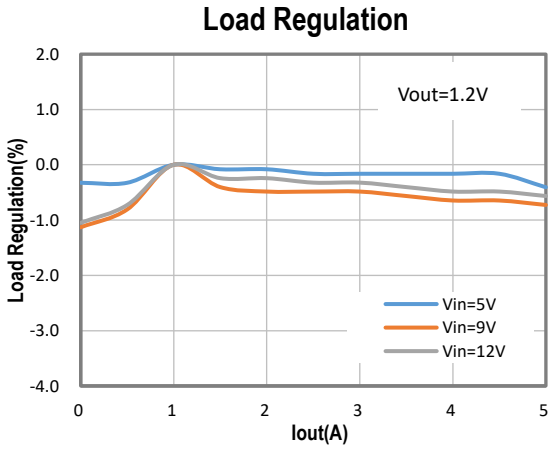
FUNCTIONAL BLOCK DIAGRAM

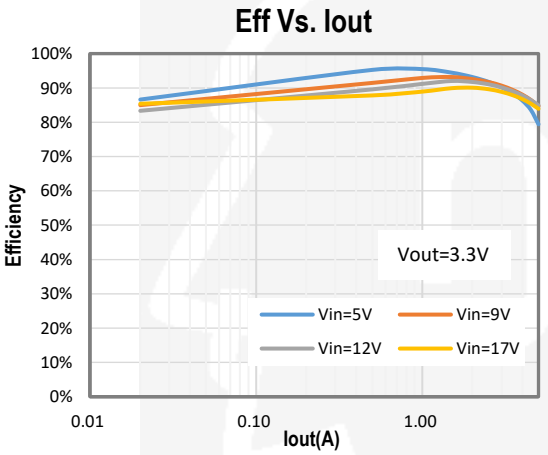


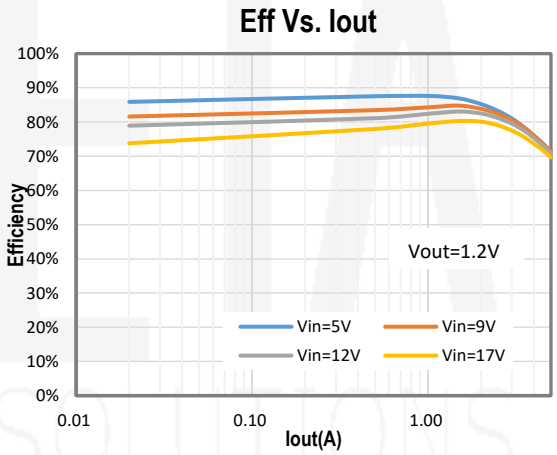
TYPICAL CHARACTERISTICS

Typical values are at Ta=25℃ unless otherwise specified

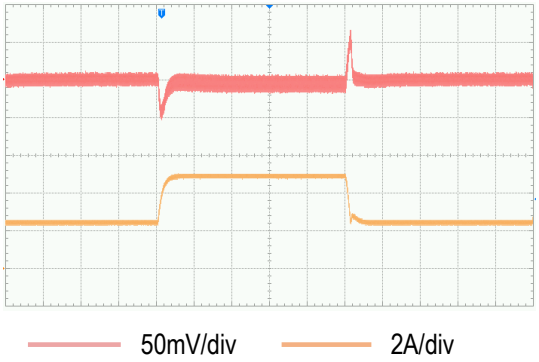




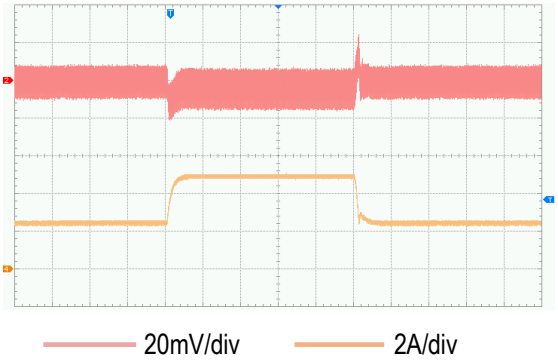




Load Step, Vout=3.3V; Iout from 2.5A to 5A



Load Step, Vout=1.2V; Iout from 2.5A to 5A



FUNCTION DESCRIPTION

The ETA1656 is a synchronous buck regulator ICs that integrates the adaptive COT control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss.

ETA1656 is a wide input range, high-efficiency and high frequency DC-to-DC step-down switching regulator, capable of delivering up to 5A of output current. It adopts an Adaptive COT control scheme that enables very fast transient response and provides a very smooth transition when the output varies from light load to heavy load. It compares the sum of the FB voltage and a ripple voltage that mimics the voltage due to the output ESR and capacitance. The constant-on-time timer varies with line to achieve relative constant switching frequency across line.

Light Load Operation

Traditionally, a fixed constant frequency PWM DC-DC regulator always switches even when the output load is small. When energy is shuffling back and forth through the power MOSFET, power is lost due to the finite Rdson of the MOSFET and parasitic capacitances. At light load, this loss is prominent and efficiency is therefore very low. ETA1656 goes into a power save mode during light load, thereby extending the range of high efficiency operation.

Enable

EN is a digital control pin that turns the ETA1656 on and off. Drive EN High to turn on the regulator, drive it Low to turn it off. An internal 1MΩ resistor from EN pin to GND allows EN to float to shut down the chip. Connecting the EN pin through a pull up resistor or shorted EN to IN will automatically turn on the chip whenever plug in IN.

Over Current Protection and Hiccup

ETA1656 has a cycle-by-cycle over current limit for both inductor current peak value and inductor current valley value. Meanwhile both inductor currents during LS_FET ON or HS_FET ON are monitored. During LS_FET on, sensed inductor current is monitored by a valley current limit comparator. HS_FET always wait until valley current limit disappear to be on again. Once, HS_FET is ON, it will be immediately OFF whenever max on time or peak current limit is reached.

When the output voltage drop until FB falls below UV threshold (70% Vnormal), the ETA1656 will enter hiccup mode. It will turn off the chip immediately for 6mS. After that, it will try to re-starts as normal for 2ms. After 2ms, if FB is still below UV threshold, then the chip enters hiccup mode again. If FB is higher than UV threshold, it will enter the normal mode.

Over-Temperature Protection

Thermal protection disables the output when the junction temperature rises to approximately 150°C, allowing the device to cool down. When the junction temperature cools down approximately 110°C, the output circuitry

is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off.

This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

OUTPUT VOLTAGE CONFIGURATION

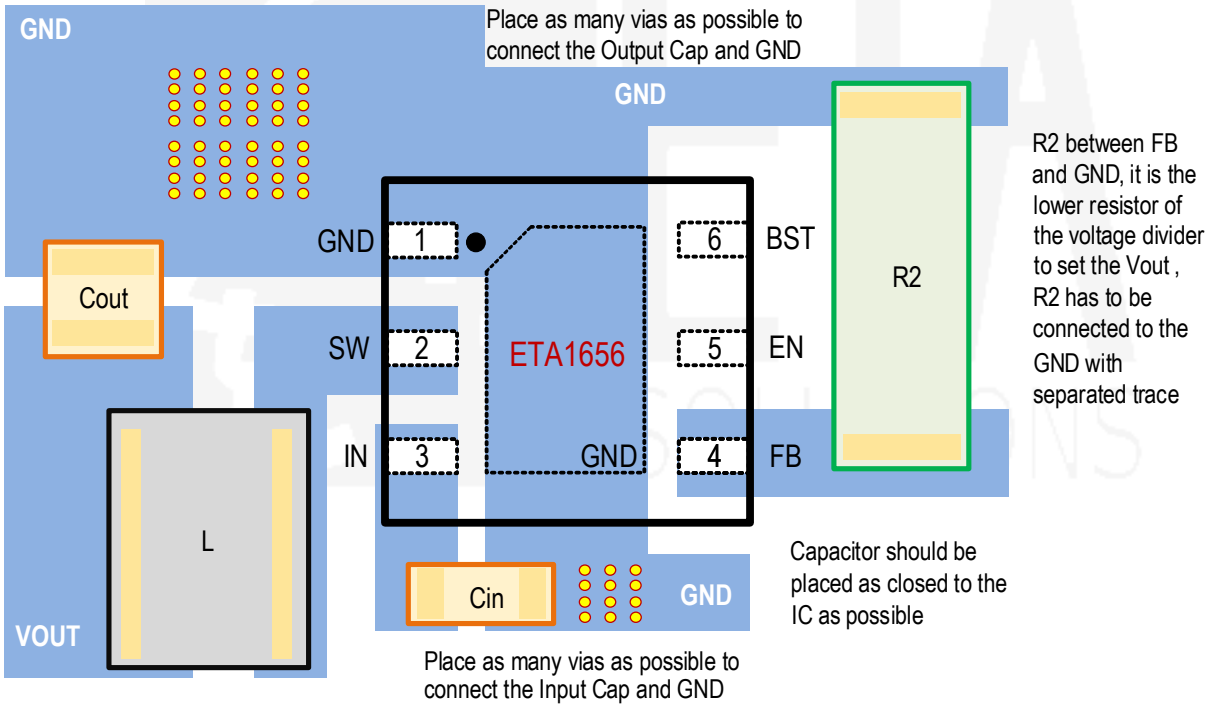
In external Output Voltage Setting Version selected, the ETA1656 regulator is programmed using an external resistor divider. The output voltage is calculated using below equation.

$$V_{OUT}=V_{REF}\times\left(1+\frac{R_1}{R_2}\right)$$

Resistors R2 has to be between 1KOhm to 20KOhm and thus R1 is calculated by following equation.

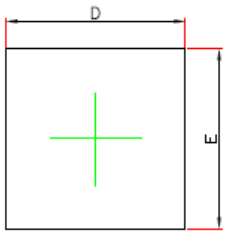
$$R_1=\left(\frac{V_{OUT}}{V_{REF}}-1\right)\times R_2$$

PCB LAYOUT GUIDELINE

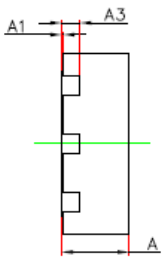


PACKAGE OUTLINE

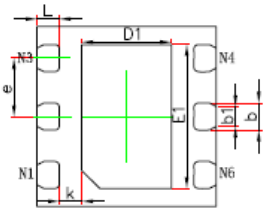
Package: DFN2x2-6



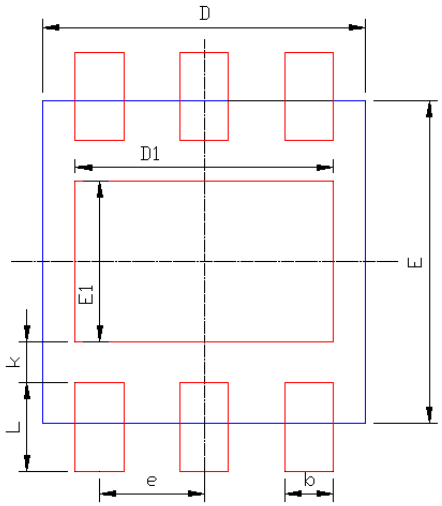
TOP VIEW



SIDE VIEW



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	1.900	2.100	0.075	0.083
E	1.900	2.100	0.075	0.083
D1	0.900	1.100	0.035	0.043
E1	1.500	1.700	0.059	0.067
k	0.250 REF.		0.010REF.	
b	0.250	0.350	0.010	0.014
b1	0.220 REF.		0.009 REF.	
e	0.650BSC.		0.026BSC.	
L	0.174	0.326	0.007	0.013

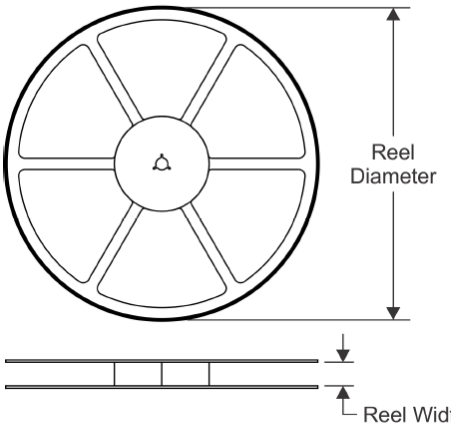


RECOMMENDED LAND PATTERN

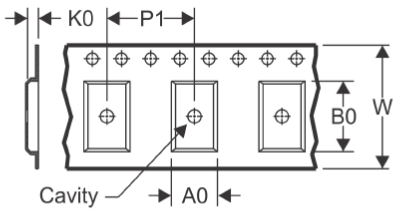
Dimensions	Value (in mm)
D	2
E	2
D1	1.6
E1	1
e	0.65
b	0.3
L	0.55
k	0.25 (at least ≥ 0.2)

TAPE AND REEL INFORMATION

REEL DIMENSIONS

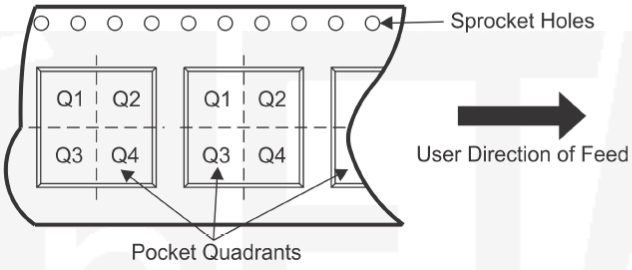


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA1656D2G	DFN2*2-6	6	3000	180	9.5	2.3	2.3	1.1	4	8	Q1