MP86920

Intelli-Phase™ Solution with Integrated HS-/LS-FETs and Driver in LGA (4mmx5mm) Package

DESCRIPTION

The MP86920 is a monolithic half-bridge driver with built-in internal power MOSFETs and gate drivers. It achieves 20A of continuous output current across a wide input supply range.

The integrated driver and MOSFETS result in high efficiency due to an optimal dead time and reduced parasitic inductance.

This device works with tri-state output controllers, and can operate between 100kHz and 2MHz. It also comes with a general-purpose current sense and temperature sense.

The MP86920 is well-suited for server and telecom applications where efficiency and small size are a premium. It is available in an LGA-27 (4mmx5mm) package.

FEATURES

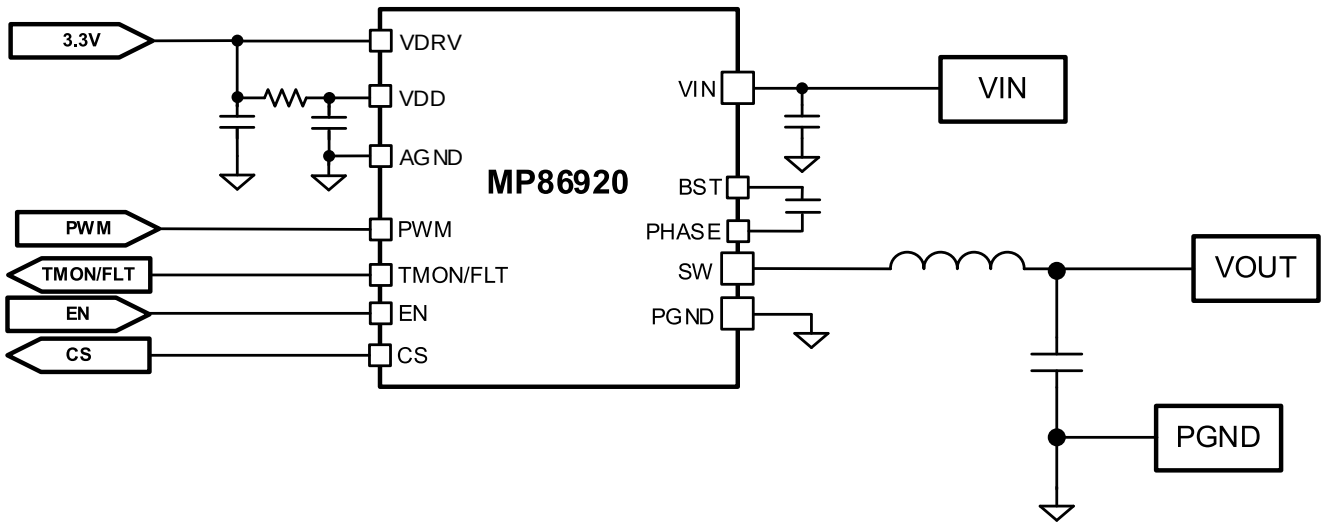
- Wide 4.5V to 16V Operating Input Range
- 20A Output Current
- Accepts Tri-State PWM Signals
- Built-In Switch for Bootstrap
- Current Sense
- Temperature Sense
- Current Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Used for Multi-Phase Operation
- Available in an LGA-27 (4mmx5mm) Package

APPLICATIONS

- Server and Telecom Voltage Regulators
- Graphics Card Core Regulators
- Power Modules

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP86920GLV	LGA-27 (4mmx5mm)	*See Below*	3

* For Tape & Reel, add suffix –Z (e.g. MP86920GLV–Z).

TOP MARKING

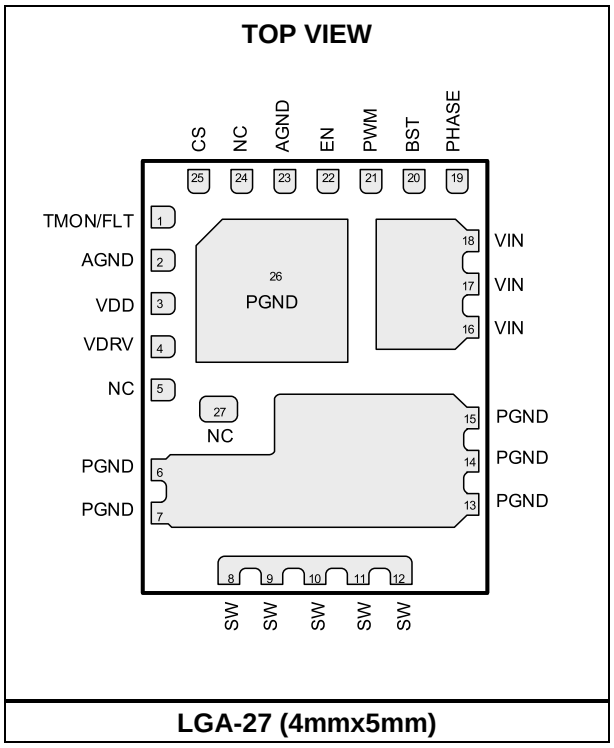
MPSYWW

M86920

LLLLLL

MPS: MPS prefix
Y: Year code
WW: Week code
M86920: Part number
LLLLLL: Lot number

PACKAGE REFERENCE



LGA-27 (4mmx5mm)

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PIN FUNCTIONS

Pin #	Name	Description
1	TMON/FLT	**Single-pin temperature sense and fault reporting.**
2, 23	AGND	**Analog ground.** Connect AGND to the PGND plane at the VDD decoupling capacitor.
3	VDD	**3.3V supply for internal circuitry.** Decouple VDD with 1µF (or higher) ceramic capacitor connected to AGND.
4	VDRV	**Driver voltage.** Connect VDRV to a 3.3V supply. Decouple this pin with a 1µF to 4.7µF ceramic capacitor.
5, 24, 27	NC	**No connection.**
6, 7, 13, 14, 15, 26	PGND	**Power ground.** Place multiple vias on the inner solid ground layers to minimize parasitic impedance and thermal resistance.
8, 9, 10, 11, 12	SW	**Switch output.**
16, 17, 18	VIN	**Supply voltage.** Place an input capacitor (C_{IN}) on VIN. Place the capacitor close to the device to support the switching current and reduce voltage spikes at the input.
19	PHASE	**Switching node for bootstrap capacitor connection.** The PHASE pin is internally connected to SW.
20	BST	**Bootstrap.** BST requires a 0.1µF to 1µF capacitor to drive the power switch's gate above the supply voltage. Connect the capacitor between the PHASE and BST pins to form a floating supply across the power switch driver.
21	PWM	**Pulse-width modulation input.** Float the PWM pin or drive it to a middle-state voltage to enable diode emulation mode.
22	EN	**Enable.** Pull EN low to disable the device and place SW in a high-impedance state.
25	CS	**Current-sense output.** Connect an external resistor to the CS pin to adjust the voltage proportional to the inductor current.

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ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (VIN) 18V
$V_{SW (DC)}$ .....-0.3V to VIN + 0.3V
$V_{SW (25ns)}$.....-5V to +25V
VIN - $V_{PHASE (DC)}$ .....-0.3V to +25V
VIN - $V_{PHASE (10ns)}$ .....-5V to +32V
V_{BST} - $V_{PHASE (25ns)}$..... 5V
V_{BST} ..... V_{PHASE} + 4V
VDD, VDRV .....-0.3V to +4V
All other pins .....-0.3V to VDD + 0.3V
Instantaneous current 45A
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 1
Charged device model (CDM).....Class C2B

Recommended Operating Conditions (2)

Supply voltage (VIN).....4.5V to 16V
Driver voltage (VDRV) .....3.0V to 3.6V
Logic voltage (VDD).....3.0V to 3.6V
Operating junction temp (T_J).... -40°C to +125°C

Thermal Resistance (3) θ_{JB} θ_{JC_TOP}

LGA-27 (4mmx5mm) ..... 4.3..... 18.7... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB} is the thermal resistance from the junction to board around the PGND soldering point.
   θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.

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ELECTRICAL CHARACTERISTICS

VIN = 12V, VDRV = VDD = EN = 3.3V, T_A = 25°C for typical values, T_J = -40°C to +125°C for maximum and minimum values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
VIN under-voltage lockout rising threshold				4.1	4.5	V
VIN under-voltage lockout threshold hysteresis				380		mV
VIN quiescent current in standby mode	$I_{IN\ STBY}$	PWM = Hi-Z, EN = low, VIN = 4.5V to 16V			5	µA
I_{VDRV} quiescent current in active mode	$I_{DRV_QUIESCENT}$	PWM = low, no switching, EN = high			3.5	mA
I_{VDRV} quiescent current in standby mode	I_{DRV_STBY}	EN = low			30	µA
VDD voltage UVLO rising threshold			2.4	2.7	2.95	V
VDD voltage UVLO hysteresis				200		mV
High-side current limit (4)	I_{LIM_FLT}			50		A
High-side current limit shutdown counter (4)				4		times
Low-side current limit (4)				-15		A
Low-side off time with negative current limit (4)				40		ns
Dead time rising (4)				3		ns
Dead time falling (4)		Positive inductor current		8		ns
		Negative inductor current		40		ns
EN input high voltage			2.30			V
EN input low voltage					0.8	V
PWM high to SW rising delay (4)	t_{RISING}			20		ns
PWM low to SW falling delay (4)	$t_{FALLING}$			20		ns
PWM tri-state to SW Hi-Z delay (4)	t_{LT}			50		ns
	t_{TL}			50		ns
	t_{TH}			50		ns
	t_{HT}			50		ns
Minimum SW pulse width (4)				30		ns
CS sense gain accuracy		5A ≤ I_{SW} ≤ 20A	-2	0	+2	%
CS sense gain				10		µA/A
CS offset		I_{SW} = 0A	-7	0	7	µA
		SW = Hi-Z	-2	0	2	µA
CS common mode voltage range	V_{CS_COM}		0.8		2	V
TMON/FLT sense gain (4)				8		mV/°C
TMON/FLT sense offset (4)		T_J = 25°C		800		mV
TMON/FLT sense voltage range (4)		T_J = 150°C		1.8		V
		T_J = 100°C		1.4		V
		T_J = 25°C		0.8		V

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ELECTRICAL CHARACTERISTICS *(continued)*

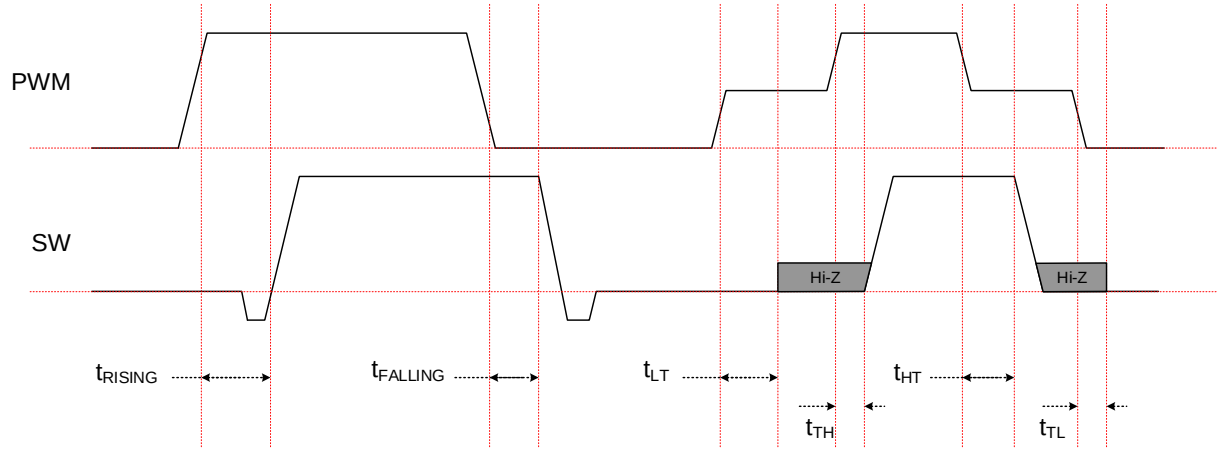
VIN = 12V, VDRV = VDD = EN = 3.3V, T_A = 25°C for typical values, T_J = -40°C to +125°C for maximum and minimum values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Over-temperature shutdown (4)				160		°C
TMON/FLT if a fault occurs (4)			3.0	3.3		V
PWM resistor		Pull-up, EN = high		6		kΩ
		Pull-down		5		kΩ
PWM logic high voltage			2.4			V
PWM tri-state region			1.1		1.9	V
PWM logic low voltage					0.7	V

Note:

4) Guaranteed by design. Not tested in production. The parameter is tested during parameters characterization.

PWM TIMING CHART

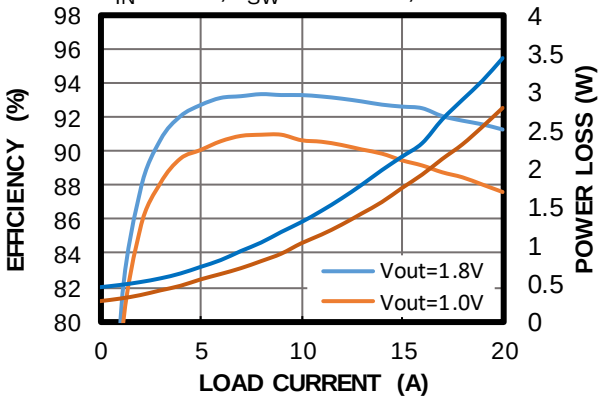


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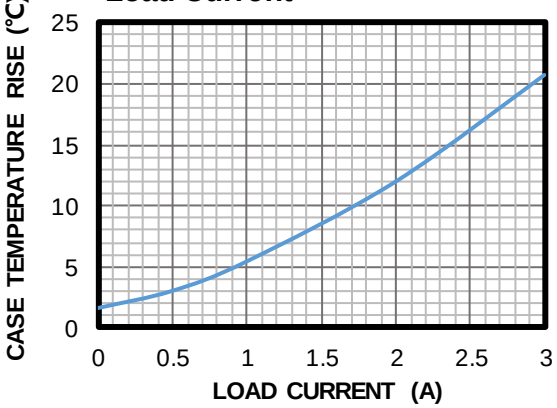
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs. Load Current

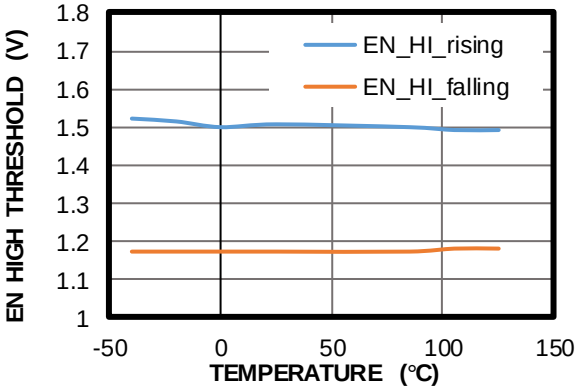
V_{IN} = 12V, f_{SW}= 800kHz, 150nH



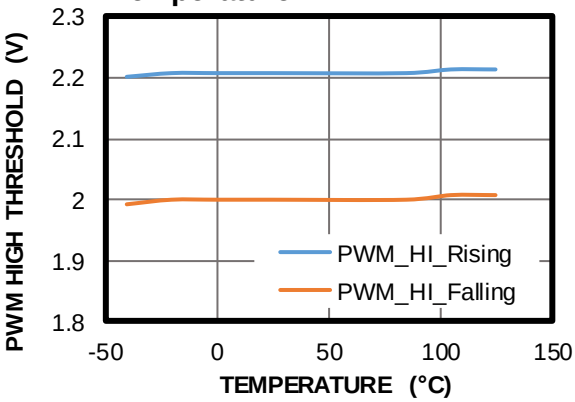
Case Temperature Rise vs. Load Current



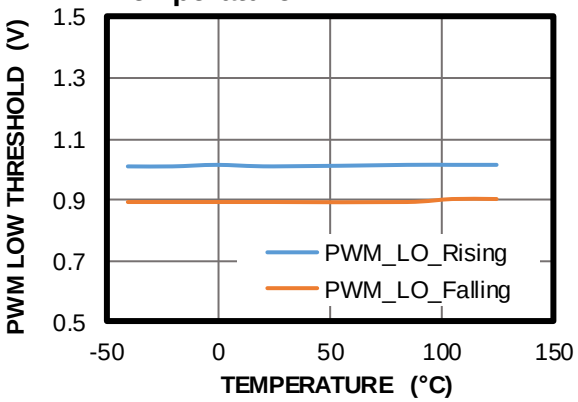
EN High Threshold vs. Temperature



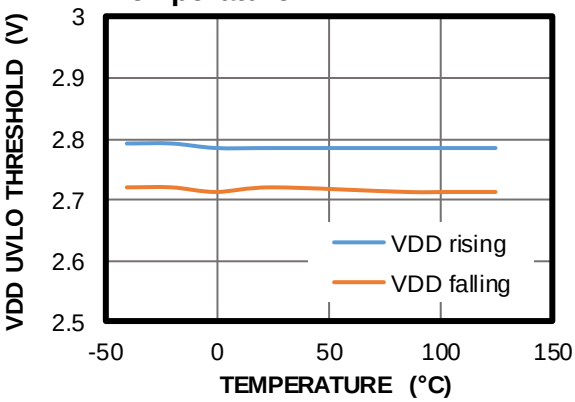
PWM High Threshold vs. Temperature



PWM Low Threshold vs. Temperature



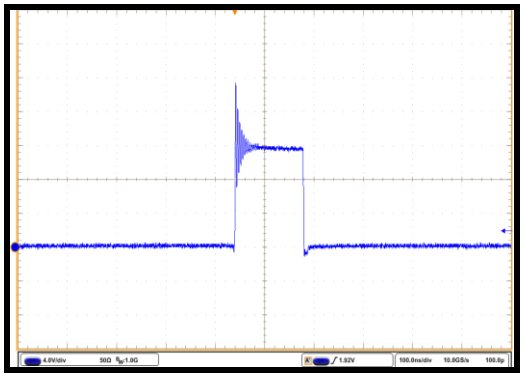
VDD UVLO Threshold vs. Temperature



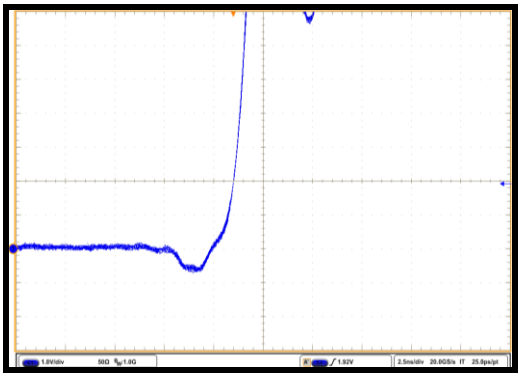
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

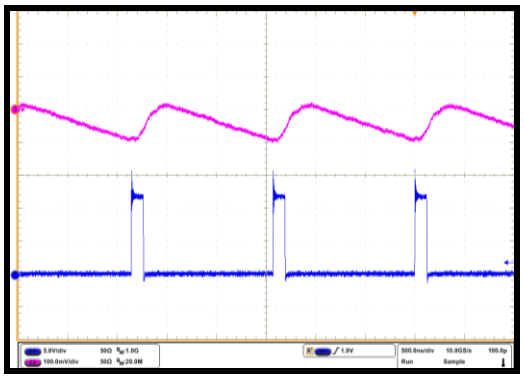
Switching
VIN = 12V, L = 150nH, load = 10A



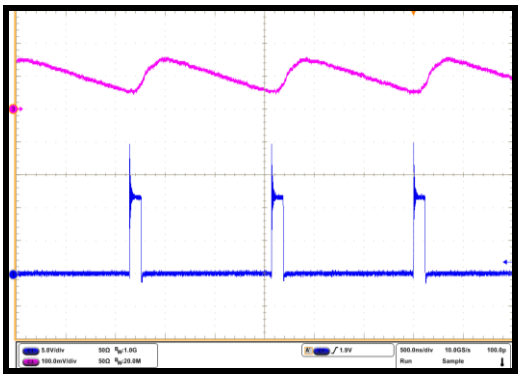
Dead Time with SW Ringing



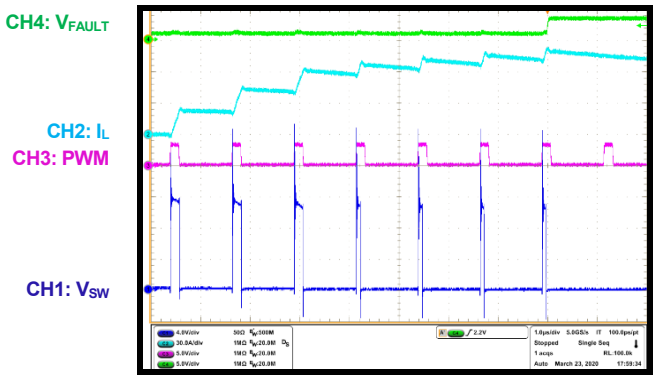
IOUT Output
Load = 0A



IOUT Output
Load = 10A



HS Current Limit



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FUNCTIONAL BLOCK DIAGRAM

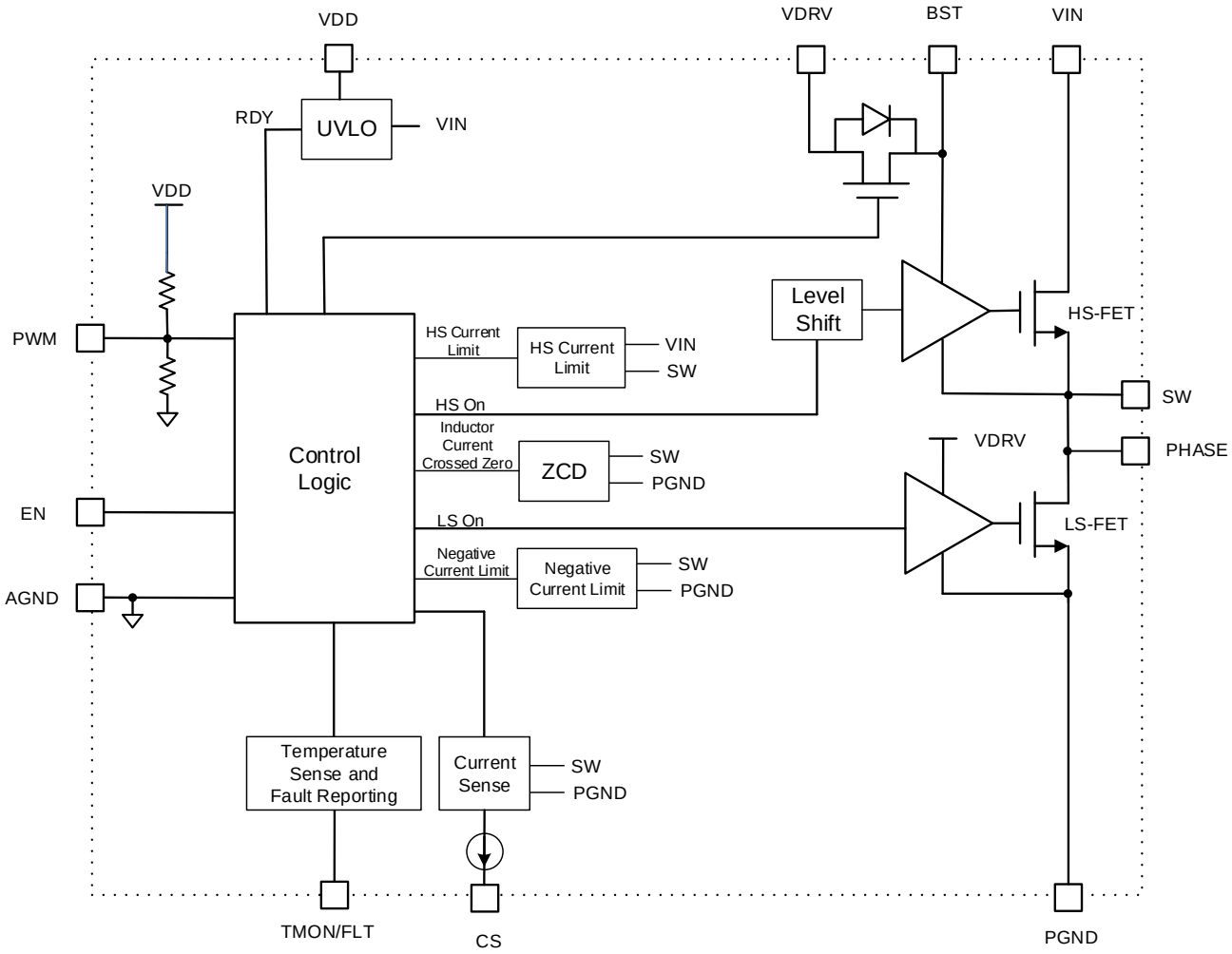


Figure 1: Functional Block Diagram

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OPERATION

The MP86920 is a 20A, monolithic half-bridge driver with MOSFETs. It is well-suited for multi-phase buck regulators. When the VIN, VDD signals are sufficiently high, operation begins.

PWM

The PWM input pin is capable of tri-state input. When the PWM input signal is within the tri-state threshold window for about 50ns (t_{HT} or t_{LT}), the high-side MOSFET (HS-FET) turns off immediately. The low-side MOSFET (LS-FET) enters diode emulation mode, and stays on until zero-current detection (ZCD).

The tri-state PWM input is enabled by forcing a middle-voltage PWM signal, or by floating the PWM input. The internal current source charges the signal to a middle voltage. See the PWM Timing Diagram on page 6 to define the propagation delay from PWM to the SW node.

Diode Emulation Mode

When PWM is in tri-state input in diode emulation mode, the LS-FET turns on when the inductor current is positive. The LS-FET turns off if the inductor current reaches 0A. Diode emulation mode can be enabled by floating the PWM pin or driving it to a middle state.

Positive and Negative Inductor Current Limit

If an over-current (OC) condition is detected on the HS-FET for four consecutive cycles, the HS-FET latches off, and TMON/FLT is pulled to 3.3V. The LS-FET turns on, and stays on until ZCD. To release the latch and restart the device, cycle the power on VIN or VDD, or toggle EN.

If the LS-FET detects a -15A current, the part turns off the LS-FET for 40ns to limit the negative current. The LS-FET's negative current limit does not trigger a fault report.

Over-Temperature Protection (OTP)

If the junction temperature reaches the over-temperature (OT) threshold, the HS-FET latches off, and TMON/FLT is pulled to 3.3V. The LS-FET turns on, and stays on until ZCD.

Temperature-Sense Output with Fault Indicator (TMON/FLT)

The TMON/FLT pin can sense the junction temperature or indicate if certain faults have occurred.

Junction Temperature Sense

When VDD exceeds its under-voltage lockout (UVLO) threshold and the part is in active mode, the TMON/FLT pin has an output voltage that is proportional to the junction temperature. The gain is 8mV/°C, and it has a 800mV offset at 25°C (e.g. the voltage is 0.8V when T_J = 25°C, and 1.4V when T_J = 100°C).

Fault Function

If a fault occurs, the TMON/FLT pin is pulled to VDD to report the fault, regardless of the temperature. TMON/FLT monitors three fault events, described below:

1. Over-current limit: The current limit fault condition must remain for four consecutive cycles to trigger this fault. If this fault occurs, the part latches off to turn off the HS-FET. The LS-FET turns on and stays on until the current reaches 0A.
2. Over-temperature fault when T_J > 160°C: If an over-temperature fault occurs, the part latches off, and the HS-FET turns off. The LS-FET turns on and stays on until the current reaches 0A.
3. SW-to-PGND short: If a short fault occurs, the part latches off to turn off the HS-FET.

The fault latch is not reset by entering standby mode. The fault latch is released by cycling the power on VIN or VDD.

Current Sense (CS)

The CS pin is a bidirectional current source that is proportional to the inductor current. The current-sense gain is 10μA/A. If required, a resistor can be used to configure the voltage gain proportional to the inductor current

The CS voltage must range between 0.8V and 2.0V to keep CS's output current linearly proportional to the inductor current. In general, there is a resistor (R_{CS}) connected from the CS pin to an external voltage that is capable of

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sinking small currents. This provides a sufficient voltage level to meet the required operating voltage range.

Figure 2 shows the typical circuit diagram for the CS pin connection to achieve a differential voltage source proportional to the inductor current.

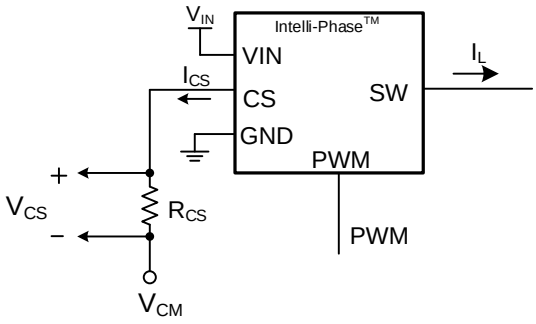


Figure 2: Typical Circuit Diagram for CS Pin Connection

Choose a value for R_{CS} such that V_{CS} stays within its operating range. This relationship can be calculated with Equation (1):

$$0.8V < I_{CS} \times R_{CS} + V_{CM} < 2.0V \quad (1)$$

Where V_{CM} is the reference voltage connected to R_{CS}, and I_{CS} is the current on the CS pin, estimated with Equation (2):

$$I_{CS} = I_L \times G_{CS} \quad (2)$$

The Intelli-Phase's™ current-sense output can be used by the controller to accurately monitor the output current. The cycle-by-cycle current information from the CS pin can be used for phase current balancing, over-current protection, and active voltage positioning (output voltage droop).

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APPLICATION INFORMATION

PCB Layout Guidelines

An efficient layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place the MLCC input capacitors as close to VIN and PGND as possible.
2. Place as many VIN and PGND vias underneath the package as possible. Place these vias between the VIN or PGND long pads.
3. Place a VIN copper plane on the second inner layer to form the PCB stack (positive/negative/positive) to reduce parasitic impedance from the MLCC input capacitor to the MP86950. Ensure that the copper plane on the inner layer covers the VIN vias and MLCC input capacitors.
4. Place more PGND vias close to the PGND pin/pad to minimize parasitic resistance, parasitic impedance, and thermal resistance.
5. Place the BST capacitor, BST resistor, and VDRV capacitor as close to the MP86950's pins as possible. For BST routing, use a trace width greater than 20mils. Avoid placing vias on the BST driving path.
6. Place the VDD decoupling capacitor close to the device.
7. Route the CS signal trace away from high voltages and current slew rate nodes (such as SW, PWM, the VIN vias, and the PGND vias).

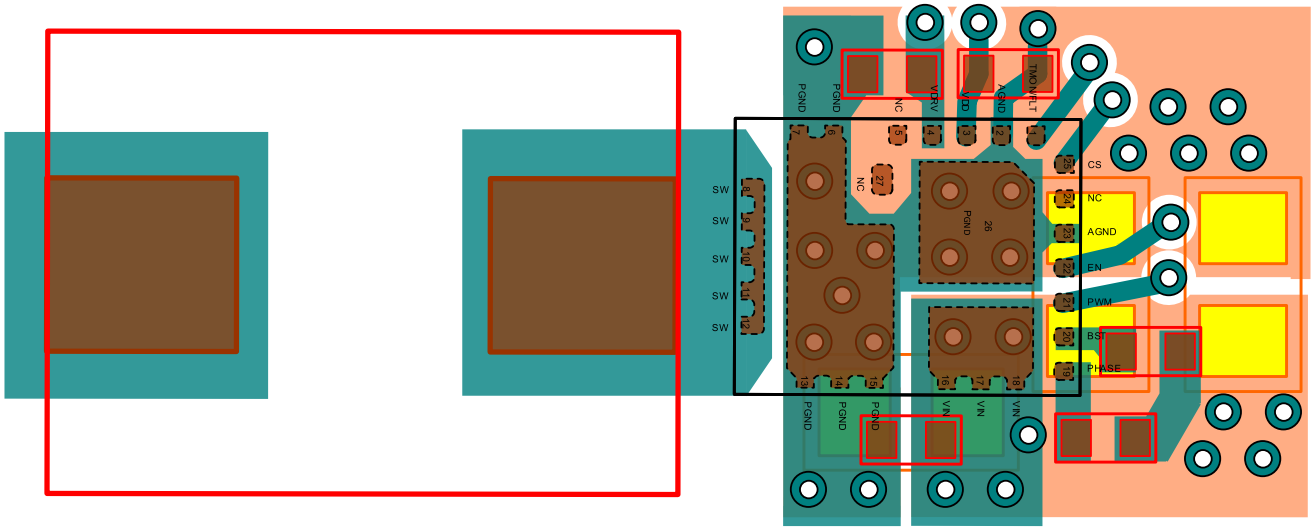


Figure 3: Recommended PCB Layout

Input Capacitor: 0402 Package (Top Side) and 0805 Package (Bottom Sides)

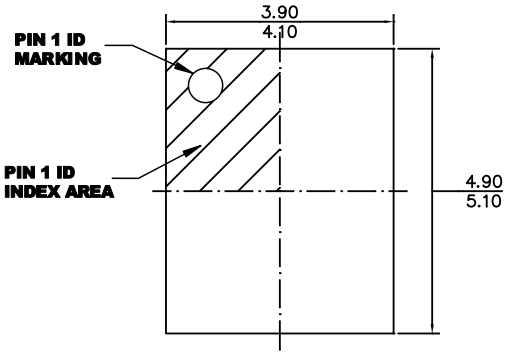
BST/VDRV/VDD Capacitor/Resistor: 0402 Package

Via Size: 10/20mils

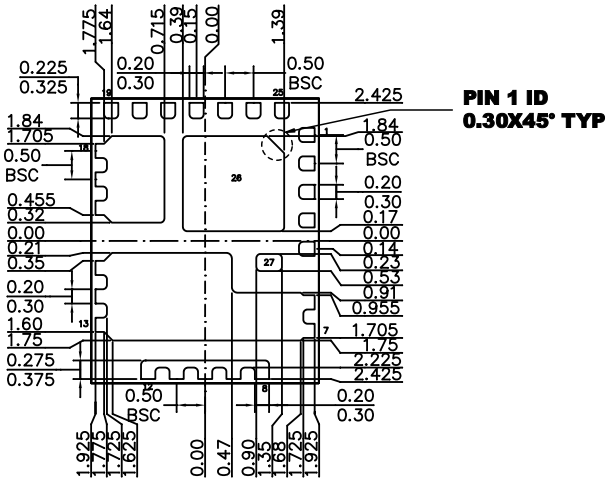
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PACKAGE INFORMATION

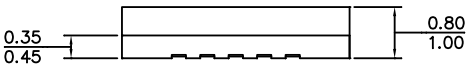
LGA-27 (4mmx5mm)



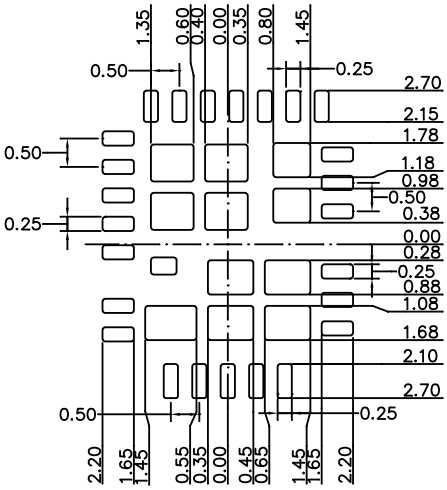
TOP VIEW



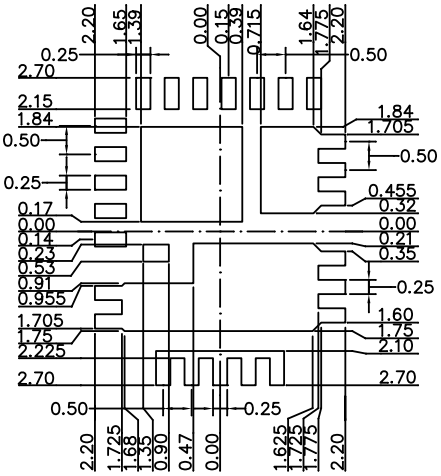
BOTTOM VIEW



SIDE VIEW



RECOMMENDED STENCIL DESIGN



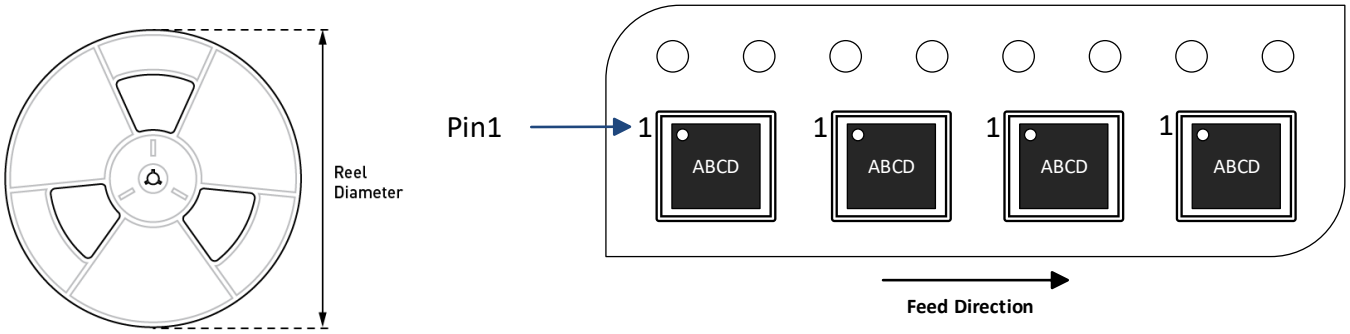
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP86920GLV–Z	LGA-27 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

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REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/22/2020	Initial Release	-

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