M62393P/FP

8-bit 8ch I²C BUS D/A Converter with Buffer Amplifiers

R03DS0046EJ0400
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Description

The M62393P/FP is an integrated circuit semiconductor of CMOS structure with 8 channels of built-in D/A converters with output buffer operational amplifiers. The input is 2-wires serial method is used for the transfer format of digital data to allow connection with a microcomputer with minimum wiring.

The output buffer operational amplifier employs AB class output circuit with sink and source drive capacity of 1.0 mA or more, and it operates in the whole voltage range from VrefU to ground. And because of connects maximum 8 pieces to 64 channels control.

Features

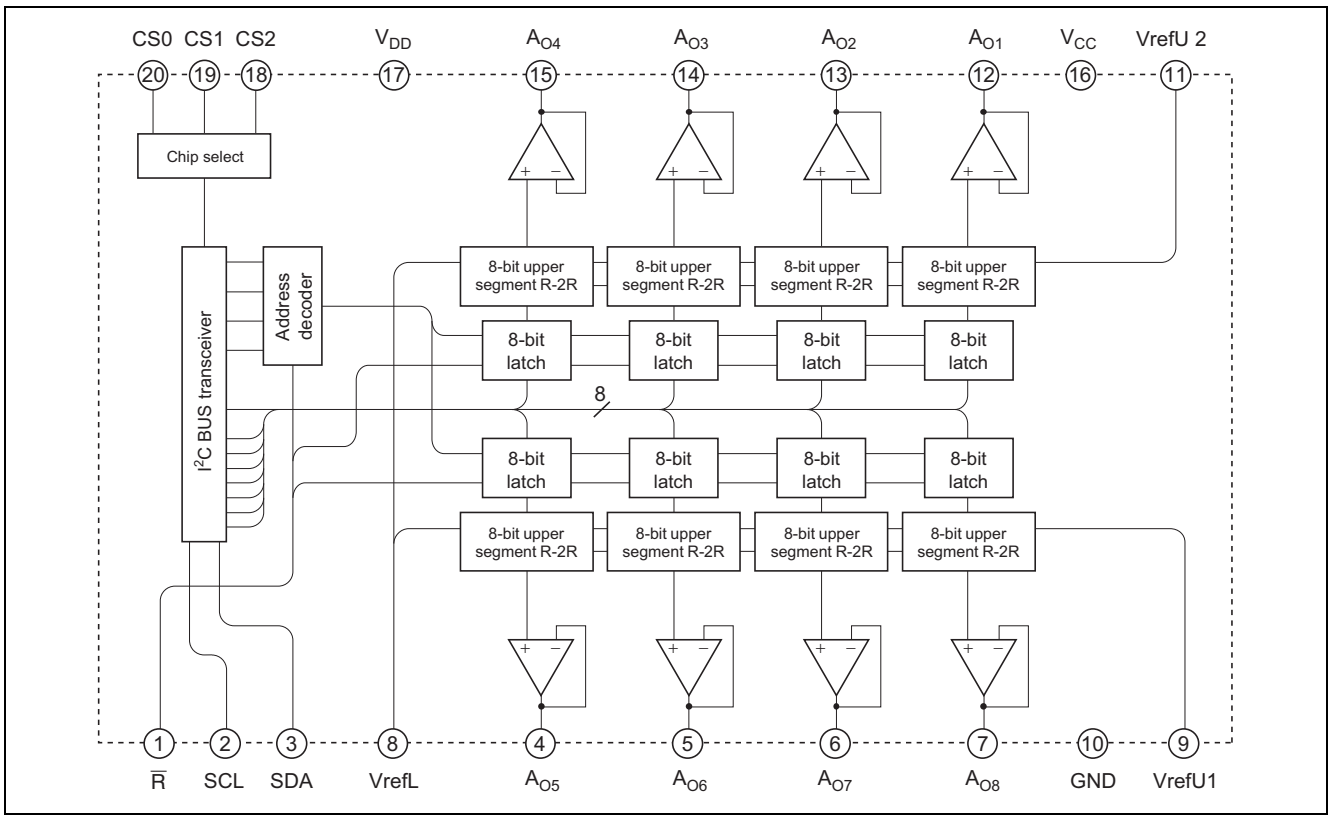
- Digital data transfer format: I²C BUS serial data method
- Output buffer operational amplifier
  It operates in the whole voltage range from VrefU (0 to 5 V) to ground.
- High output current drive capacity: ±1.0 mA over
- Preparation two high level reference voltage terminal because there are two high level reference voltage terminal, it can set up two kinds differ voltage range.

Application

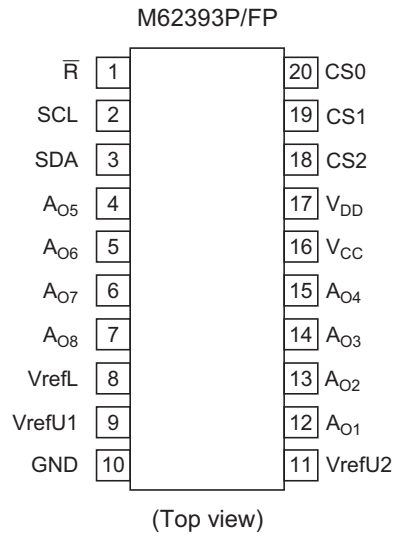
Conversion from digital control data to analog control data for home-use and industrial equipment.

Signal gain control or automatic adjustment of display-monitor or CTV.

Block Diagram



Pin Arrangement



Outline: 20P4 [P] (not recommend for new design)
PRSP0020DA-A (20P2N-A) [FP]

Pin Description

Pin No.	Pin Name	Function
3	SDA	Serial data input terminal
1	$\overline{R}$	Reset signal input terminal
2	SCL	Serial clock input terminal
12	Ao1	8-bit D/A converter output terminal
13	Ao2	
14	Ao3	
15	Ao4	
4	Ao5	
5	Ao6	
6	Ao7	
7	Ao8	
16	V_{CC}	Analog power supply terminal
17	V_{DD}	Digital power supply terminal
10	GND	Analog and digital common GND
8	VrefL	D/A converter low level reference voltage input terminal
9	VrefU1	D/A converter high level reference voltage input terminal 1
11	VrefU2	D/A converter high level reference voltage input terminal 2
18	CS2	Chip select data input terminal 2
19	CS1	Chip select data input terminal 1
20	CS0	Chip select data input terminal 0

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	–0.3 to +7.0	V
Supply voltage	V_{DD}	–0.3 to +7.0	V
D/A converter high level reference voltage	VrefU1, 2	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{DD} + 0.3	V
Output voltage	V_O	–0.3 to V_{DD} + 0.3	V
Power dissipation	Pd	990 (P) / 590 (FP)	mW
Operating temperature	Topr	–20 to +85	°C
Storage temperature	Tstg	–40 to +125	°C

Electrical Characteristics

<Digital Part>

(V_{CC}, V_{DD}, VrefU1, 2 = +5 V ± 10%, V_{CC} ≥ VrefU1, 2, GND = VrefL = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{DD}	4.5	5.0	5.5	V	
Supply current	I_{DD}	—	—	1.0	mA	CLK = 1 MHz operation, I_{AO} = 0 μA
Output low voltage (SDA)	V_{OL}	—	—	0.4	V	Isink = 3 mA
Input leak current	I_{ILK}	–10	—	10	μA	V_{IN} = 0 to V_{CC}
Input low voltage	V_{IL}	—	—	0.2 V_{CC}	V	
Input high voltage	V_{IH}	0.8 V_{CC}	—	—	V	

<Analog Part>

(V_{CC}, V_{DD}, VrefU1, 2 = +5 V ± 10%, V_{CC} ≥ VrefU1, 2, GND = VrefL = 0 V, Ta = –20 to +85°C, unless otherwise noted.)

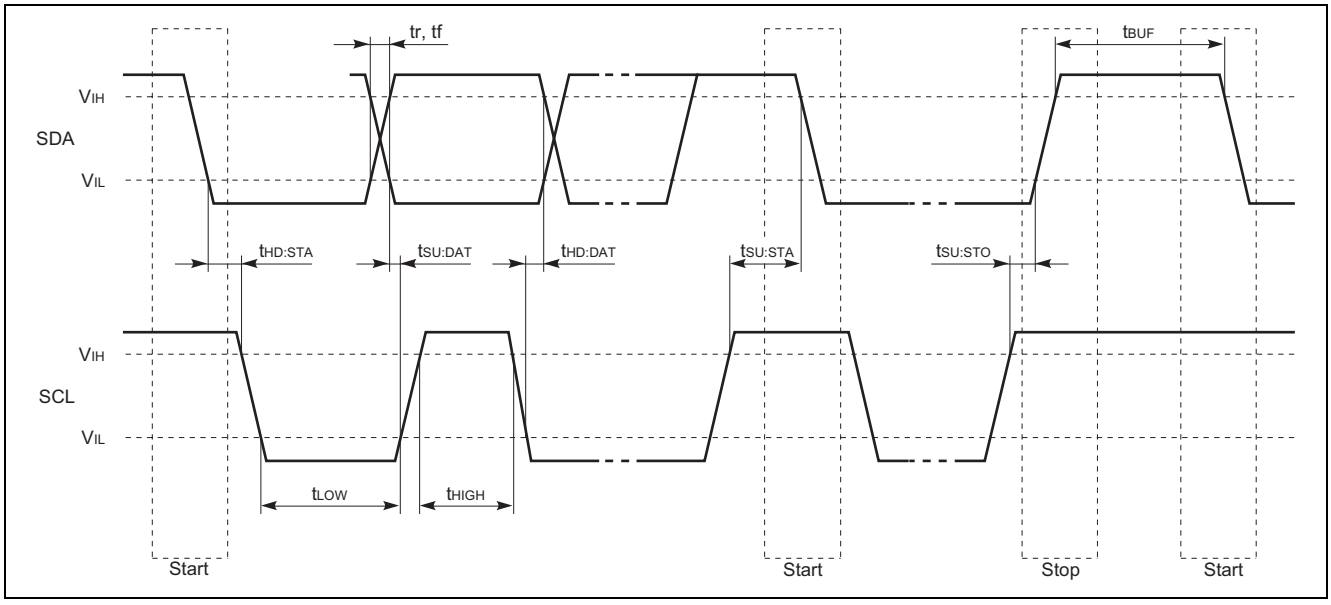
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Supply current	I_{CC}	—	1.6	3.2	mA	CLK = 1 MHz operation, I_{AO} = 0 μA
D/A converter high level reference voltage input current	IrefU	—	1.0	2.0	mA	VrefU = 5 V, VrefL = 0 V Data condition: at maximum current
D/A converter high level reference voltage range	VrefU	3.5	—	V_{CC}	V	The output dose not necessarily be the values within the reference voltage setting range.
D/A converter low level reference voltage range	VrefL	GND	—	V_{CC} – 3.5	V	
Buffer amplifier output voltage range	V_{AO}	0.1	—	V_{CC} – 0.1	V	I_{AO} = ±100 μA
		0.2	—	V_{CC} – 0.2	V	I_{AO} = ±500 μA
Buffer amplifier output current range	I_{AO}	–1.0	—	1.0	mA	Upper side saturation voltage = 0.3 V Lower side saturation voltage = 0.2 V
Differential nonlinearity	S_{DL}	–1.0	—	1.0	LSB	VrefU = 4.79 V VrefL = 0.95 V V_{CC} = 5.5 V (15 mV/LSB) Without load (I_{AO} = 0)
Nonlinearity	S_L	–1.5	—	1.5	LSB	
Zero code error	S_{ZERO}	–2.0	—	2.0	LSB	
Full scale error	S_{FULL}	–2.0	—	2.0	LSB	
Output capacitive load	C_O	—	—	0.1	μF	
Buffer amplifier output impedance	R_O	—	5.0	—	Ω	

I²C BUS Line Characteristics

Item	Symbol	Normal Mode		High Speed Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Time the bus must be free before a new transmission can start	t_{BUF}	4.7	—	1.3	—	µs
Hold time start condition. After this period. The first clock pulse is generated.	$t_{HD:STA}$	4.0	—	0.6	—	µs
Low period of the clock	t_{LOW}	4.7	—	1.3	—	µs
High period of the clock	t_{HIGH}	4.0	—	0.6	—	µs
Setup time for start condition (only relevant for a repeated start condition)	$t_{SU:STA}$	4.7	—	4.7	—	µs
Hold time data	$t_{HD:DAT}$	0	—	0	0.9	µs
Setup time data	$t_{SU:DAT}$	250	—	100	—	ns
Rise time of both SDA and SCL lines	t_R	—	1000	20	300	ns
Fall time of both SDA and SCL lines	t_F	—	300	20	300	ns
Setup time for stop condition	$t_{SU:STO}$	4.0	—	0.6	—	µs

Note: Transmitter must internally at reset a hold time to bridge the undefined region (300 ns Max) of the falling edge of SCL.

Timing Chart

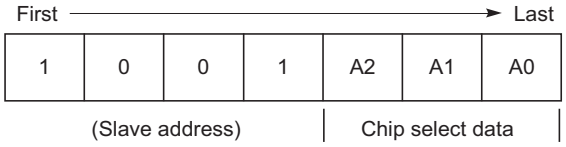


I²C BUS Format

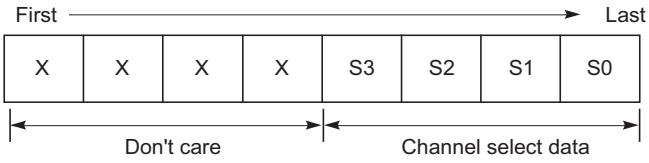
STA	Slave address	W	A	Sub address	A	DAC data	A	STP

Digital Data Format

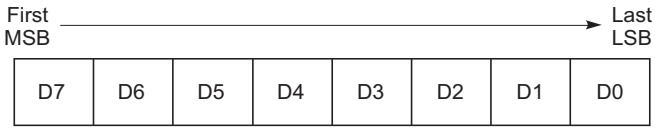
- Slave Address



- Sub Address



- DAC Data



(1) Chip Select Data

MSB LSB

A2	A1	A0	CS2	CS1	CS0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
:	:	:	:	:	:
1	1	1	1	1	1

(2) Channel Select Data

MSB LSB

S3	S2	S1	S0	Channel Selection
0	0	0	0	Don't care
0	0	0	1	ch1 selection
0	0	1	0	ch2 selection
:	:	:	:	:
0	1	1	1	ch7 selection
1	0	0	0	ch8 selection
1	0	0	1	Don't care
:	:	:	:	:
1	1	1	1	Don't care

(3) DAC Data

First MSB → Last LSB

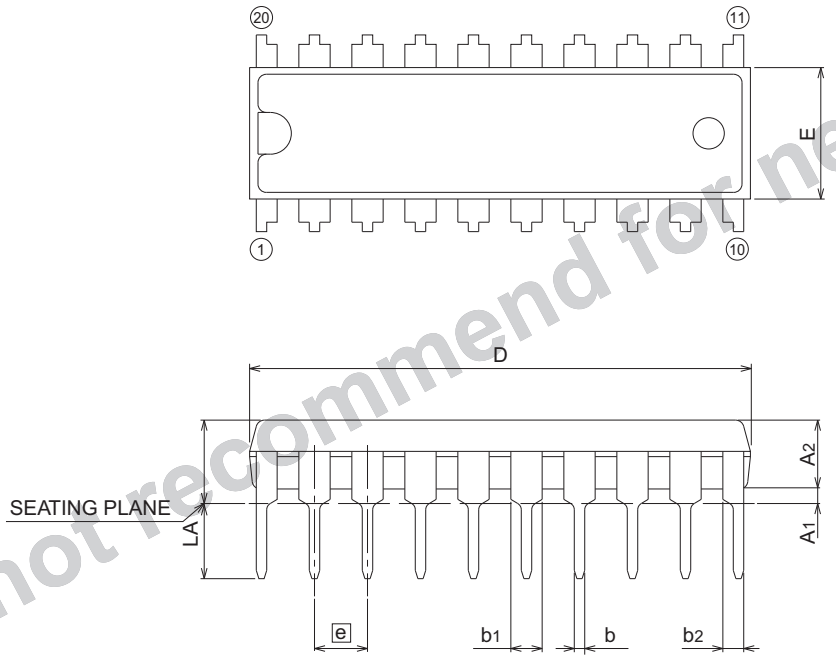
D7	D6	D5	D4	D3	D2	D1	D0	DAC Output
0	0	0	0	0	0	0	0	(VrefU – VrefL) / 256 × 1 + VrefL
0	0	0	0	0	0	0	1	(VrefU – VrefL) / 256 × 2 + VrefL
0	0	0	0	0	0	1	0	(VrefU – VrefL) / 256 × 3 + VrefL
0	0	0	0	0	0	1	1	(VrefU – VrefL) / 256 × 4 + VrefL
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	(VrefU – VrefL) / 256 × 255 + VrefL
1	1	1	1	1	1	1	1	VrefU

Package Dimensions

20P4

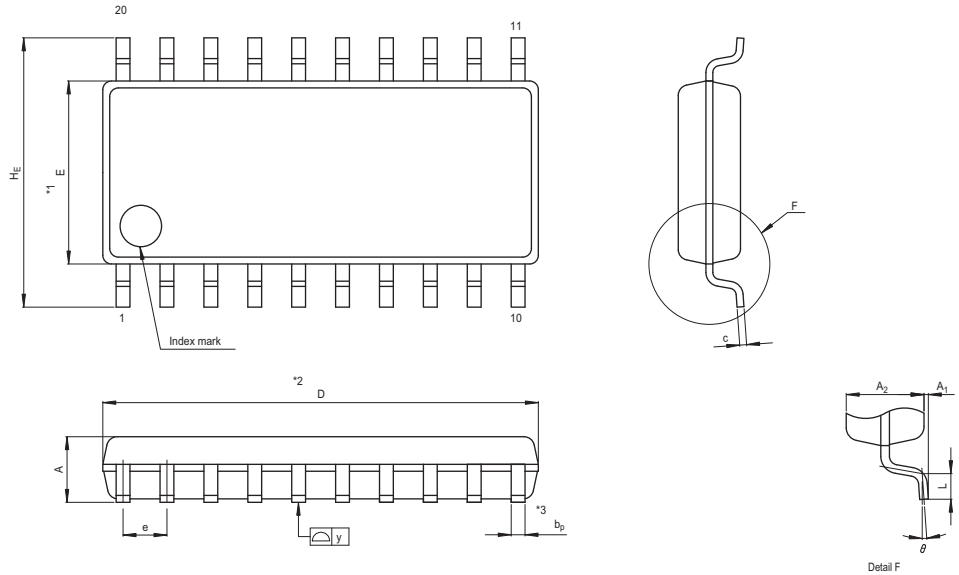
Plastic 20pin 300mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
DIP20-P-300-2.54	—	1.3	Alloy 42/Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b	0.4	0.5	0.6
b_1	1.4	1.5	1.8
b_2	0.9	1.0	1.3
c	0.22	0.27	0.34
D	23.8	24.0	24.2
E	6.15	6.3	6.45
e	—	2.54	—
e1	—	7.62	—
L	3.0	—	—
θ	0°	—	15°

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.3x12.6-1.27	PRSP0020DA-A	20P2N-A	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.5	12.6	12.7
E	5.2	5.3	5.4
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

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