



## General Description

The IPP200N15N3G use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable.



**TO-220**

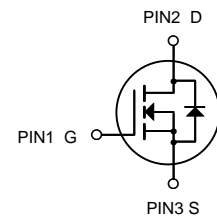
## General Features

$V_{DS} = 150V$   $I_D = 120A$

$R_{DS(ON)} < 11.5m\Omega @ V_{GS} = 10V$

## Applications

- Consumer electronic power supply Motor control
- Synchronous-rectification Isolated DC
- Synchronous-rectification applications



N-Channel MOSFET

## Package Marking and Ordering Information

Product ID	Pack	Brand	Qty(PCS)
IPP200N15N3G	TO-220	HXY MOSFET	50

## Absolute Maximum Ratings at $T_j = 25^\circ C$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	VDS	150	V
Gate source voltage	VGS	$\pm 20$	V
Continuous drain current <sup>1)</sup>	ID	120	A
Pulsed drain current <sup>2)</sup>	ID, pulse	352	A
Power dissipation <sup>3)</sup>	PD	178.6	W
Single pulsed avalanche energy <sup>5)</sup>	EAS	204.8	mJ
Operation and storage temperature	Tstg, Tj	-55 to 150	$^\circ C$
Thermal resistance, junction-case	R $\theta$ JC	0.7	$^\circ C/W$
Thermal resistance, junction-ambient <sup>4)</sup>	R $\theta$ JA	52	$^\circ C/W$



**Electrical Characteristics** (T<sub>J</sub> = 25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Static Characteristics</b>							
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	150	-	-	V	
Gate-body Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0V, V <sub>GS</sub> = ±20V	-	-	±100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V	T <sub>J</sub> =25°C	-	-	1	μA
			T <sub>J</sub> =100°C	-	-	100	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2	3	4	V	
Drain-Source On-Resistance <sup>4</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A	-	9.5	11.5	mΩ	
Forward Transconductance <sup>4</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 20A	-	69	-	S	
<b>Dynamic Characteristics<sup>5</sup></b>							
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 75V, V <sub>GS</sub> = 0V, f = 1MHz	-	3310	-	pF	
Output Capacitance	C <sub>oss</sub>		-	268	-		
Reverse Transfer Capacitance	C <sub>rss</sub>		-	9.4	-		
Gate Resistance	R <sub>g</sub>	f = 1MHz	-	3.2	-	Ω	
<b>Switching Characteristics<sup>5</sup></b>							
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 75V, I <sub>D</sub> = 20A	-	45	-	nC	
Gate-Source Charge	Q <sub>gs</sub>		-	15	-		
Gate-Drain Charge	Q <sub>gd</sub>		-	8.5	-		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 75V, R <sub>G</sub> = 3Ω, I <sub>D</sub> = 20A	-	16	-	ns	
Rise Time	t <sub>r</sub>		-	12	-		
Turn-Off Delay Time	t <sub>d(off)</sub>		-	30	-		
Fall Time	t <sub>f</sub>		-	18	-		
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20A, di/dt = 100A/μs	-	76	-	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	182	-	nC	
<b>Drain-Source Body Diode Characteristics</b>							
Diode Forward Voltage <sup>4</sup>	V <sub>SD</sub>	I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V	-	-	1.2	V	
Continuous Source Current	I <sub>S</sub>	T <sub>C</sub> = 25°C	-	-	120	A	

Notes:

1. Repetitive rating, pulse width limited by junction temperature T<sub>J(MAX)</sub> = 150°C
2. The EAS data shows Max. rating . The test condition is V<sub>DD</sub> = 50V, V<sub>GS</sub> = 10V, L = 0.4mH, I<sub>AS</sub> = 32A.
3. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.
5. This value is guaranteed by design hence it is not included in the production test.



### Typical Characteristics

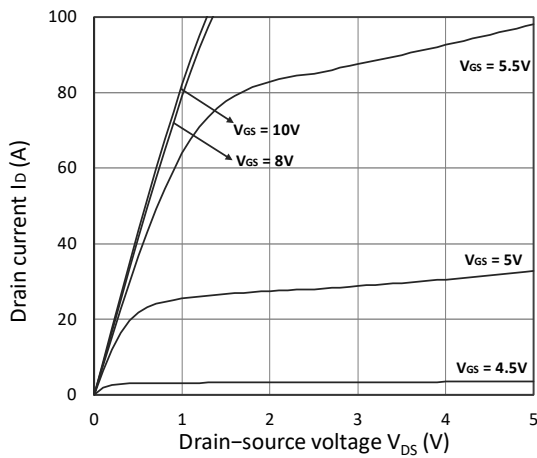


Figure 1. Output Characteristics

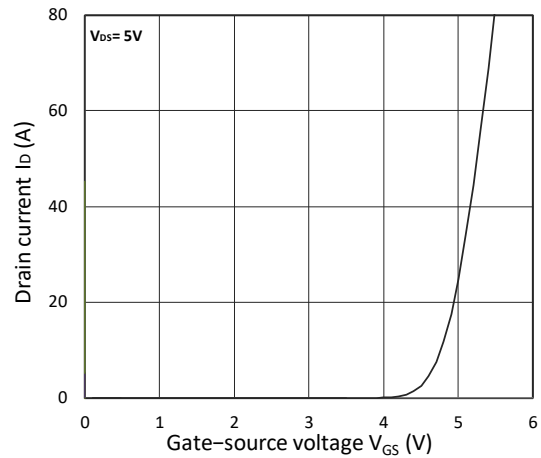


Figure 2. Transfer Characteristics

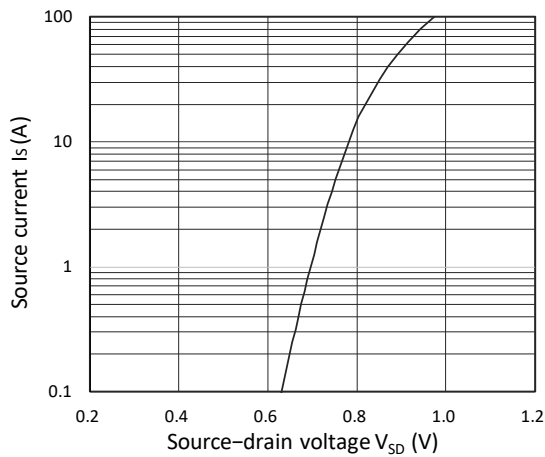


Figure 3. Forward Characteristics of Reverse

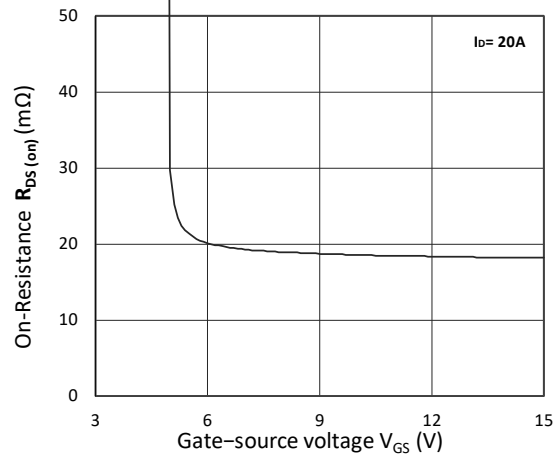


Figure 4.  $R_{DS(on)}$  vs.  $V_{GS}$

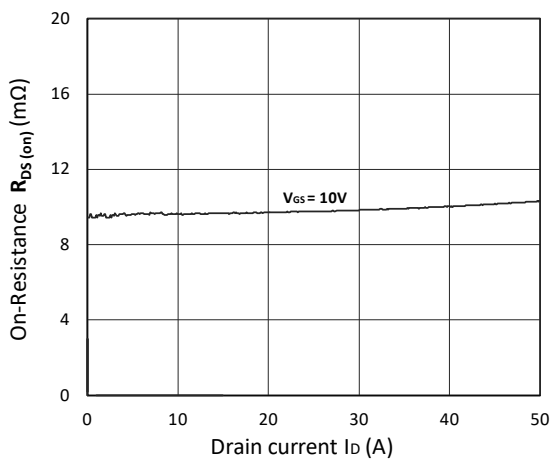


Figure 5.  $R_{DS(on)}$  vs.  $I_D$

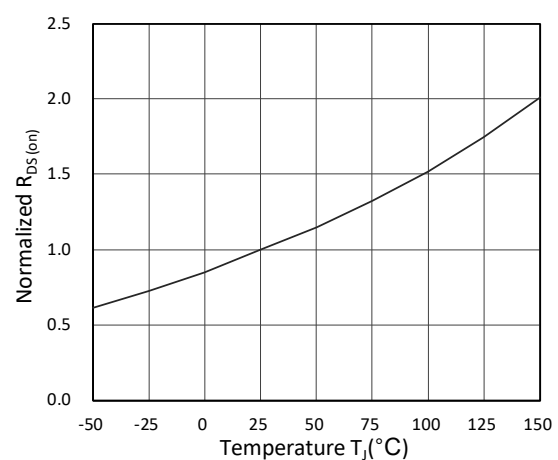


Figure 6. Normalized  $R_{DS(on)}$  vs. Temperature

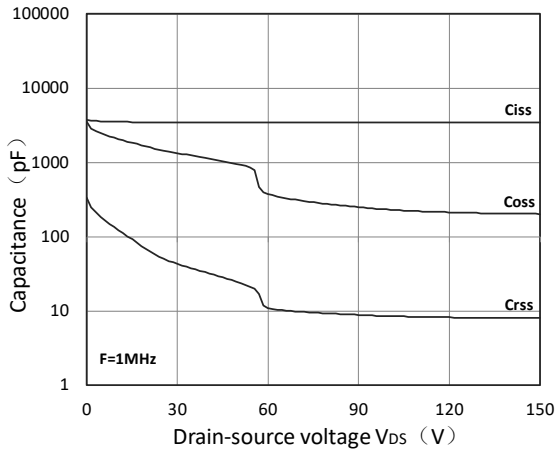


Figure 7. Capacitance Characteristics

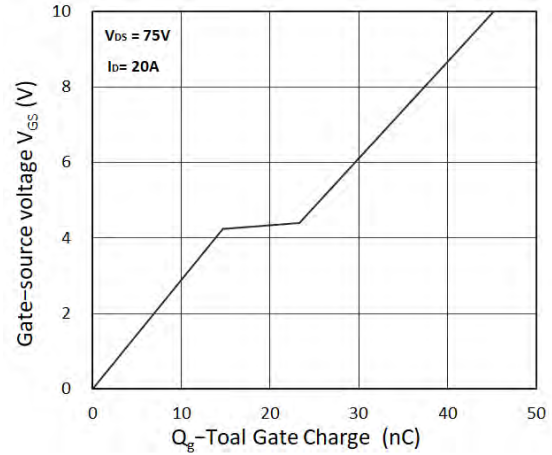


Figure 8. Gate Charge Characteristics

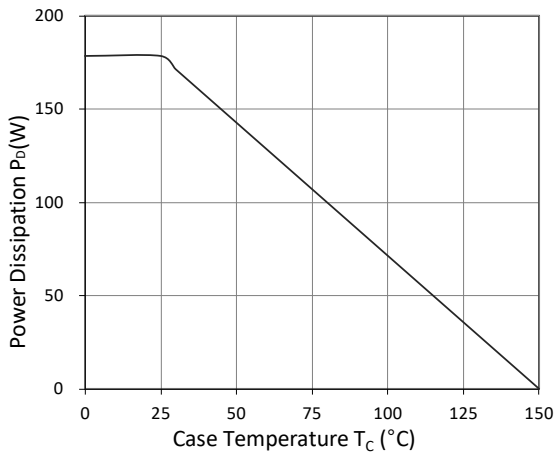


Figure 9. Power Dissipation

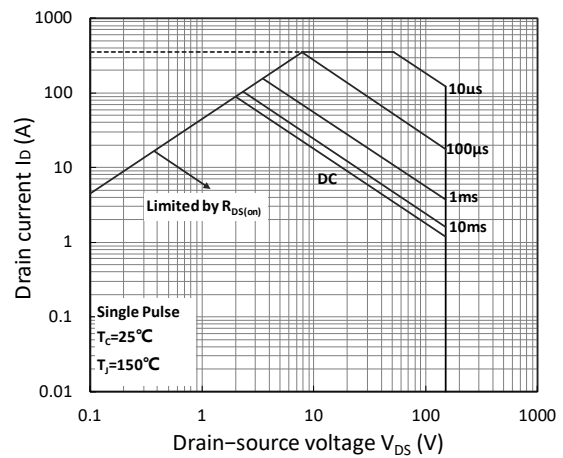


Figure 10. Safe Operating Area

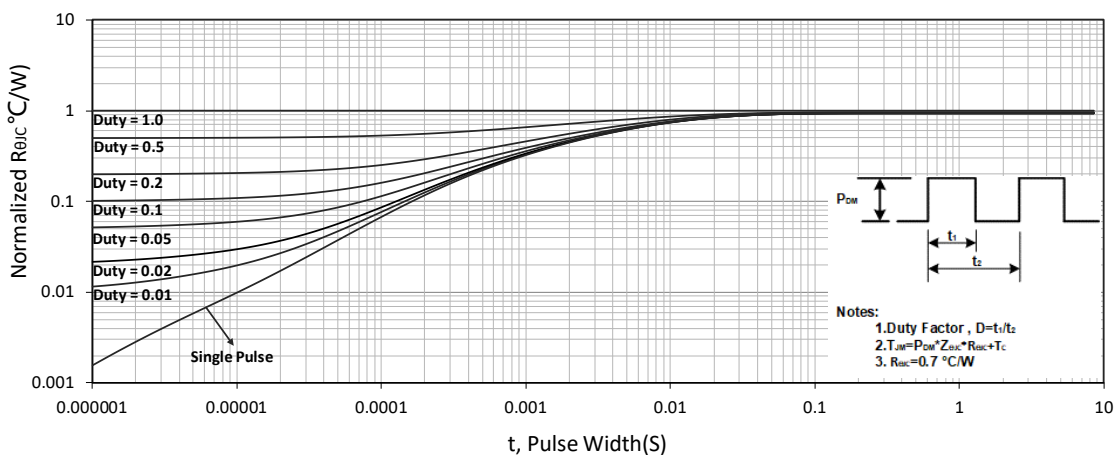


Figure 11. Normalized Maximum Transient Thermal Impedance



### Test Circuit

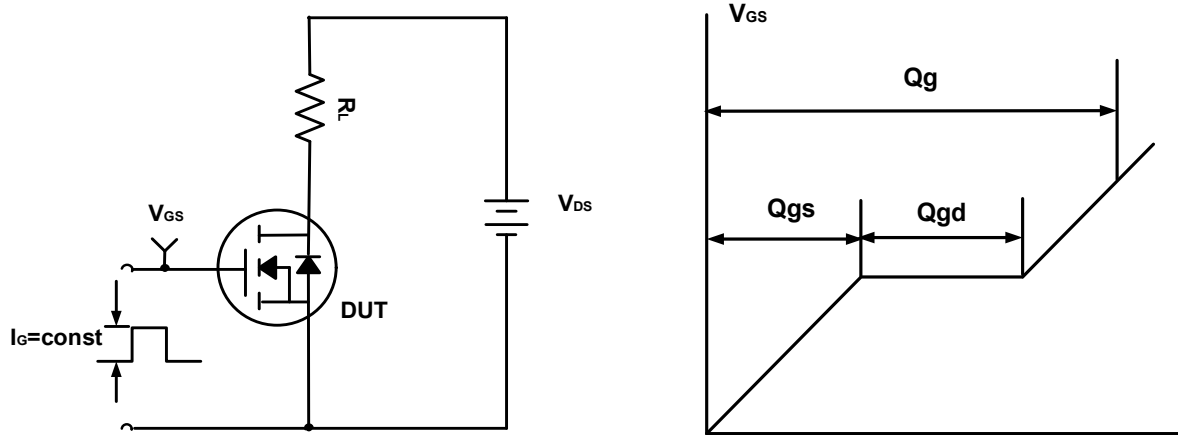


Figure A. Gate Charge Test Circuit & Waveforms

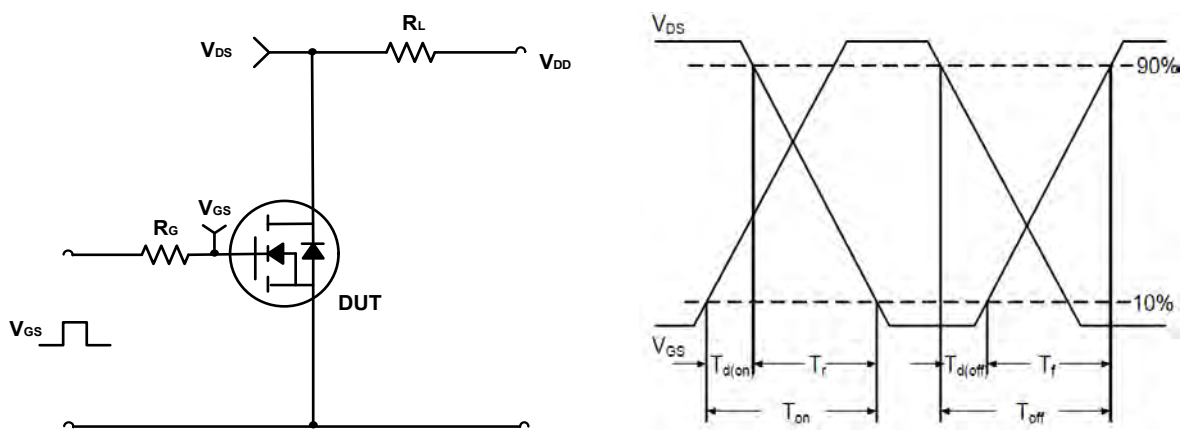


Figure B. Switching Test Circuit & Waveforms

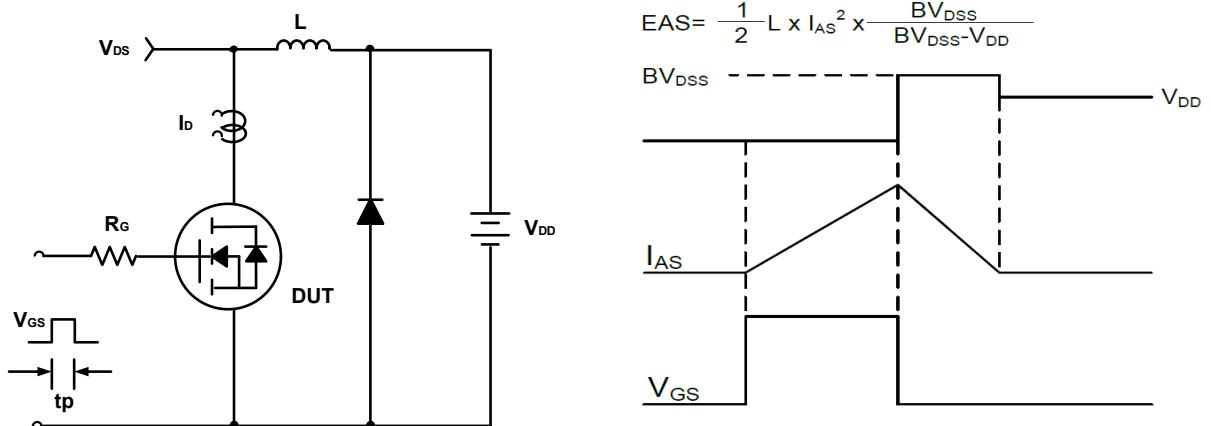
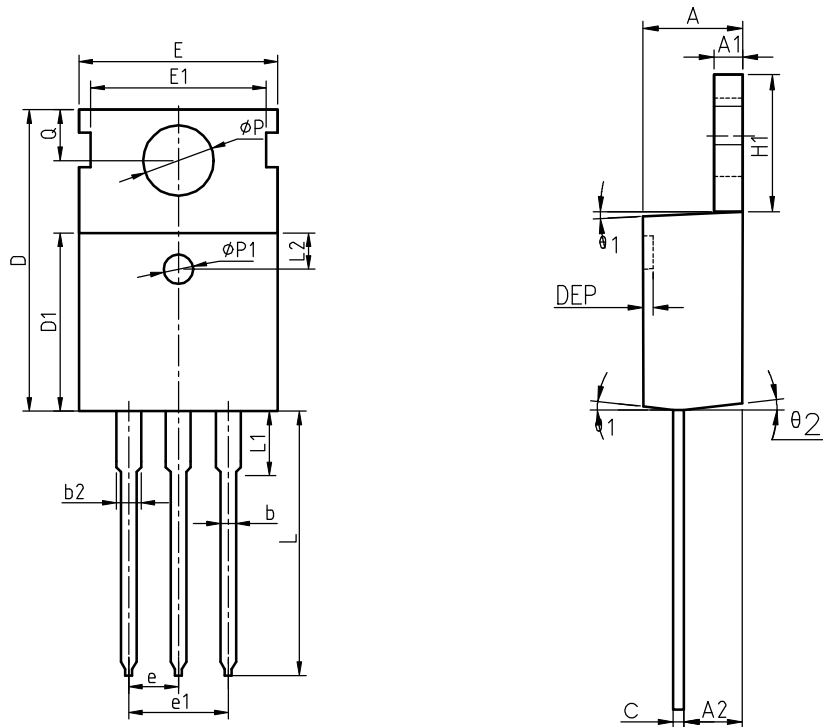


Figure C. Unclamped Inductive Switching Circuit & Waveforms



Package Information

TO-220



COMMON DIMENSIONS

SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	4.40	4.57	4.70	0.173	0.180	0.185
A1	1.27	1.30	1.33	0.050	0.051	0.052
A2	2.35	2.40	2.50	0.093	0.094	0.098
b	0.77	0.80	0.90	0.030	0.031	0.035
b2	1.17	1.27	1.36	0.046	0.050	0.054
c	0.48	0.50	0.56	0.019	0.020	0.022
D	15.40	15.60	15.80	0.606	0.614	0.622
D1	9.00	9.10	9.20	0.354	0.358	0.362
DEP	0.05	0.10	0.20	0.002	0.004	0.008
E	9.80	10.00	10.20	0.386	0.394	0.402
E1	-	8.70	-	-	0.343	-
E2	9.80	10.00	10.20	0.386	0.394	0.402
e		2.54	BSC		0.100	BSC
e1		5.08	BSC		0.200	BSC
H1	6.40	6.50	6.60	0.252	0.256	0.260
L	12.75	13.50	13.65	0.502	0.531	0.537
L1	-	3.10	3.30	-	0.122	0.130
L2		2.50	REF		0.098	REF
P	3.50	3.60	3.63	0.138	0.142	0.143
P1	3.50	3.60	3.63	0.138	0.142	0.143
Q	2.73	2.80	2.87	0.107	0.110	0.113
$\theta_1$	5°	7°	9°	5°	7°	9°
$\theta_2$	1°	3°	5°	1°	3°	5°
$\theta_3$	1°	3°	5°	1°	3°	5°



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