

NTD4302

MOSFET – Power, N-Channel, DPAK/IPAK 68 A, 30 V

Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- I_{DSS} Specified at Elevated Temperature
- DPAK Mounting Information Provided
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC-DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery Powered Products:
i.e., Computers, Printers, Cellular and Cordless Telephones,
and PCMCIA Cards

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	30	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 20	Vdc
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	1.65	$^\circ\text{C/W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	75	W
Continuous Drain Current @ $T_C = 25^\circ\text{C}$ (Note 4)	I_D	68	A
Continuous Drain Current @ $T_C = 100^\circ\text{C}$	I_D	43	A
Thermal Resistance – Junction-to-Ambient (Note 2)	$R_{\theta JA}$	67	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.87	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	11.3	A
Continuous Drain Current @ $T_A = 100^\circ\text{C}$	I_D	7.1	A
Pulsed Drain Current (Note 3)	I_{DM}	36	A
Thermal Resistance – Junction-to-Ambient (Note 1)	$R_{\theta JA}$	120	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.04	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	8.4	A
Continuous Drain Current @ $T_A = 100^\circ\text{C}$	I_D	5.3	A
Pulsed Drain Current (Note 3)	I_{DM}	28	A
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 30\text{ Vdc}$, $V_{GS} = 10\text{ Vdc}$, Peak $I_L = 17\text{ Apk}$, $L = 5.0\text{ mH}$, $R_G = 25\ \Omega$)	E_{AS}	722	mJ
Maximum Lead Temperature for Soldering Purposes, 1/8 in from case for 10 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

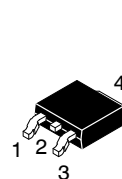
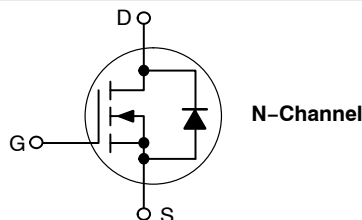
1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. When surface mounted to an FR4 board using 0.5 sq. in. drain pad size.
3. Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.
4. Current Limited by Internal Lead Wires.



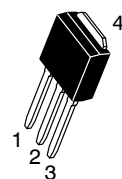
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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	7.8 m Ω @ 10 V	68 A

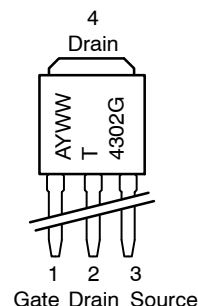
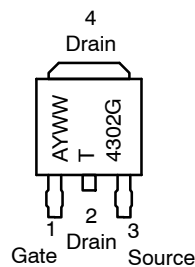


DPAK
CASE 369C
(Surface Mount)
STYLE 2



IPAK
CASE 369D
(Straight Lead)
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENTS



A = Assembly Location*
Y = Year
WW = Work Week
T4302 = Device Code
G = Pb-Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD4302

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μA) Positive Temperature Coefficient	V _{(BR)DSS}	30 –	– 25	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{GS} = 0 Vdc, V _{DS} = 30 Vdc, T _J = 25°C) (V _{GS} = 0 Vdc, V _{DS} = 30 Vdc, T _J = 125°C)	I _{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±20 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	±100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Negative Temperature Coefficient	V _{GS(th)}	1.0 –	1.9 –3.8	3.0 –	Vdc
Static Drain-Source On-State Resistance (V _{GS} = 10 Vdc, I _D = 20 Adc) (V _{GS} = 10 Vdc, I _D = 10 Adc) (V _{GS} = 4.5 Vdc, I _D = 5.0 Adc)	R _{DS(on)}	– – –	0.0078 0.0078 0.010	0.010 0.010 0.013	Ω
Forward Transconductance (V _{DS} = 15 Vdc, I _D = 10 Adc)	g _{FS}	–	20	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 24 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	2050	2400	pF
Output Capacitance		C _{oss}	–	640	800	
Reverse Transfer Capacitance		C _{rss}	–	225	310	

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	(V _{DD} = 25 Vdc, I _D = 1.0 Adc, V _{GS} = 10 Vdc, R _G = 6.0 Ω)	t _{d(on)}	–	11	20	ns
Rise Time		t _r	–	15	25	
Turn-Off Delay Time		t _{d(off)}	–	85	130	
Fall Time		t _f	–	55	90	
Turn-On Delay Time	(V _{DD} = 25 Vdc, I _D = 1.0 Adc, V _{GS} = 10 Vdc, R _G = 2.5 Ω)	t _{d(on)}	–	11	20	ns
Rise Time		t _r	–	13	20	
Turn-Off Delay Time		t _{d(off)}	–	55	90	
Fall Time		t _f	–	40	75	
Turn-On Delay Time	(V _{DD} = 24 Vdc, I _D = 20 Adc, V _{GS} = 10 Vdc, R _G = 2.5 Ω)	t _{d(on)}	–	15	–	ns
Rise Time		t _r	–	25	–	
Turn-Off Delay Time		t _{d(off)}	–	40	–	
Fall Time		t _f	–	58	–	
Gate Charge	(V _{DS} = 24 Vdc, I _D = 2.0 Adc, V _{GS} = 10 Vdc)	Q _T	–	55	80	nC
		Q _{gs} (Q1)	–	5.5	–	
		Q _{gd} (Q2)	–	15	–	

BODY-DRAIN DIODE RATINGS (Note 5)

Diode Forward On-Voltage (I _S = 2.3 Adc, V _{GS} = 0 Vdc) (I _S = 20 Adc, V _{GS} = 0 Vdc) (I _S = 2.3 Adc, V _{GS} = 0 Vdc, T _J = 125°C)		V _{SD}	–	0.75	1.0	Vdc
			–	0.90	–	
			–	0.65	–	
Reverse Recovery Time	(I _S = 2.3 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/μs)	t _{rr}	–	39	65	ns
		t _a	–	20	–	
		t _b	–	19	–	
Reverse Recovery Stored Charge		Q _{rr}	–	0.043	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Indicates Pulse Test: Pulse Width = 300 μsec max, Duty Cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperature.

TYPICAL CHARACTERISTICS

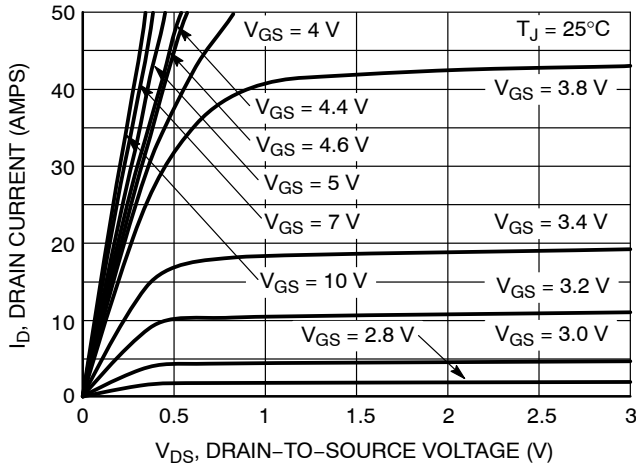


Figure 1. On-Region Characteristics

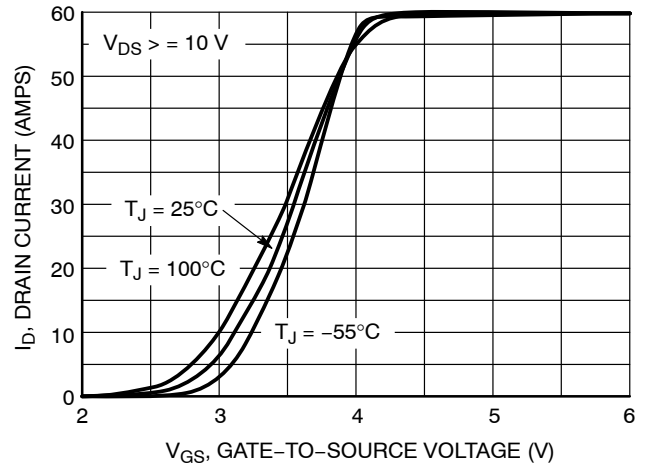


Figure 2. Transfer Characteristics

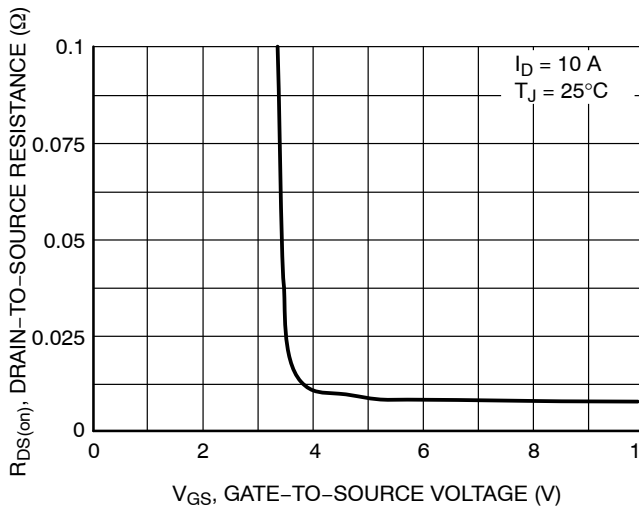


Figure 3. On-Resistance vs. Gate-to-Source Voltage

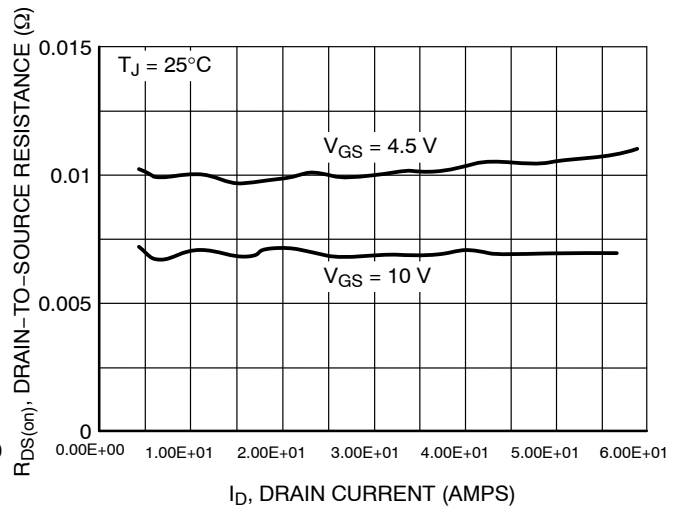


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

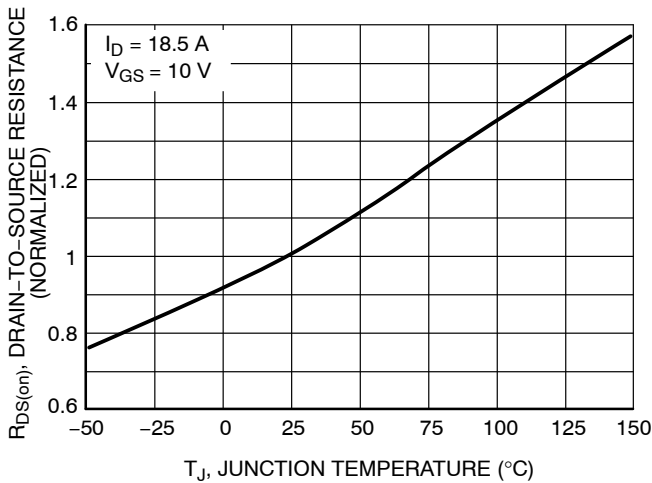


Figure 5. On-Resistance Variation with Temperature

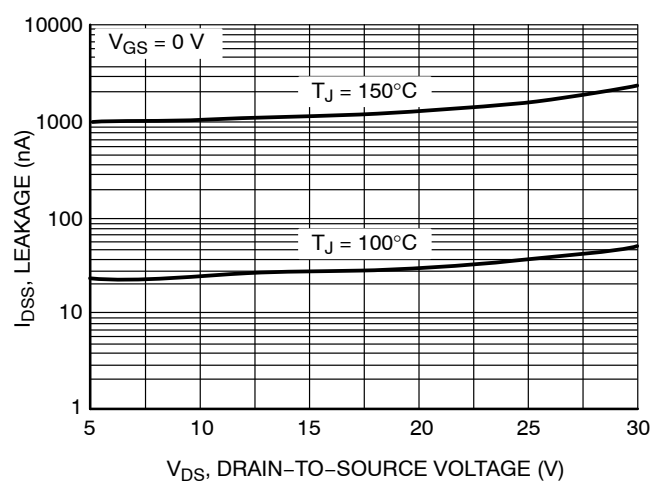


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

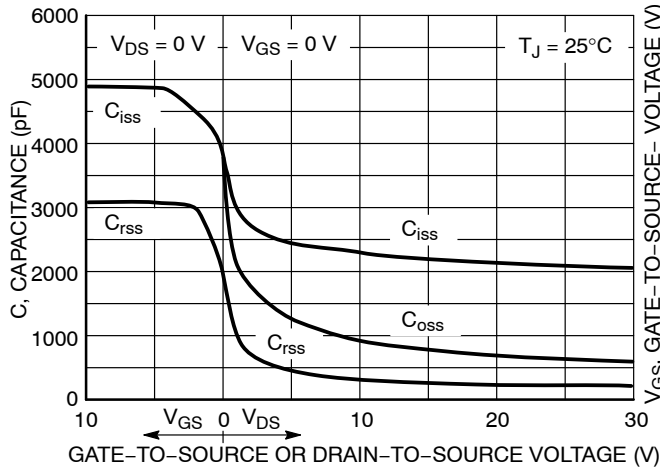


Figure 7. Capacitance Variation

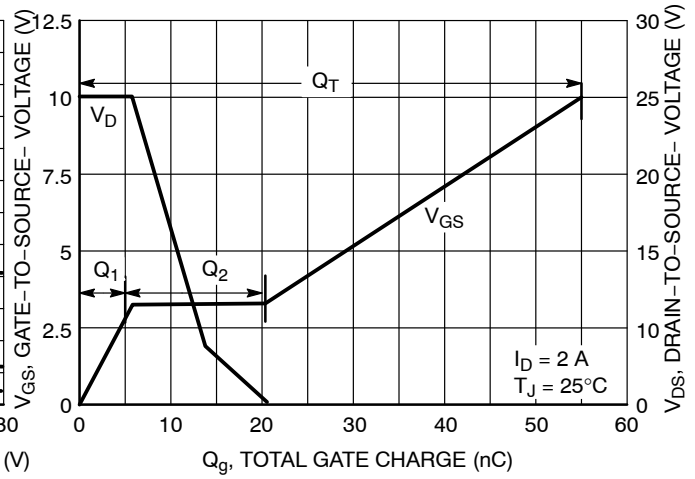


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

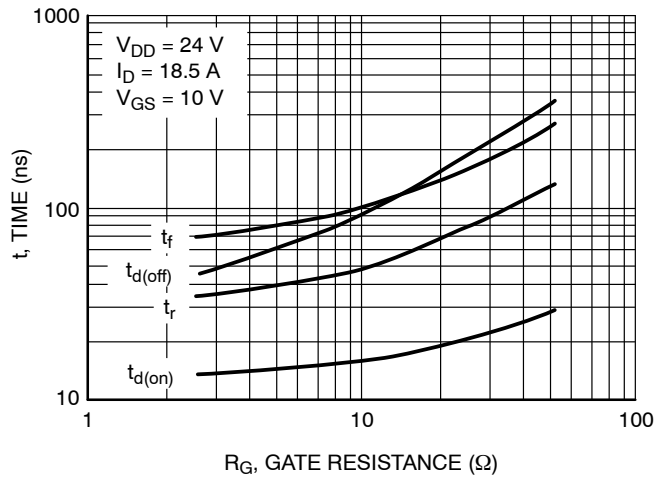


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

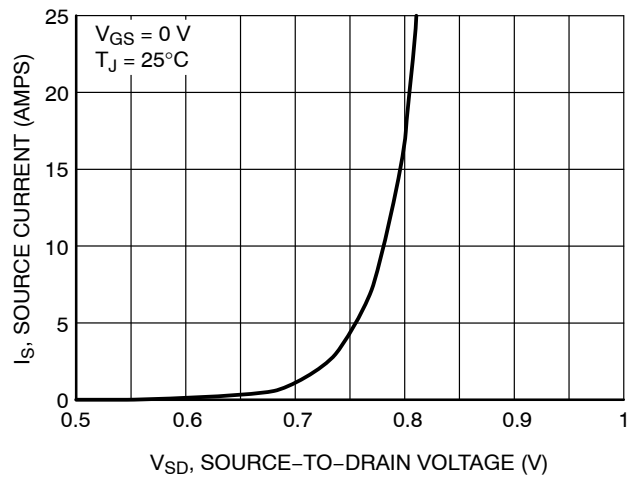


Figure 10. Diode Forward Voltage vs. Current

NTD4302

TYPICAL CHARACTERISTICS

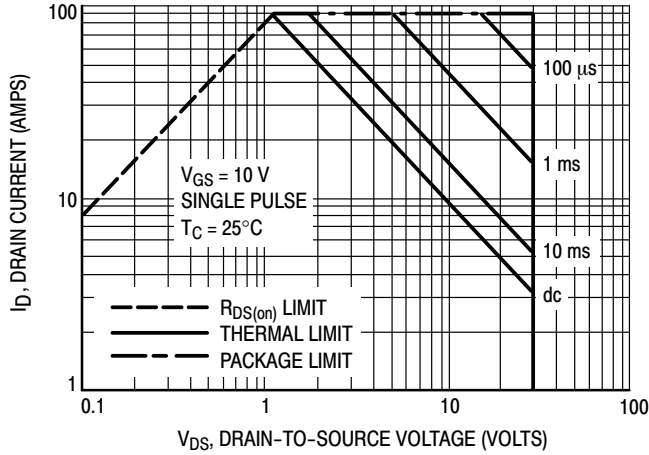


Figure 11. Maximum Rated Forward Biased Safe Operating Area

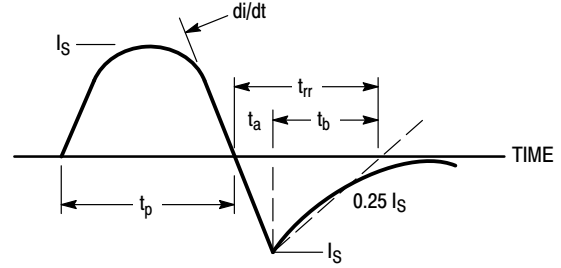


Figure 12. Diode Reverse Recovery Waveform

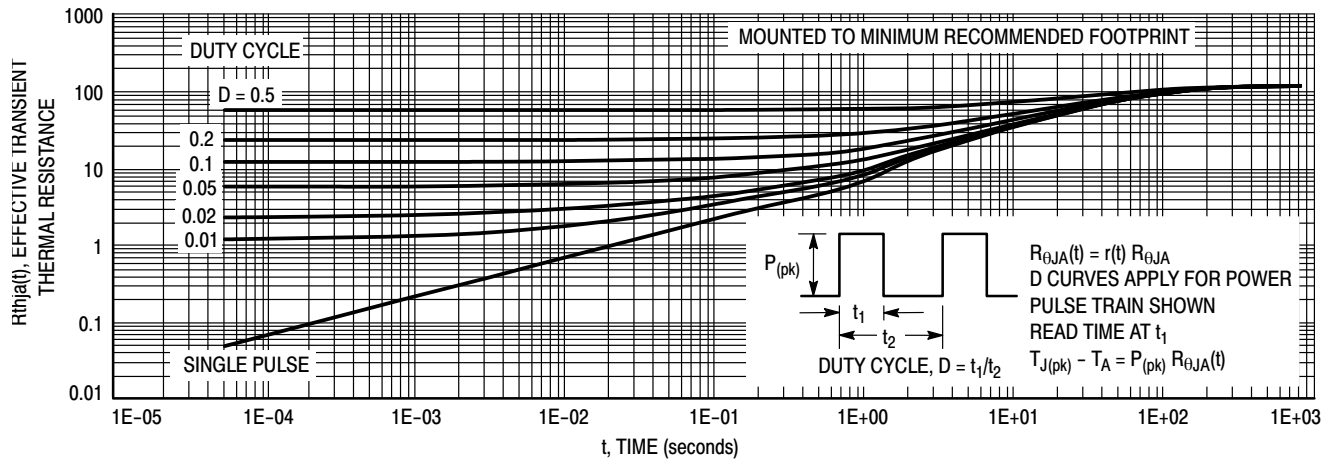


Figure 13. Thermal Response - Various Duty Cycles

ORDERING INFORMATION

Device	Package Type	Package	Shipping [†]
NTD4302G	DPAK	369C (Pb-Free)	75 Units / Rail
NTD4302-1G	IPAK	369D (Pb-Free)	75 Units / Rail
NTD4302T4G	DPAK	369C (Pb-Free)	2500 Tape & Reel

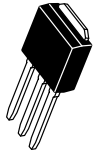
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

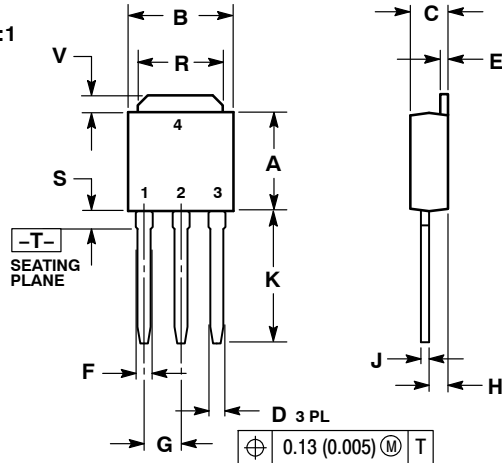
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IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

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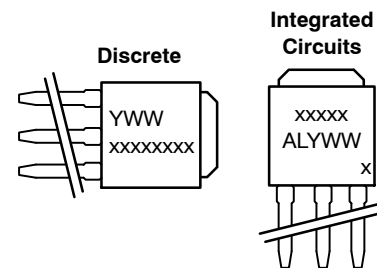


- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

MARKING DIAGRAMS

- STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE
- STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR



xxxxxxxx = Device Code
A = Assembly Location
IL = Wafer Lot
Y = Year
WW = Work Week

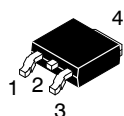
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DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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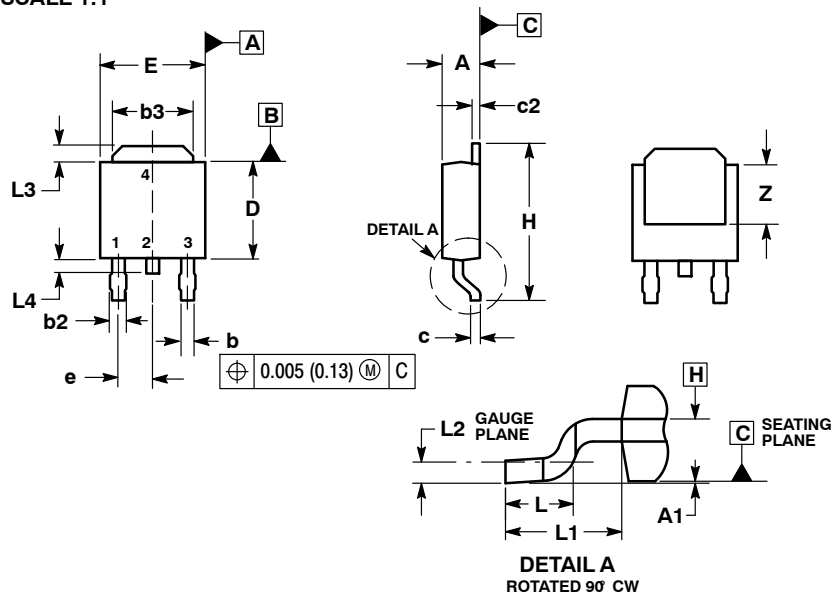
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DPAK (SINGLE GAUGE)

CASE 369AA-01

ISSUE B

DATE 03 JUN 2010



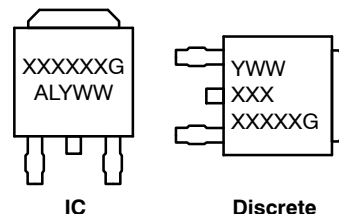
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

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2. ANODE
3. GATE
4. ANODE
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PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE
- STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2
- STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

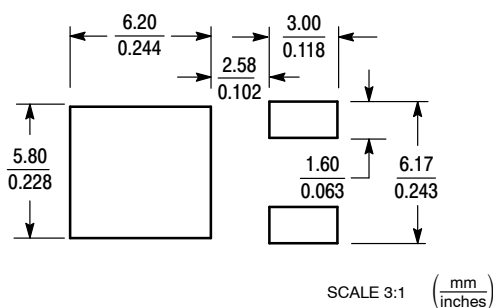
GENERIC MARKING DIAGRAM*



XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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