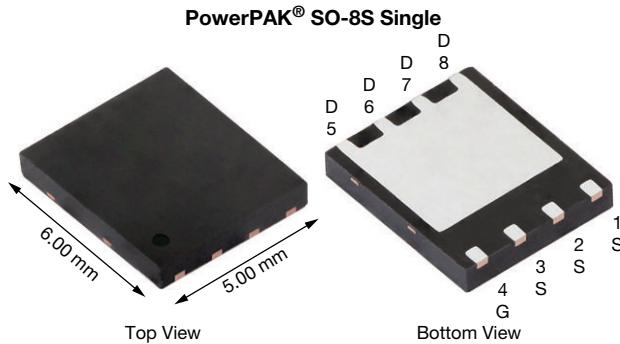


N-Channel 60 V (D-S) MOSFET



FEATURES

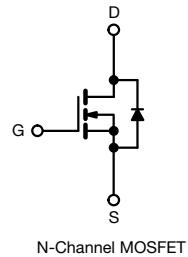
- TrenchFET® Gen IV power MOSFET
- Very low $R_{DS(on)} \times Q_g$ figure-of-merit (FOM)
- Leadership $R_{DS(on)}$ minimizes power loss from conduction
- 100 % R_g and UIS tested
- Enhance power dissipation and lower R_{thJC}
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- DC/DC converters
- OR-ing and hot swap switch
- Power supplies
- Motor drive control
- Battery management



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	60
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00115
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 7.5$ V	0.0013
Q_g typ. (nC)	81
I_D (A) ^a	359
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK SO-8S
Lead (Pb)-free and halogen-free	SiRS4600DP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current ($T_J = 150$ °C)	I_D	359	A
		287	
		62 b, c	
		50 b, c	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	500	A
Continuous source-drain diode current	I_S	252	
		7.5 b, c	
Single pulse avalanche current	I_{AS}	68	mJ
Single pulse avalanche energy	E_{AS}	231	
Maximum power dissipation	P_D	278	W
		178	
		8.3 b, c	
		5.3 b, c	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	R_{thJA}	10	15	°C/W
Maximum junction-to-case (drain)	R_{thJC}	0.3	0.45	

Notes

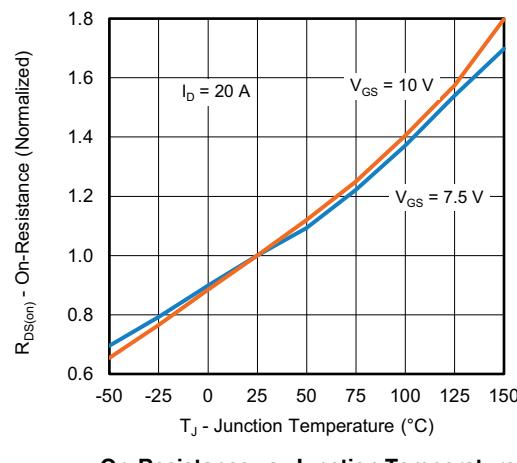
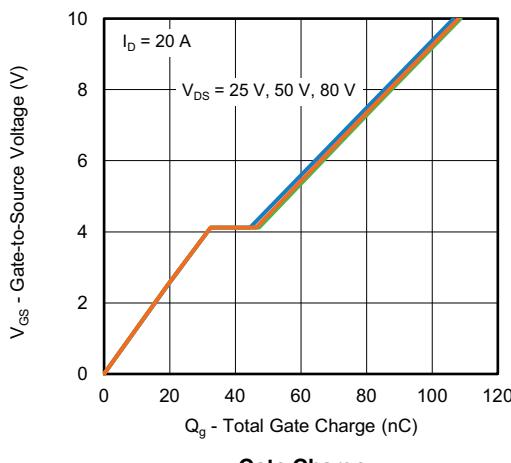
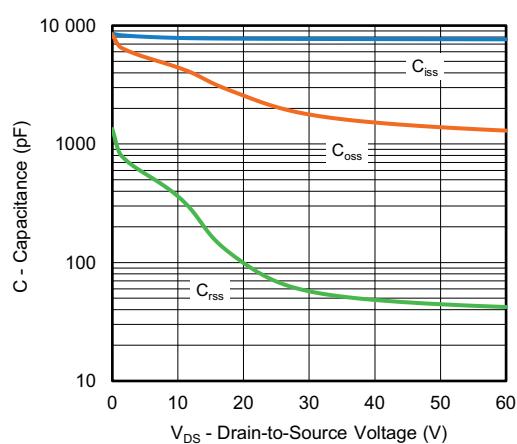
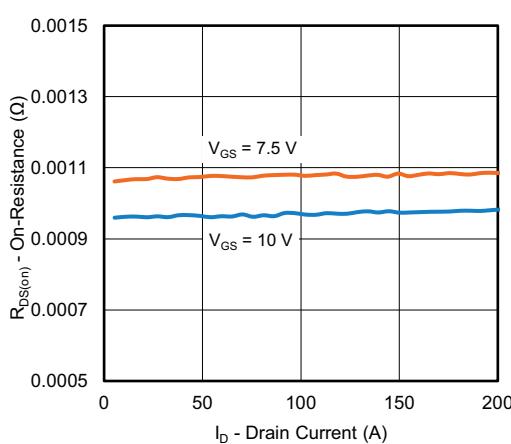
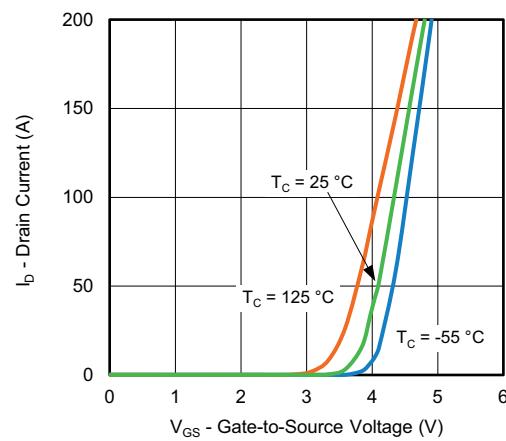
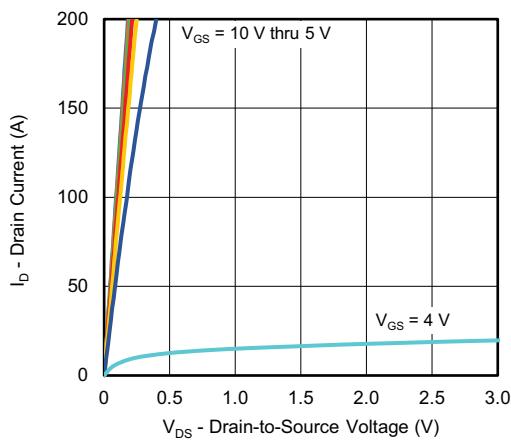
- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 45 °C/W

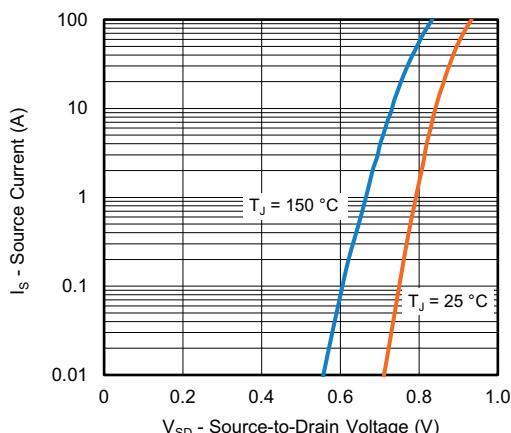
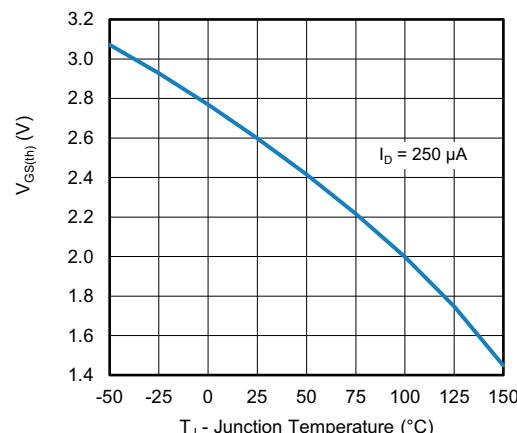
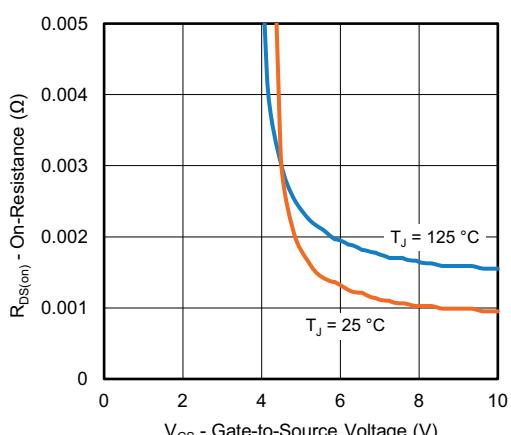
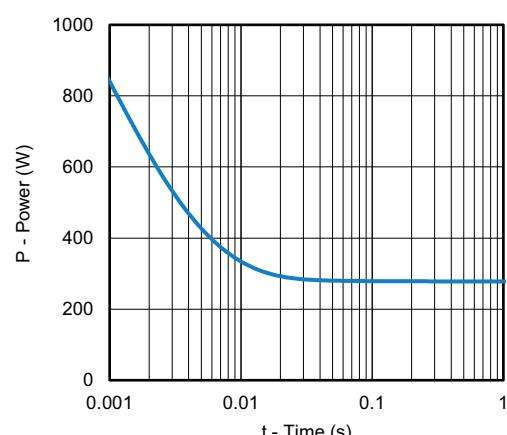
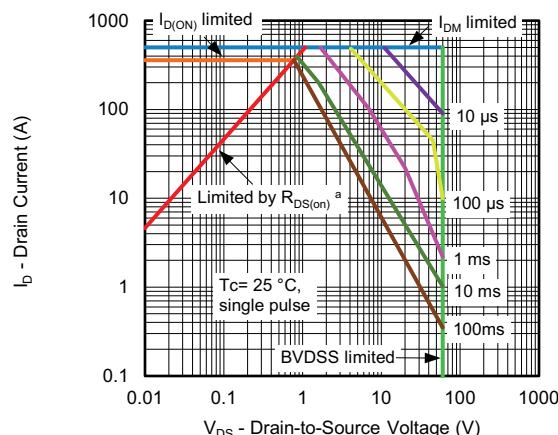
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10 \text{ mA}$	-	32	-	$\text{mV}/^\circ\text{C}$
$V_{GS(\text{th})}$ temperature coefficient	$\Delta V_{GS(\text{th})}/T_J$	$I_D = 250 \mu\text{A}$	-	-8.1	-	
Gate-source threshold voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2	-	4	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 60 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$	-	-	10	
Drain-source on-state resistance ^a	$R_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$	-	0.00091	0.00115	Ω
		$V_{GS} = 7.5 \text{ V}$, $I_D = 20 \text{ A}$	-	0.00103	0.0013	
Forward transconductance ^a	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 45 \text{ A}$	-	140	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	7655	-	pF
Output capacitance	C_{oss}		-	1775	-	
Reverse transfer capacitance	C_{rss}		-	57	-	
Total gate charge	Q_g	$V_{DS} = 30 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$	-	108	162	nC
Gate-source charge	Q_{gs}	$V_{DS} = 30 \text{ V}$, $V_{GS} = 7.5 \text{ V}$, $I_D = 20 \text{ A}$	-	81	122	
Gate-drain charge	Q_{gd}		-	33	-	
Output charge	Q_{oss}		-	14	-	
Gate resistance	R_g	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0 \text{ V}$	-	111	-	Ω
Turn-on delay time	$t_{d(\text{on})}$	$f = 1 \text{ MHz}$ $V_{DD} = 30 \text{ V}$, $R_L = 3 \Omega$, $I_D \geq 10 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_g = 1 \Omega$	0.24	1.2	2.4	
Rise time	t_r		-	21	40	
Turn-off delay time	$t_{d(\text{off})}$		-	13	25	
Fall time	t_f		-	45	90	
Turn-on delay time	$t_{d(\text{on})}$		-	10	20	
Rise time	t_r		-	25	50	
Turn-off delay time	$t_{d(\text{off})}$		-	23	50	
Fall time	t_f		-	40	80	
			-	10	20	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25^\circ\text{C}$	-	-	218	A
Pulse diode forward current	I_{SM}		-	-	500	
Body diode voltage	V_{SD}	$I_S = 10 \text{ A}$, $V_{GS} = 0 \text{ V}$	-	0.70	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 10 \text{ A}$, $\text{di}/\text{dt} = 100 \text{ A}/\mu\text{s}$, $T_J = 25^\circ\text{C}$	-	70	140	ns
Body diode reverse recovery charge	Q_{rr}		-	132	260	
Reverse recovery fall time	t_a		-	42	-	ns
Reverse recovery rise time	t_b		-	28	-	

Notes

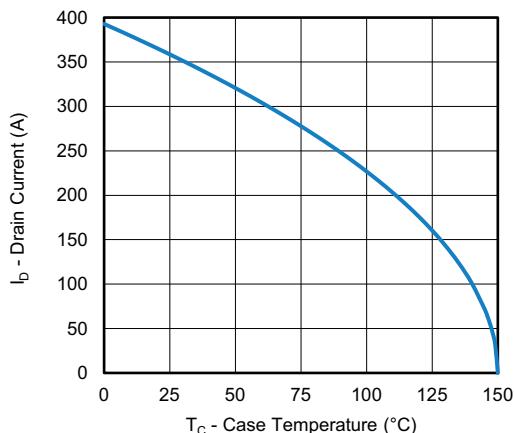
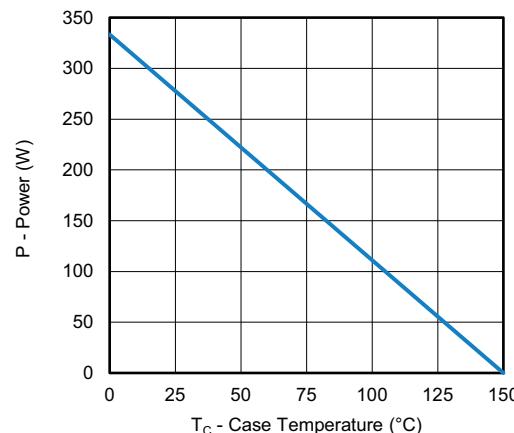
- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2 \%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

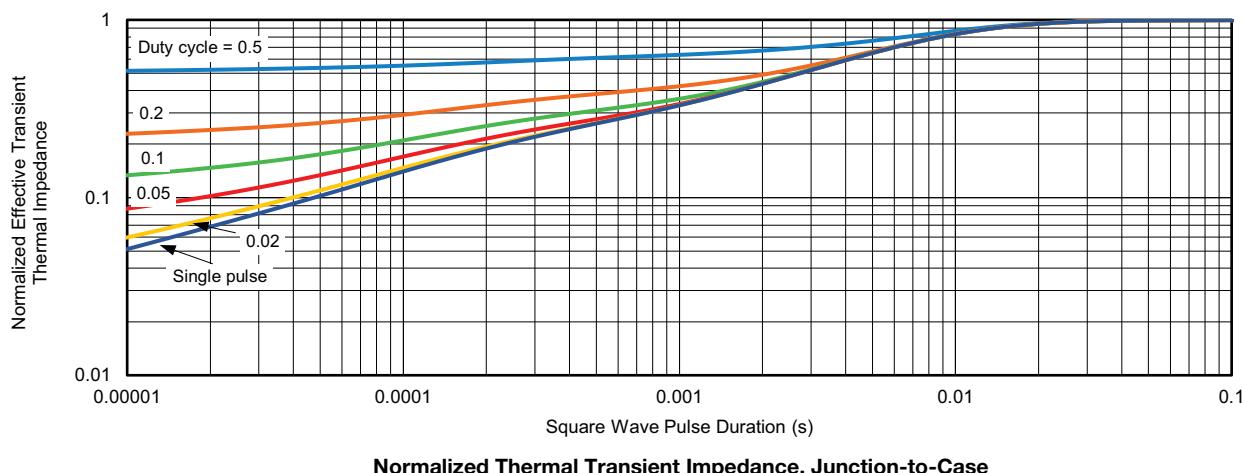
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Source-Drain Diode Forward Voltage

Threshold Voltage

On-Resistance vs. Gate-to-Source Voltage

Single Pulse Power, Junction-to-Case

Safe Operating Area, Junction-to-Case
Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

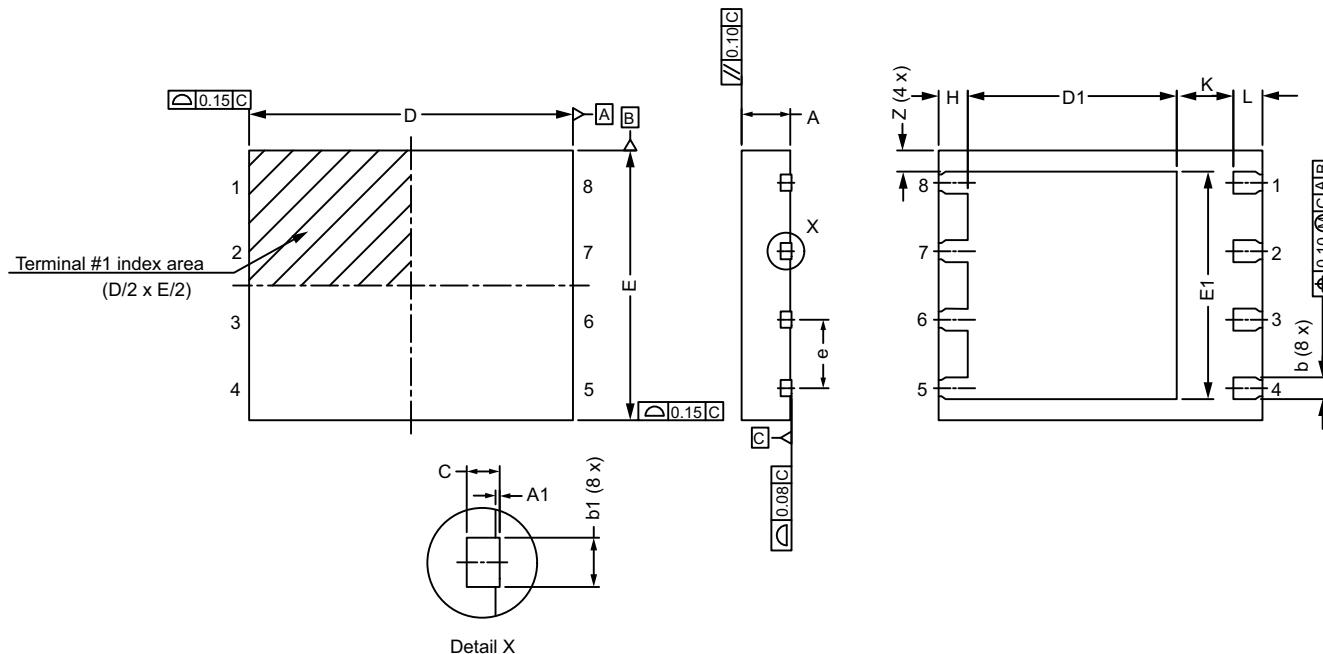
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62248.

PowerPAK® SO-8S BWL

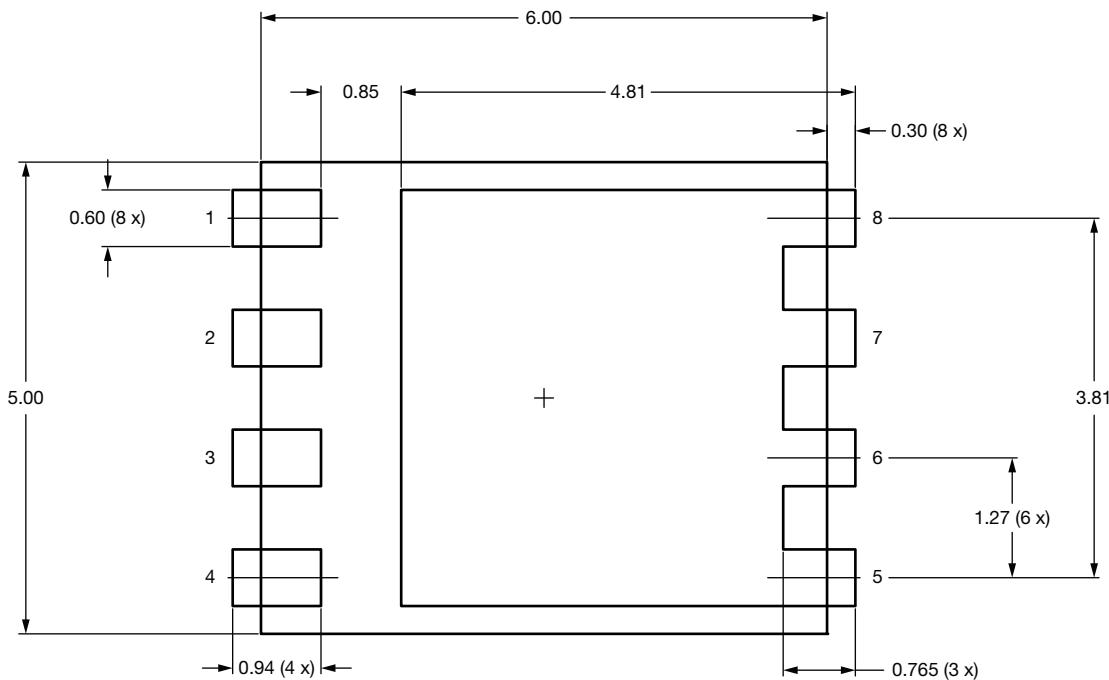
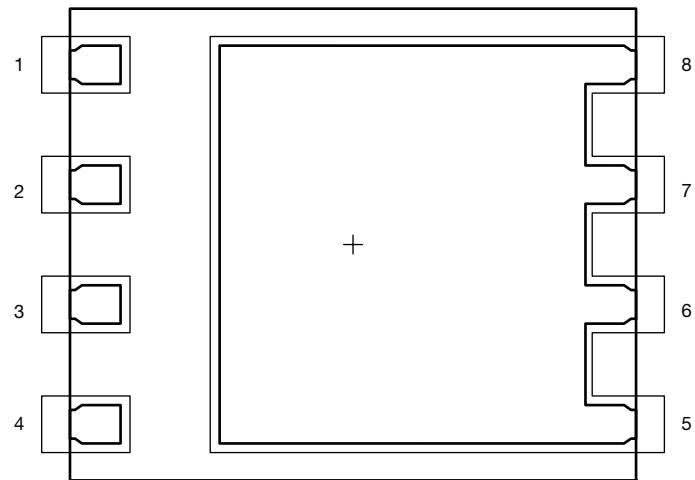


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.033	0.035	0.037
A1	-	-	0.05	-	-	0.002
b	0.31	0.41	0.51	0.012	0.016	0.020
b1	0.20	0.30	0.40	0.008	0.012	0.016
c	0.20 ref.			0.008 ref.		
D	5.90	6.00	6.10	0.232	0.236	0.240
D1	3.78	3.88	3.98	0.149	0.153	0.157
E	4.90	5.00	5.10	0.193	0.197	0.201
E1	4.12	4.22	4.32	0.162	0.166	0.170
e	1.27 BSC			0.050 BSC		
H	0.44	0.54	0.64	0.017	0.021	0.025
K	1.05 ref.			0.041 ref.		
L	0.44	0.54	0.64	0.017	0.021	0.025
Z	0.39 ref.			0.015 ref.		

ECN: C20-0936-Rev. A, 03-Aug-2020

DWG: 6082

Recommended Land Pattern PowerPAK® SO-8S BWL



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