

Data Sheet

Description

The ACPL-W60L/ACPL-K63L are optically coupled gates that combine a GaAsP light emitting diode and an integrated high gain photo detector. The output of the detector IC is an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 15 kV/ μ s at 3.3V.

This unique design provides maximum AC and DC circuit isolation while achieving LVTTTL/LVCMOS compatibility. The optocoupler AC and DC operational parameters are guaranteed from -40°C to $+100^{\circ}\text{C}$ allowing trouble-free system performance.

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

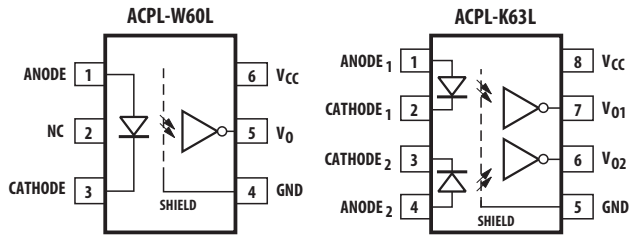
Features

- Dual Voltage Operation (3.3V/5V)
- Package clearance/creepage at 8 mm
- 15 kV/ μ s minimum Common Mode Rejection (CMR) at $V_{\text{CM}} = 1000\text{V}$
- High speed: 15 MBd typical
- LVTTTL/LVCMOS compatible
- Low input current capability: 5 mA
- Guaranteed AC and DC performance over temperature: -40°C to $+100^{\circ}\text{C}$
- Available in 6-pin stretched SO-6 and 8 pin stretched SO-8
- Safety approvals: UL, CSA, IEC/EN/DIN EN 60747-5-5

Applications

- Isolated line receiver
- Computer-peripheral interfaces
- Microprocessor system interfaces
- Digital isolation for A/D, D/A conversion
- Switching power supply
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement
- Field bus

Functional Diagram

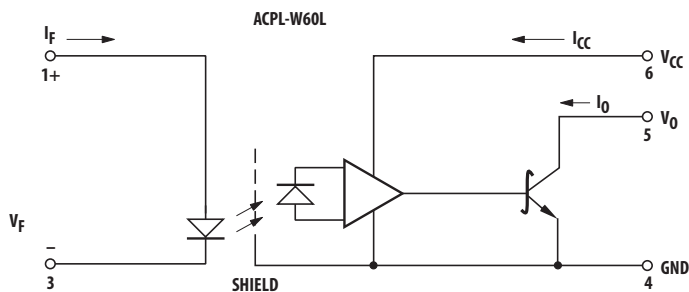


TRUTH TABLE
(POSITIVE LOGIC)

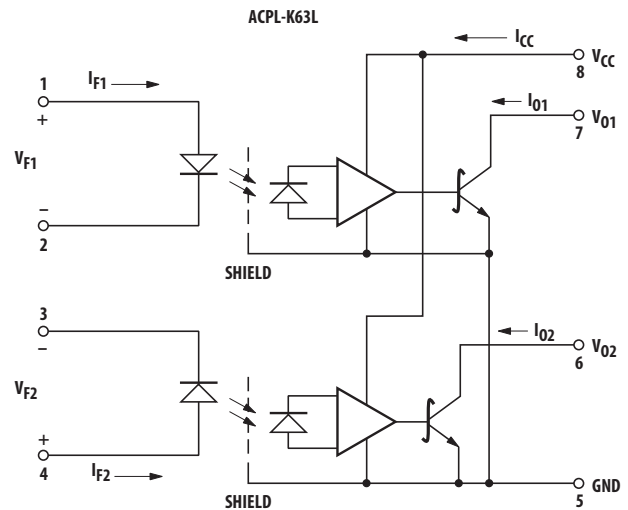
| LED | OUTPUT |
|-----|--------|
| ON | L |
| OFF | H |

A 0.1- μF bypass capacitor must be connected between pins 4 and 6 for ACPL-W60L, and pins 5 and 8 for ACPL-K63L.

Schematic Diagrams



Bypassing of the power supply line is required, with a 0.1- μF ceramic disc capacitor adjacent to each optocoupler. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.



These optocouplers are suitable for high-speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Ordering Information

ACPL-W60L/-K63L is UL Recognized with 5000 V_{rms} for 1 minute per UL1577 and is approved under CSA Component Acceptance Notice #5, File CA 88324.

| Part Number | Option | Package | Surface Mount | Tape and Reel | UL 5000 Vrms/ 1 Minute rating | IEC/EN/DIN EN 60747-5-5 | Quantity |
|-------------|-------------------|----------------|---------------|---------------|----------------------------------|----------------------------|---------------|
| | RoHS Compliant | | | | | | |
| ACPL-W60L | -000E | Stretched SO-6 | X | | X | | 100 per tube |
| | -500E | | X | X | X | | 1000 per reel |
| | -560E | | X | X | X | X | 1000 per reel |
| ACPL-K63L | -000E | Stretched SO-8 | X | | X | | 80 per tube |
| | -500E | | X | X | X | | 1000 per reel |
| | -560E | | X | X | X | X | 1000 per reel |

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

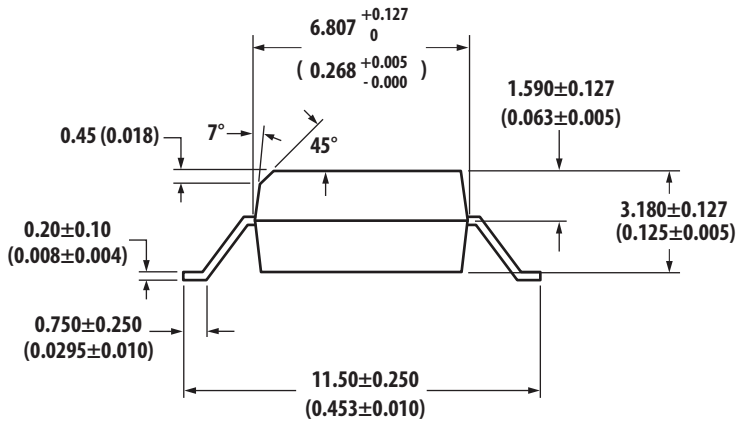
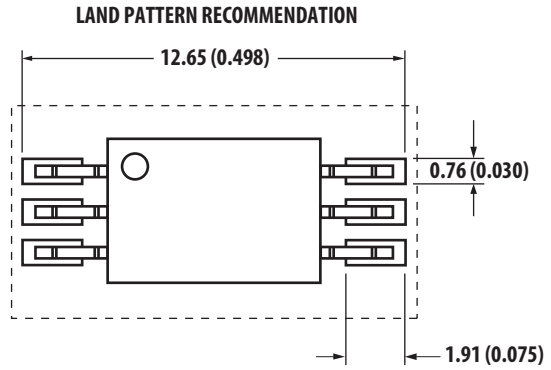
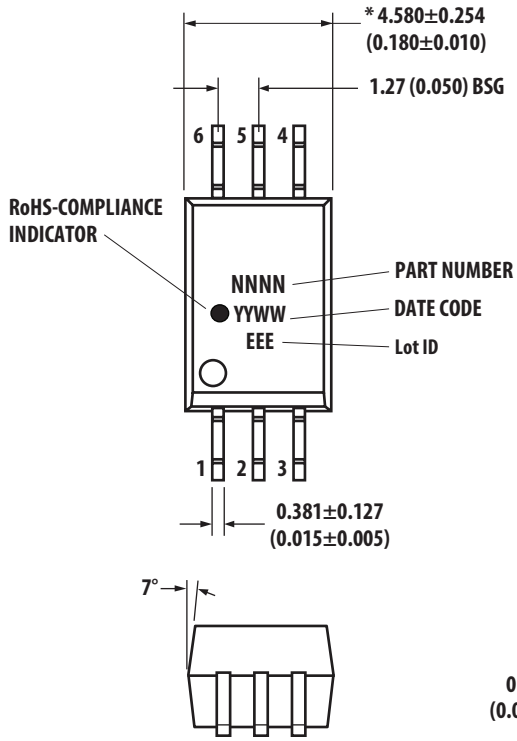
Example 1:

ACPL-W60L-560E to order product of Stretched SO-6 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

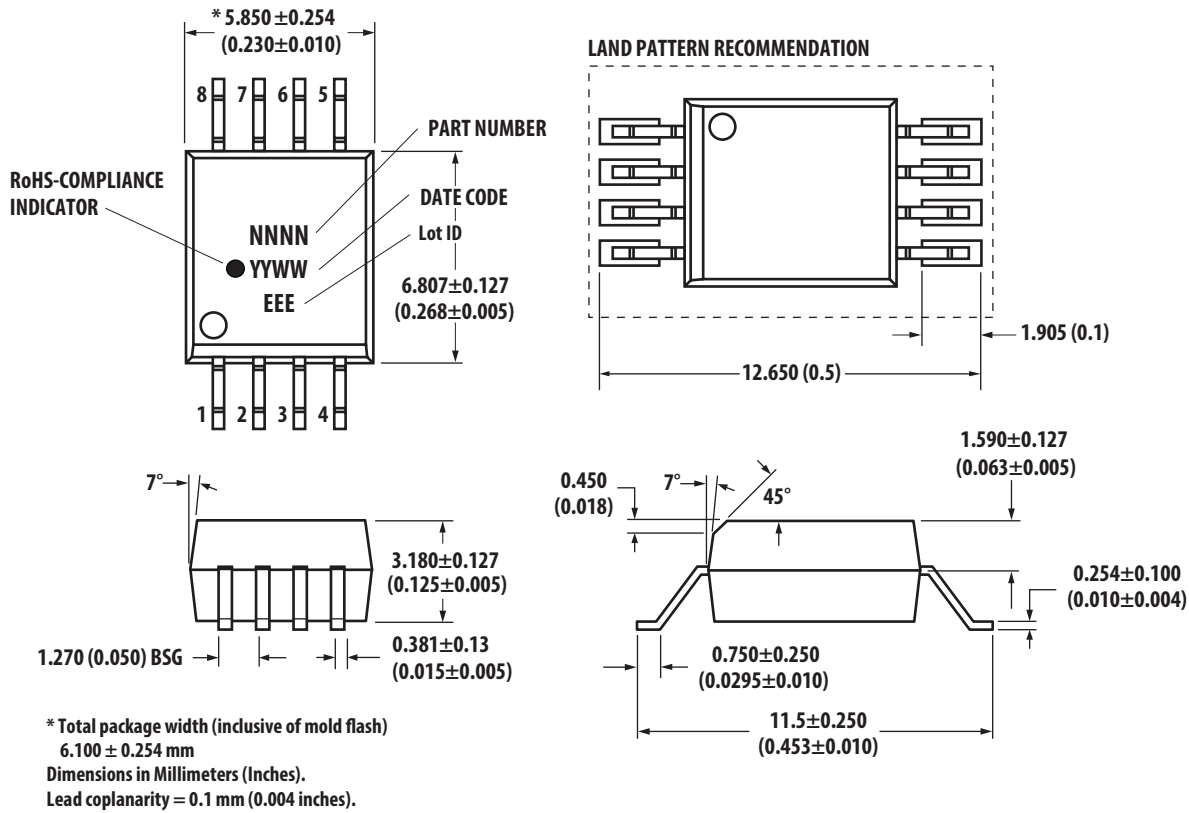
Package Outline Drawings

ACPL-W60L Stretched SO-6 Package



* Total package width (inclusive of mold flash)
 4.834 ± 0.254 mm
 Dimensions in Millimeters (Inches).
 Lead coplanarity = 0.1 mm (0.004 inches).

ACPL-K63L Stretched SO-8 Package



Recommended Solder Reflow Thermal Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

The ACPL-W60L/K63L have been approved by the following organizations.

| | |
|--------------------------------|---|
| UL | Approval under UL 1577, Component Recognition Program, File E55361. |
| CSA | Approval under CSA Component Acceptance Notice #5, File CA 88324. |
| IEC/EN/DIN EN 60747-5-5 | Approval/Pending Approval |

Insulation and Safety-Related Specifications

| Parameter | Symbol | ACPL-W60L/ K63L | Units | Conditions |
|---|---------|--------------------|-------|--|
| Minimum External Air Gap (External Clearance) | L (101) | 8 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (External Creepage) | L (102) | 8 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.08 | mm | Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity. |
| Tracking Resistance (Comparative Tracking Index) | CTI | 175 | Volts | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | IIIa | — | Material Group (DIN VDE 0110, 1/89, Table 1) |

IEC/EN/DIN EN 60747-5-5 Insulation-Related Characteristics (Option x60E)

| Description | Symbol | Characteristic ACPL-W60L ACPL-K63L | Units |
|---|----------------|--|-------------|
| Installation classification per DIN VDE 0110/39, Table 1 | | | |
| for rated mains voltage $\leq 150 V_{rms}$ | | I-IV | |
| for rated mains voltage $\leq 300 V_{rms}$ | | I-IV | |
| for rated mains voltage $\leq 600 V_{rms}$ | | I-III | |
| for rated mains voltage $\leq 1000 V_{rms}$ | | I-III | |
| Climatic Classification | | 55/100/21 | |
| Pollution Degree (DIN VDE 0110/39) | | 2 | |
| Maximum Working Insulation Voltage | V_{IORM} | 1140 | V_{peak} |
| Input to Output Test Voltage, Method b ^a $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1s$, Partial Discharge $< 5 pC$ | V_{PR} | 2137 | V_{peak} |
| Input-to-Output Test Voltage, Method a ^a $V_{IORM} \times 1.6 = V_{PR}$, Type and Sample Test, $t_m = 10s$, Partial Discharge $< 5 pC$ | V_{PR} | 1824 | V_{peak} |
| Highest Allowable Overvoltage (Transient Overvoltage, $t_{ini} = 60s$) | V_{IOTM} | 8000 | V_{peak} |
| Safety Limiting Values – maximum values allowed in the event of a failure | | | |
| Case Temperature | T_S | 175 | $^{\circ}C$ |
| Input Current | $I_{S,INPUT}$ | 230 | mA |
| Output Power | $P_{S,OUTPUT}$ | 600 | mW |
| Insulation Resistance at T_S , $V_{IO} = 500 V$ | R_S | $\geq 10^9$ | Ω |

- a. Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

NOTE These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety limit data shall be ensured by means of protective circuits.

Absolute Maximum Ratings (No Derating Required Up to 85°C)

| Parameter | Symbol | Device ^a | Min. | Max. | Units | Note |
|-----------------------------------|----------|---------------------|--|------|-------|------|
| Storage Temperature | T_S | | -55 | 125 | °C | |
| Operating Temperature† | T_A | | -40 | 100 | °C | |
| Average Forward Input Current | I_F | ACPL-W60L | — | 20 | mA | b |
| | | ACPL-K63L | — | 15 | | c, d |
| Reverse Input Voltage | V_R | | — | 5 | V | c |
| Input Power Dissipation | P_I | | — | 40 | mW | |
| Supply Voltage (1 Minute Maximum) | V_{CC} | | — | 7 | V | |
| Output Collector Current | I_O | | — | 50 | mA | c |
| Output Collector Voltage | V_O | | — | 7 | V | c |
| Output Power Dissipation | P_O | ACPL-W60L | — | 85 | mW | |
| | | ACPL-K63L | — | 60 | | c, e |
| Solder Reflow Temperature Profile | | | See Package Outline Drawings | | | |

- Ratings apply to all devices except otherwise noted in the Package column.
- Peaking circuits may produce transient input currents up to 50 mA, 50-ns maximum pulse width, provided average current does not exceed 20 mA.
- Each channel.
- Peaking circuits may produce transient input currents up to 50 mA, 50-ns maximum pulse width, provided average current does not exceed 15 mA.
- Derate linearly above +80°C free-air temperature at a rate of 2.7 mW/°C.

Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Units | Conditions |
|---|-----------------------|------|------|-----------|---|
| Input Current, Low Level | I_{FL} ^a | 0 | 250 | μA | |
| Input Current, High Level ^b | I_{FH} ^c | 5 | 15 | mA | $2.7V \leq V_{CC} \leq 3.6V$, $T_A = 85^\circ C$ to $100^\circ C$ |
| | | 6 | | mA | |
| Power Supply Voltage | V_{CC} | 2.7 | 3.6 | V | |
| | | 4.5 | 5.5 | V | |
| Operating Temperature | T_A | -40 | 100 | °C | |
| Fan Out (at $R_L = 1\text{ k}\Omega$) ^b | N | — | 5 | TTL Loads | |
| Output Pull-up Resistor | R_L | 330 | 4 k | Ω | |

- The off condition can also be guaranteed by ensuring that $V_{FL} \leq 0.8$ volts.
- Each channel.
- At $T_A = -40^\circ C$ to $85^\circ C$. The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.

Electrical Specifications

Over recommended operating conditions ($T_A = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $2.7\text{V} \leq V_{CC} \leq 3.6\text{V}$) unless otherwise specified.
All Typical at $V_{CC} = 3.3\text{V}$, $T_A = 25^\circ\text{C}$.

| Parameter | Symbol | Device | Min. | Typ. | Max. | Units | Test Conditions | Figure | Note |
|-------------------------------------|---------------------------|--------|------|------|------|----------------------------|--|--------|------|
| High Level Output Current | I_{OH} | | — | 4.5 | 50 | μA | $V_{CC} = 3.3\text{V}$, $V_O = 3.3\text{V}$, $I_F = 250 \mu\text{A}$ | 1, 2 | a |
| Input Threshold Current | I_{TH} | | — | 3.0 | 5.0 | mA | $T_A = -40^\circ\text{C}$ to 85°C , $V_{CC} = 3.3\text{V}$, $V_O = 0.6\text{V}$, I_{OL} (Sinking) = 13mA | 3, 4 | |
| | | | | | 6.0 | mA | $V_{CC} = 3.3\text{V}$, $V_O = 0.6\text{V}$, I_{OL} (Sinking) = 13mA | 3, 4 | |
| Low Level Output Voltage | V_{OL} | | — | 0.35 | 0.6 | V | $V_{CC} = 3.3\text{V}$, $I_F = 5\text{mA}$, I_{OL} (Sinking) = 13mA | 5, 6 | |
| High Level Supply Current | I_{CCH} | Single | — | 4.7 | 7.0 | mA | $I_F = 0\text{mA}$ | | |
| | | Dual | — | 6.9 | 10.0 | | $V_{CC} = 3.3\text{V}$ | | |
| Low Level Supply Current | I_{CCL} | Single | — | 7.0 | 10.0 | mA | $I_F = 10\text{mA}$ | | |
| | | Dual | — | 8.7 | 15.0 | | $V_{CC} = 3.3\text{V}$ | | |
| Input Forward Voltage | V_F | | 1.4 | 1.5 | 1.75 | V | $T_A = 25^\circ\text{C}$, $I_F = 10\text{mA}$ | 9 | a |
| Input Reverse Breakdown Voltage | B_{VR} | | 5 | — | — | V | $I_R = 10 \mu\text{A}$ | | a |
| Input Diode Temperature Coefficient | $\Delta V_F / \Delta T_A$ | | — | -1.6 | — | $\text{mV}/^\circ\text{C}$ | $I_F = 10\text{mA}$ | | a |
| Input Capacitance | C_{IN} | | — | 60 | — | pF | $f = 1\text{MHz}$, $V_F = 0\text{V}$ | | a |

a. Each channel.

Electrical Specifications (DC)

Over recommended operating conditions ($T_A = -40^\circ\text{C}$ to $+100^\circ\text{C}$, $4.5\text{V} \leq V_{DD} \leq 5.5\text{V}$) unless otherwise specified.
All typicals at $V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$.

| Parameter | Symbol | Device | Min. | Typ. | Max. | Units | Test Conditions | Figure | Note |
|-------------------------------------|---------------------------|--------|------|------|------|----------------------------|---|--------|------|
| High Level Output Current | I_{OH} | | — | 5.5 | 100 | μA | $V_{CC} = 5.5\text{V}$, $V_O = 5.5\text{V}$, $I_{FL} = 250 \mu\text{A}$ | 1, 2 | a |
| Input Threshold Current | I_{TH} | | — | 2.0 | 5.0 | mA | $V_{CC} = 5.5\text{V}$, $V_O = 0.6\text{V}$, $I_{OL} > 13\text{mA}$ | 3, 4 | |
| Low Level Output Voltage | V_{OL} | | — | 0.35 | 0.6 | V | $V_{CC} = 5.5\text{V}$, $I_F = 5\text{mA}$, $I_{OL(\text{Sinking})} = 13\text{mA}$ | 5, 6 | |
| High Level Supply Current | I_{CCH} | Single | — | 7.0 | 10.0 | mA | $V_{CC} = 5.5\text{V}$, $I_F = 0\text{mA}$ | | |
| | | Dual | — | 10.0 | 15.0 | mA | $V_{CC} = 5.5\text{V}$, $I_F = 0\text{mA}$ | | |
| Low Level Supply Current | I_{CCL} | Single | — | 9.0 | 13.0 | mA | $V_{CC} = 5.5\text{V}$, $I_F = 10\text{mA}$ | | |
| | | Dual | — | 13.0 | 21.0 | mA | $V_{CC} = 5.5\text{V}$, $I_F = 10\text{mA}$ | | |
| Input Forward Voltage | V_F | | 1.4 | 1.5 | 1.75 | V | $T_A = 25^\circ\text{C}$, $I_F = 10\text{mA}$ | 9 | a |
| | | | 1.3 | — | 1.8 | | | | |
| Input Reverse Breakdown Voltage | BV_R | | 5 | — | — | V | $I_R = 10 \mu\text{A}$ | | a |
| Input Diode Temperature Coefficient | $\Delta V_F / \Delta T_A$ | | — | -1.6 | — | $\text{mV}/^\circ\text{C}$ | $I_F = 10\text{mA}$ | | a |
| Input Capacitance | C_{IN} | | — | 60 | — | pF | $f = 1\text{MHz}$, $V_F = 0\text{V}$ | | a |

a. Each channel.

Switching Specifications

Over recommended temperature ($T_A = -40^\circ\text{C}$ to $+100^\circ\text{C}$), $V_{CC} = 3.3\text{V}$, $I_F = 7.5\text{ mA}$ unless otherwise specified.
All Typical at $T_A = 25^\circ\text{C}$, $V_{CC} = 3.3\text{V}$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Figure | Note |
|---|-----------------------|------|------|------|-------|--|--------------------|------|
| Propagation Delay Time to High Output Level | t_{PLH} | — | — | 90 | ns | $T_A = -40^\circ\text{C}$ to 85°C , $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | 10, 11, 12, 13, 14 | a, b |
| | | — | — | 95 | ns | $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | | |
| Propagation Delay Time to Low Output Level | t_{PHL} | — | — | 75 | ns | $T_A = -40^\circ\text{C}$ to 85°C , $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | | a, c |
| | | — | — | 90 | ns | $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | | |
| Pulse Width Distortion | $ t_{PHL} - t_{PLH} $ | — | — | 25 | ns | $T_A = -40^\circ\text{C}$ to 85°C , $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | 13, 14 | d |
| | | — | — | 30 | ns | $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | | |
| Propagation Delay Skew | t_{PSK} | — | — | 40 | ns | | | d, e |
| Output Rise Time (10–90%) | t_r | — | 45 | — | ns | | | a |
| Output Fall Time (90–10%) | t_f | — | 20 | — | ns | | | a |

- Each channel.
- The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5-V point on the rising edge of the output pulse.
- The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5-V point on the falling edge of the output pulse.
- See test circuit for measurement details.
- t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.

Switching Specifications (AC)

Over recommended temperature ($T_A = -40^\circ\text{C}$ to $+100^\circ\text{C}$), $V_{CC} = 5\text{V}$, $I_F = 7.5\text{ mA}$ unless otherwise specified.
All Typical at $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V}$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Figure | Note |
|---|-----------------------|------|------|------|-------|---|--------------------|------|
| Propagation Delay Time to High Output Level | t_{PLH} | 20 | 48 | 75 | ns | $T_A = 25^\circ\text{C}$, $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | 10, 11, 12, 13, 14 | a, b |
| | | — | — | 100 | ns | $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | | |
| Propagation Delay Time to Low Output Level | t_{PHL} | 25 | 50 | 75 | ns | $T_A = 25^\circ\text{C}$, $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | | a, c |
| | | — | — | 100 | ns | $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | | |
| Pulse Width Distortion | $ t_{PHL} - t_{PLH} $ | — | 3.5 | 35 | ns | $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | 13, 14 | d |
| Propagation Delay Skew | t_{psk} | — | — | 40 | ns | $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | | d, e |
| Output Rise Time (10%-90%) | t_r | — | 24 | — | ns | $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | | a |
| Output Fall Time (10%-90%) | t_f | — | 10 | — | ns | $R_L = 350\Omega$, $C_L = 15\text{ pF}$ | | a |

- Each channel.
- The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5-V point on the rising edge of the output pulse.
- The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5-V point on the falling edge of the output pulse.
- See test circuit for measurement details.
- t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.

| Parameter | Symbol | Min. | Typ. | Units | Test Conditions | Figure | Note |
|--|----------|------|------|-------------|--|--------|------|
| Output High Level Common Mode Transient Immunity | $ CM_H $ | 15 | 25 | kV/ μ s | $V_{CC} = 3.3V, I_F = 0 \text{ mA}, V_{O(MIN)} = 2V, R_L = 350\Omega, T_A = 25^\circ\text{C}, V_{CM} = 1000V$ and $V_{CM} = 10V$ | 15 | a, b |
| Output Low Level Common Mode Transient Immunity | $ CM_L $ | 15 | 25 | kV/ μ s | $V_{CC} = 3.3V, I_F = 7.5 \text{ mA}, V_{O(MAX)} = 0.8V, R_L = 350\Omega, T_A = 25^\circ\text{C}, V_{CM} = 1000V$ and $V_{CM} = 10V$ | 15 | a, b |
| Output High Level Common Mode Transient Immunity | $ CM_H $ | 10 | 15 | kV/ μ s | $V_{CC} = 5V, I_F = 0 \text{ mA}, V_{O(MIN)} = 2V, R_L = 350\Omega, T_A = 25^\circ\text{C}, V_{CM} = 1000V$ | 15 | a, b |
| Output Low Level Common Mode Transient Immunity | $ CM_L $ | 10 | 15 | kV/ μ s | $V_{CC} = 5V, I_F = 7.5 \text{ mA}, V_{O(MAX)} = 0.8V, R_L = 350\Omega, T_A = 25^\circ\text{C}, V_{CM} = 1000V$ | 15 | c, b |

- a. CM_H is the maximum tolerable rate of rise on the common mode voltage to assure that the output will remain in a high logic state (that is, $V_o > 2.0V$).
- b. For sinusoidal voltages, $(|dV_{CM}| / dt)_{max} = \pi f_{CM} V_{CM} (p-p)$.
- c. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (that is, $V_o < 0.8V$).

Package Characteristics

All Typicals at $T_A = 25^\circ\text{C}$.

| Parameter | Symbol | Package | Min. | Typ. | Max | Units | Test Conditions | Figure | Note |
|---|-------------|----------------------|------|-----------|-----|---------------|---|---------------------|---------|
| Input-Output Insulation | I_{I-O}^a | Single | — | — | 1 | μA | 45% RH, $t = 5s, V_{I-O} = 3 \text{ kV DC}, T_A = 25^\circ\text{C}$ | | b, c |
| Input-Output Momentary Withstand Voltage ^a | V_{ISO} | Single, Dual Channel | 5000 | | — | Vrms | RH \leq 50%, $t = 1 \text{ min}, T_A = 25^\circ\text{C}$ | | b, c |
| Input-Output Resistance | R_{I-O} | Single, Dual Channel | — | 10^{12} | — | Ω | $V_{I-O} = 500 \text{ V}_{dc}$ | | b, d, e |
| Input-Output Capacitance | C_{I-O} | Single, Dual Channel | — | 0.5 | — | pF | $f = 1 \text{ MHz}, T_A = 25^\circ\text{C}$ | | b, d, e |
| Input-Input Insulation Leakage Current | I_{I-I} | Dual Channel | — | 0.005 | — | μA | RH \leq 45%, $t = 5s, V_{I-I} = 500V$ | | f |
| Resistance (Input-Input) | R_{I-I} | Dual Channel | — | 10^{11} | — | Ω | | | f |
| Capacitance (Input-Input) | C_{I-I} | Dual Channel | — | 0.25 | — | pG | | $f = 1 \text{ MHz}$ | f |

- a. The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable), your equipment level safety specification or Broadcom Application Note 1074 entitled *Optocoupler Input-Output Endurance Voltage*.
- b. Single channel device is considered a two-terminal part when pins 1, 2, 3 are shorted together, and pins 4, 5, 6 shorted together separately. Dual channel device is considered a two-terminal part when pins 1, 2, 3, 4 are shorted together, and pins 5, 6, 7, 8 are shorted together separately.
- c. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $\geq 6000 V_{rms}$ for one second (leakage detection current limit, $I_{I-O} \leq 5 \mu\text{A}$). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.
- d. Each channel.
- e. Measured between the LED anode and cathode shorted together and pins 5 through 8 shorted together. For dual channel products only.
- f. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together. For dual channel products only.

Figure 1 Typical High Level Output Current vs. Temperature, $V_{CC} = 3.3V$

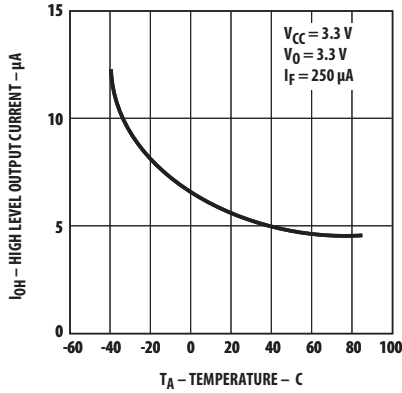


Figure 2 Typical High Level Output Current vs. Temperature, $V_{CC} = 5V$

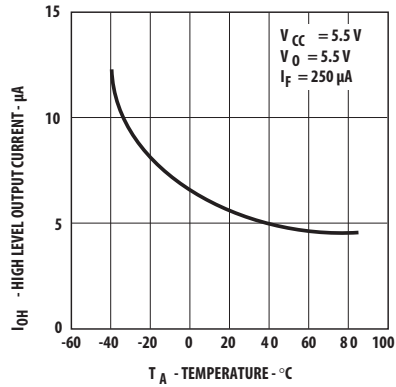


Figure 3 Typical Input Threshold Current vs Temperature, $V_{CC} = 3.3V$

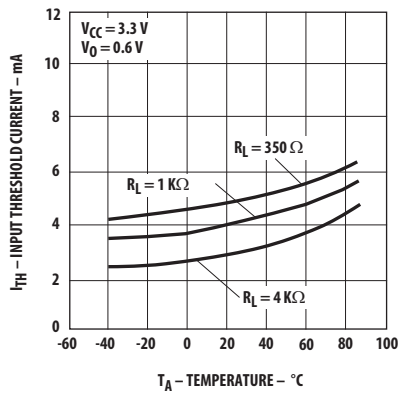


Figure 4 Typical Input Threshold Current vs Temperature, $V_{CC} = 5V$

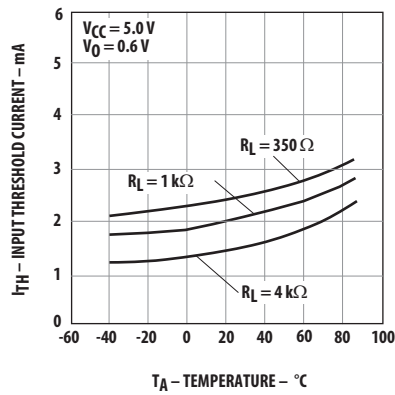


Figure 5 Typical Low Level Output Voltage vs. Temperature, $V_{CC} = 3.3V$

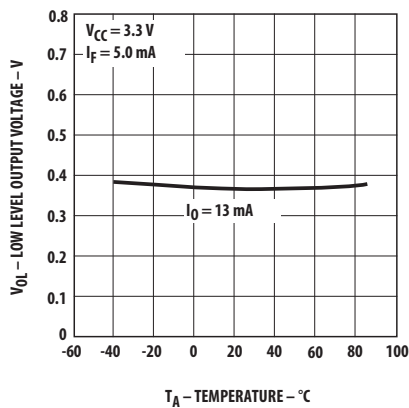


Figure 6 Typical Low Level Output Voltage vs. Temperature, $V_{CC} = 5V$

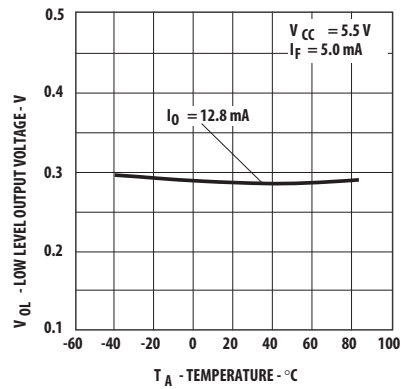


Figure 7 Typical Low Level Output Current vs. Temperature, $V_{CC} = 3.3V$

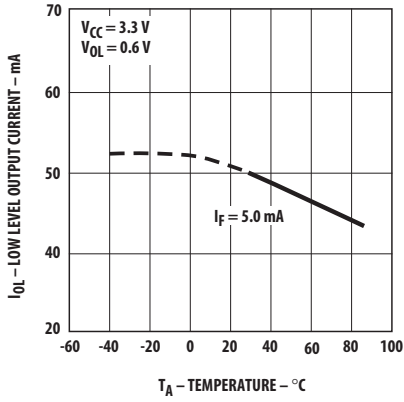


Figure 8 Typical Low Level Output Current vs. Temperature, $V_{CC} = 5V$

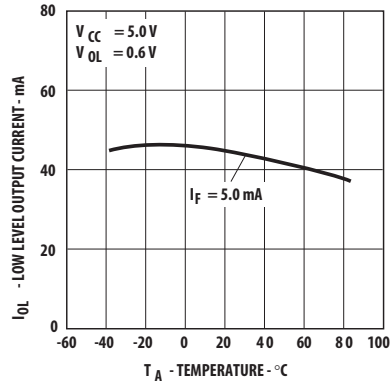


Figure 9 Typical Input Diode Forward Characteristic

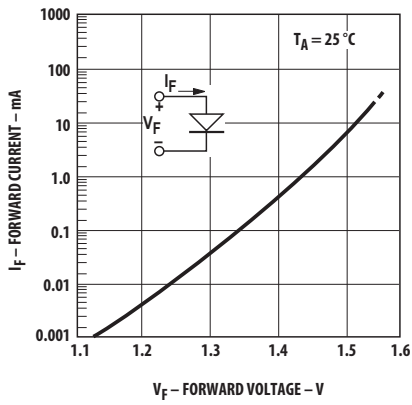
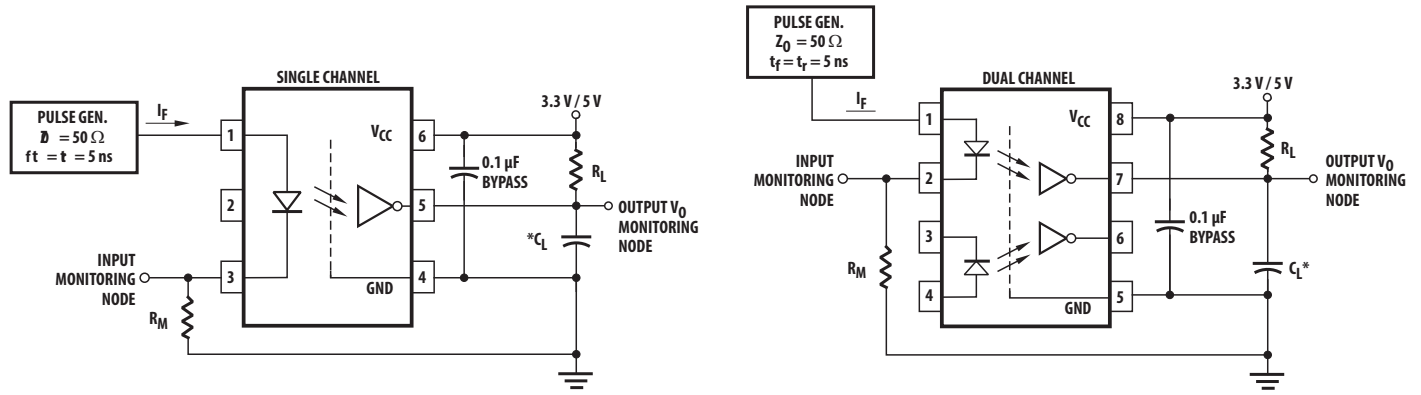


Figure 10 Test Circuit for t_{PHL} and t_{PLH}



* C_L IS APPROXIMATELY 15 pF WHICH INCLUDES PROBE AND STRAY WIRING CAPACITANCE.

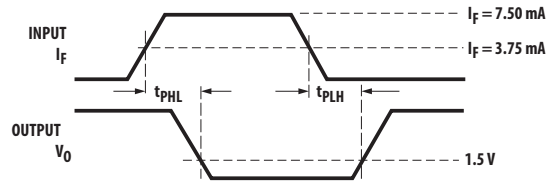


Figure 11 Typical Propagation Delay vs. Temperature $V_{CC} = 3.3V$

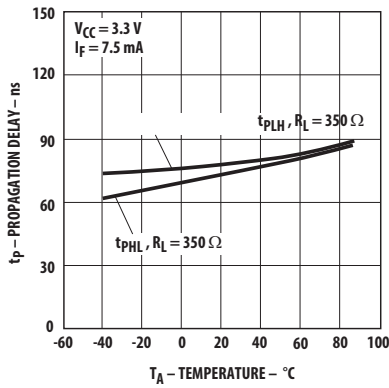


Figure 12 Typical Propagation Delay vs. Temperature $V_{CC} = 5V$

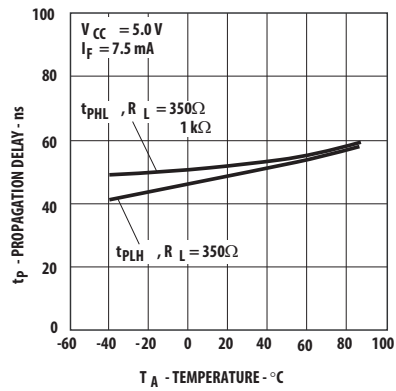


Figure 13 Typical Pulse Width Distortion vs. Temperature, $V_{CC} = 3.3V$

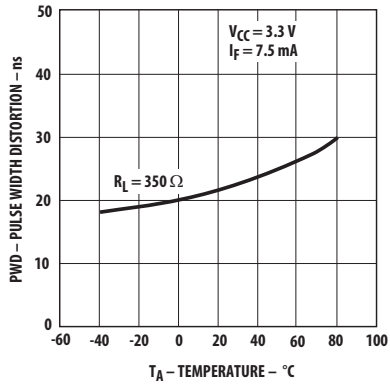


Figure 14 Typical Pulse Width Distortion vs. Temperature, $V_{CC} = 5V$

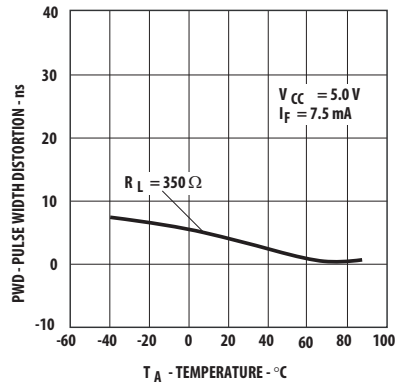
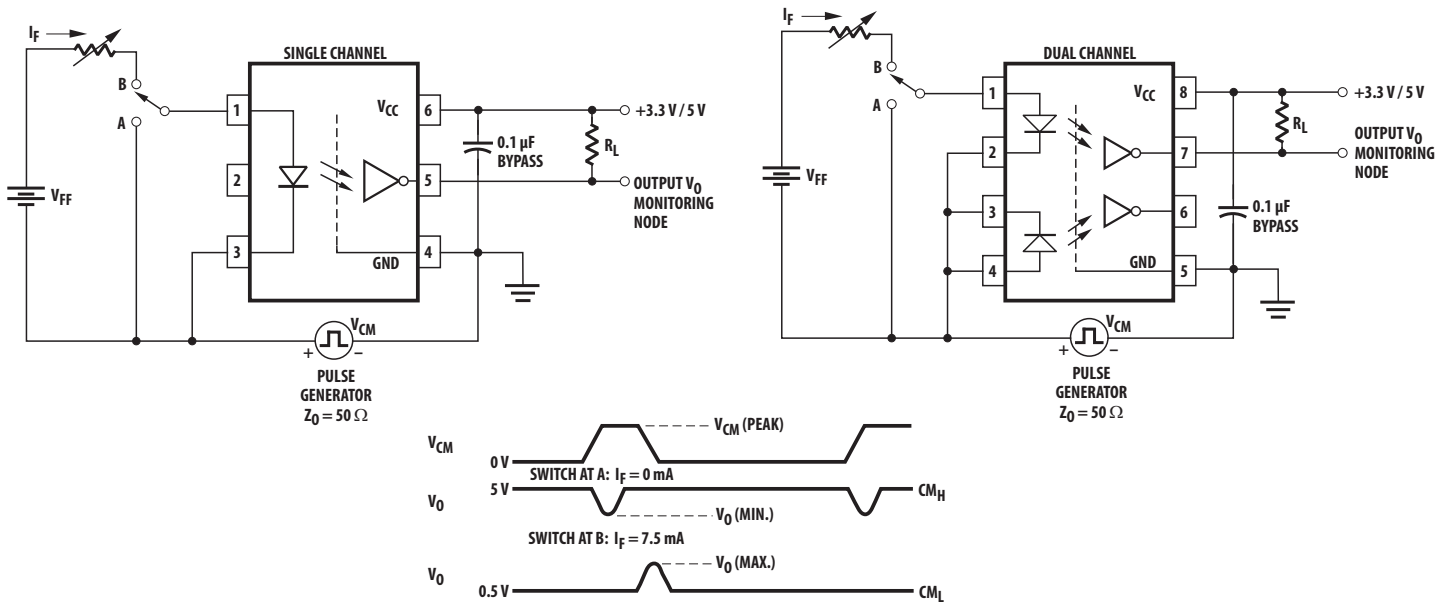


Figure 15 Test Circuit for Common Mode Transient Immunity and Typical Waveforms



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