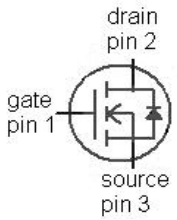
OptiMOS™ 5 Power-Transistor

Features

- N-channel, normal level
- Optimized for FOM_{OSS}
- Very low on-resistance $R_{DS(on)}$
- 175 °C operating temperature
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[1] for target application
- Ideal for high-frequency switching and synchronous rectification

Product Summary

V_{DS}	100	V
$R_{DS(on),max}$	2.0	mΩ
I_D	176	A



RoHS

Halogen-Free

Type	IPB020N10N5
	
Package	PG-TO263-3
Marking	020N10N5

Maximum ratings, at T_A=25 °C, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	T_C=25 °C	176	A
		T_C=100 °C	135	
Pulsed drain current[2]	$I_{D,pulse}$	T_C=25 °C	704	
Avalanche energy, single pulse	E_{AS}	I_D=50 A, R_{GS}=25 Ω	1166	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25 °C	375	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

[1] J-STD20 and JESD22

[2] see Diagram 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - case	R_{thJC}		-	0.3	0.4	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint	-	-	62	
		6 cm^2 cooling area[4)]	-	-	40	
Soldering temperature, wave and reflow soldering are allowed	T_{sold}	reflow MSL1			260	°C
Electrical characteristics, at T_j=25 °C, unless otherwise specified						
Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0 V, I_D=1 mA	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=270 µA	2.2	3	3.8	
Zero gate voltage drain current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V, T_j=25 °C	-	0.1	7	µA
		V_{DS}=100 V, V_{GS}=0 V, T_j=125 °C	-	10	100	
Gate-source leakage current	I_{GSS}	V_{GS}=20 V, V_{DS}=0 V	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10 V, I_D=100 A	-	1.7	2.0	mΩ
		V_{GS}=6 V, I_D=50 A	-	2.0	2.5	
Gate resistance[5)]	R_G		-	1.3	2	Ω
Transconductance	g_{fs}	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=100 A	124	248	-	S

[4)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

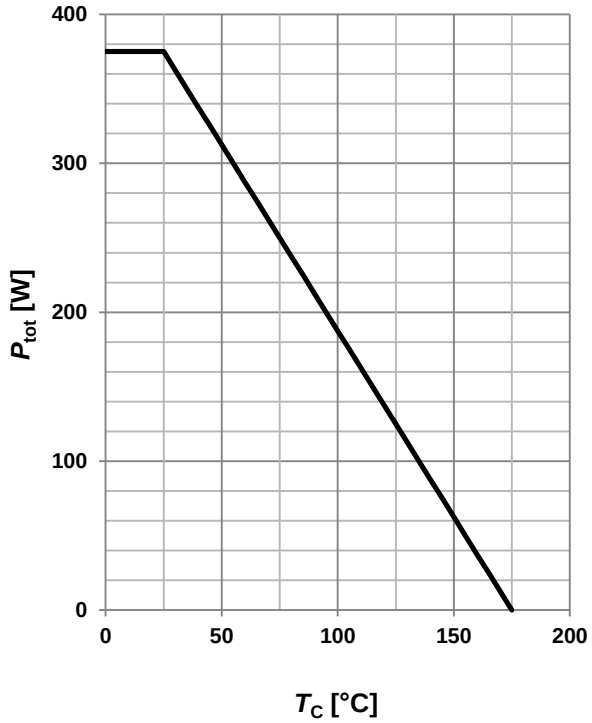
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[5]						
Input capacitance	C_{iss}	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz	-	12000	15600	pF
Output capacitance	C_{oss}		-	1810	2353	
Reverse transfer capacitance	C_{rss}		-	80	140	
Turn-on delay time	$t_{d(on)}$	V_{DD}=50 V, V_{GS}=10 V, I_D=100 A, $R_{G,ext}$=1.6 Ω	-	33	-	ns
Rise time	t_r		-	26	-	
Turn-off delay time	$t_{d(off)}$		-	77	-	
Fall time	t_f		-	29	-	
Gate Charge Characteristics[6]						
Gate to source charge	Q_{gs}	V_{DD}=50 V, I_D=100 A, V_{GS}=0 to 10 V	-	54	-	nC
Gate to drain charge[5]	Q_{gd}		-	34	51	
Switching charge	Q_{sw}		-	52	-	
Gate charge total[5]	Q_g		-	168	210	
Gate plateau voltage	$V_{plateau}$		-	4.5	-	V
Output charge[5]	Q_{oss}	V_{DD}=50 V, V_{GS}=0 V	-	213	283	nC
Reverse Diode						
Diode continous forward current	I_S	T_C=25 °C	-	-	176	A
Diode pulse current	$I_{S,pulse}$		-	-	480	
Diode forward voltage	V_{SD}	V_{GS}=0 V, I_F=100 A, T_j=25 °C	-	0.9	1.2	V
Reverse recovery time[5]	t_{rr}	V_R=50 V, I_F=I_S, di_F/dt=100 A/µs	-	99	198	ns
Reverse recovery charge[5]	Q_{rr}		-	287	574	nC

[5] Defined by design. Not subject to production test

[6] See figure 16 for gate charge parameter definition

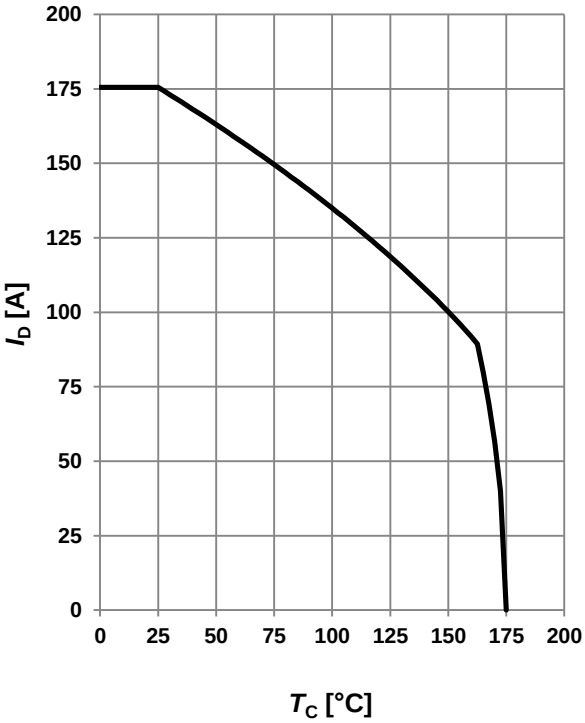
1 Power dissipation

$P_{tot}=f(T_C)$



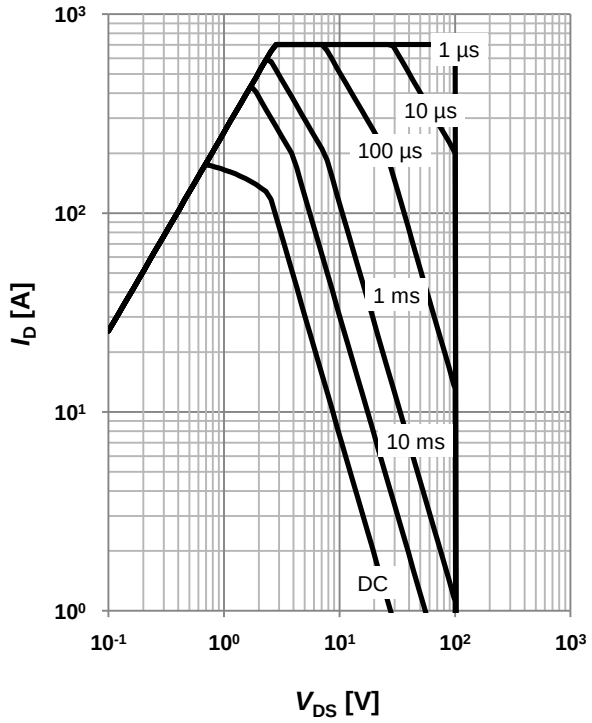
2 Drain current

$I_D=f(T_C)$; $V_{GS}\geq 10$ V



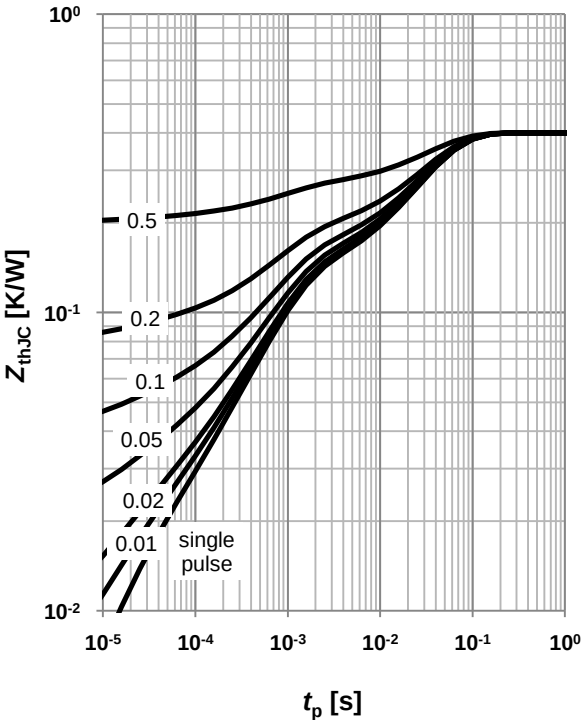
3 Safe operating area

$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$
parameter: t_p



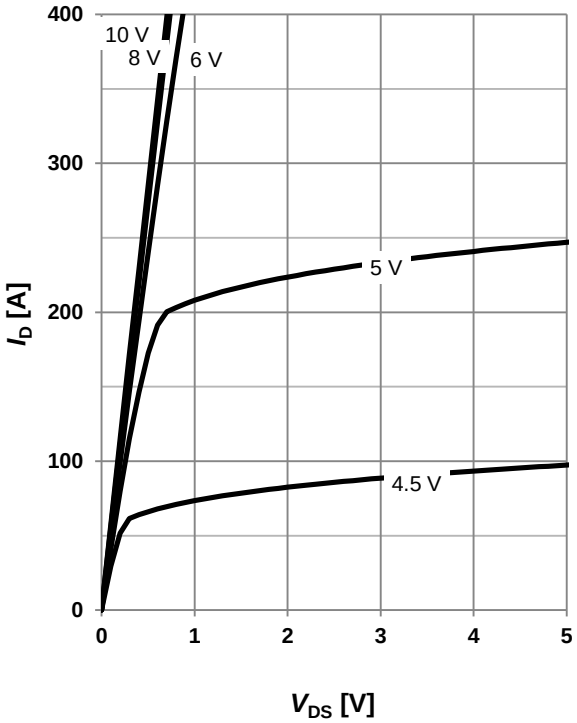
4 Max. transient thermal impedance

$Z_{thJC}=f(t_p)$
parameter: $D=t_p/T$



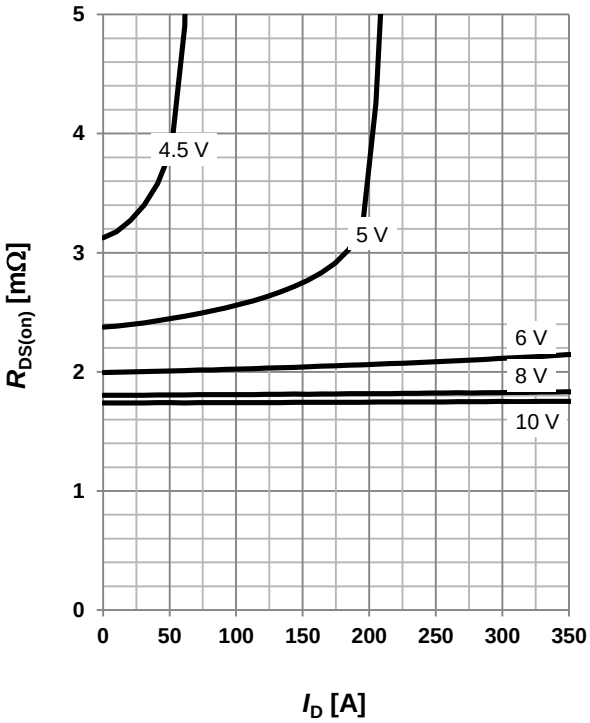
5 Typ. output characteristics

I_D=f(V_{DS}); T_j=25 °C
parameter: V_{GS}



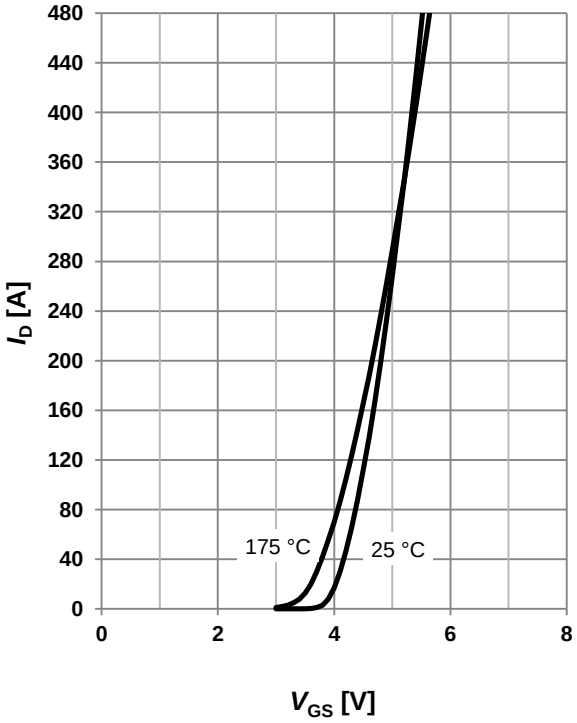
6 Typ. drain-source on resistance

$R_{DS(on)}$=f(I_D); T_j=25 °C
parameter: V_{GS}



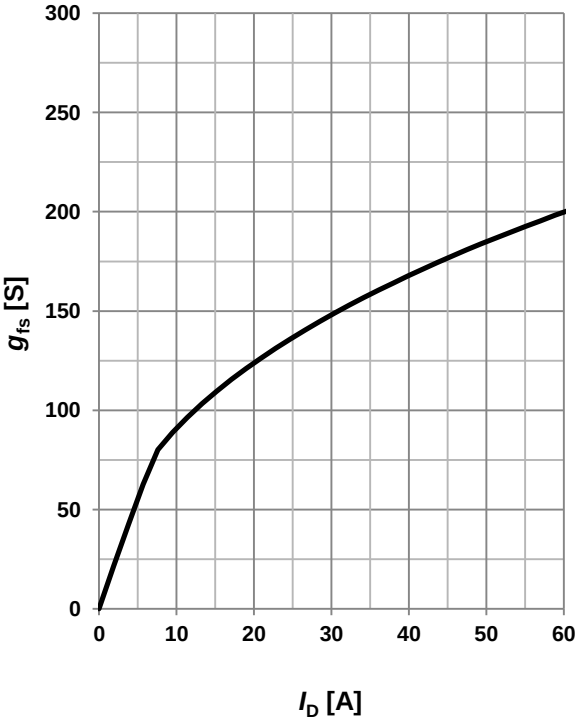
7 Typ. transfer characteristics

I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$
parameter: T_j



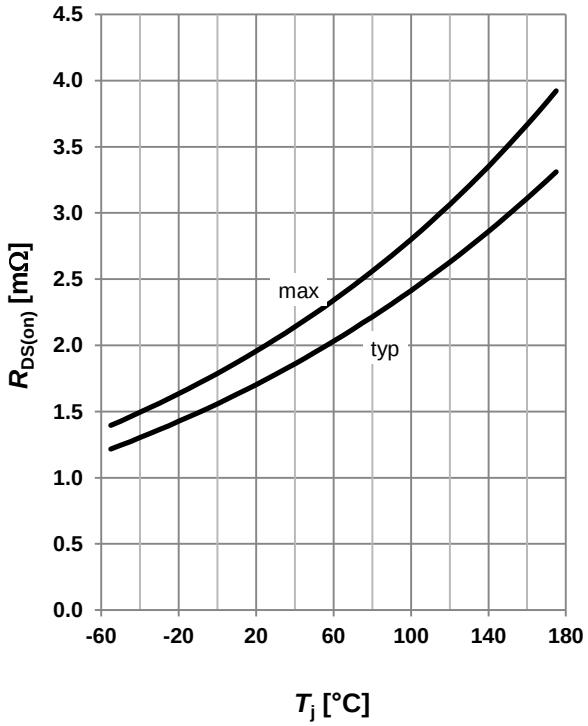
8 Typ. forward transconductance

g_{fs}=f(I_D); T_j=25 °C



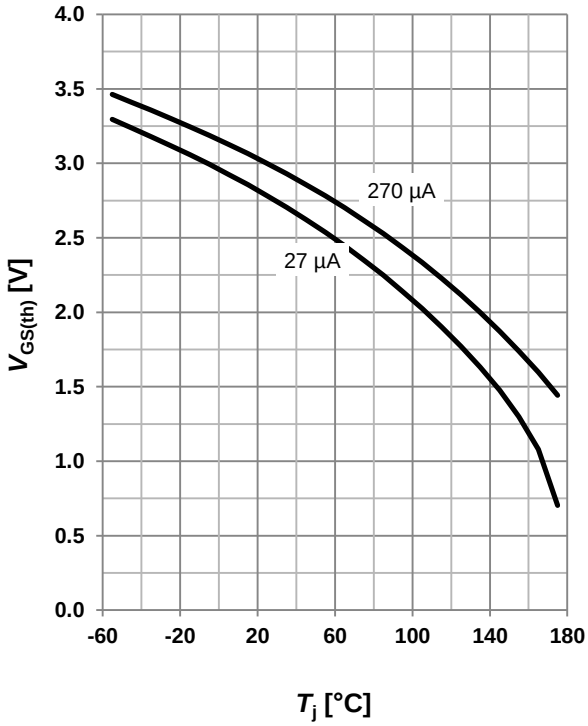
9 Drain-source on-state resistance

$R_{DS(on)}$=f(T_j); I_D=100 A; V_{GS}=10 V



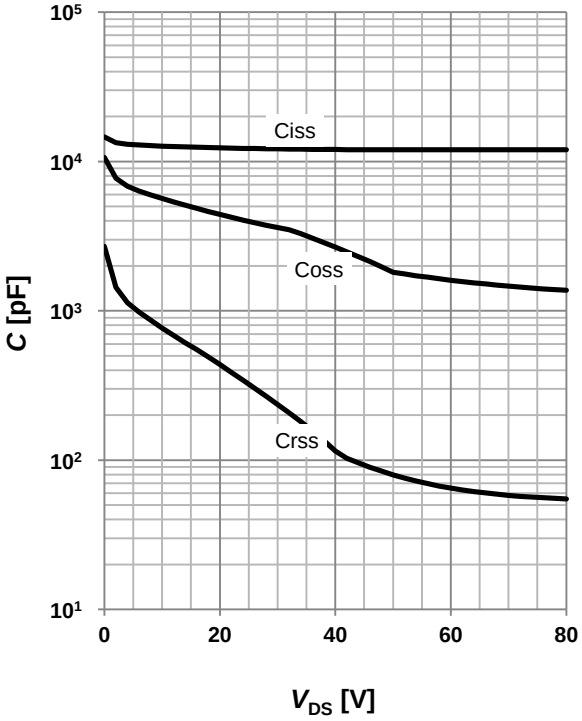
10 Typ. gate threshold voltage

$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}
parameter: I_D



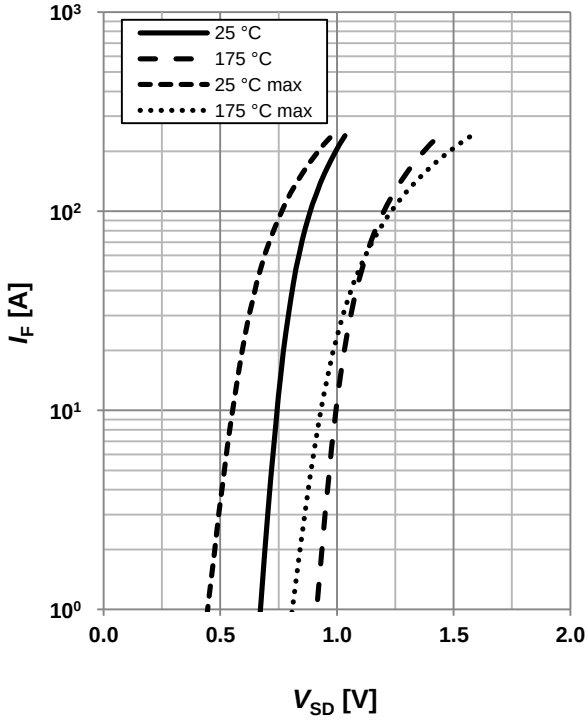
11 Typ. capacitances

C=f(V_{DS}); V_{GS}=0 V; f=1 MHz



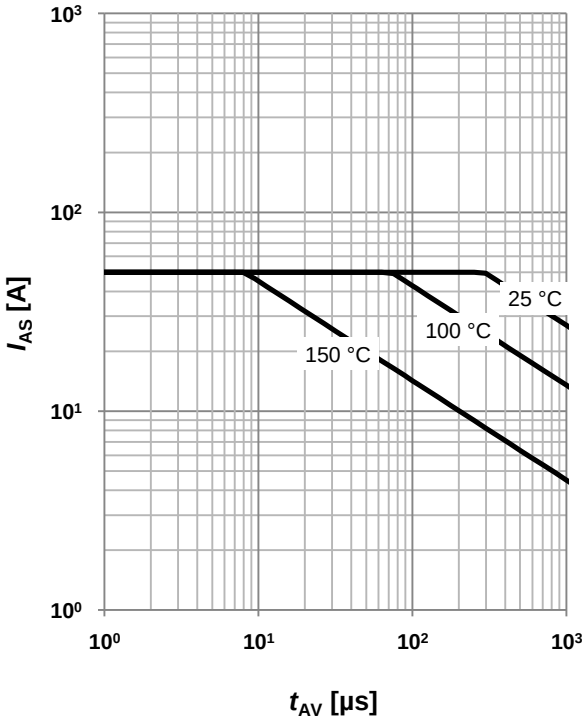
12 Forward characteristics of reverse diode

I_F=f(V_{SD})
parameter: T_j



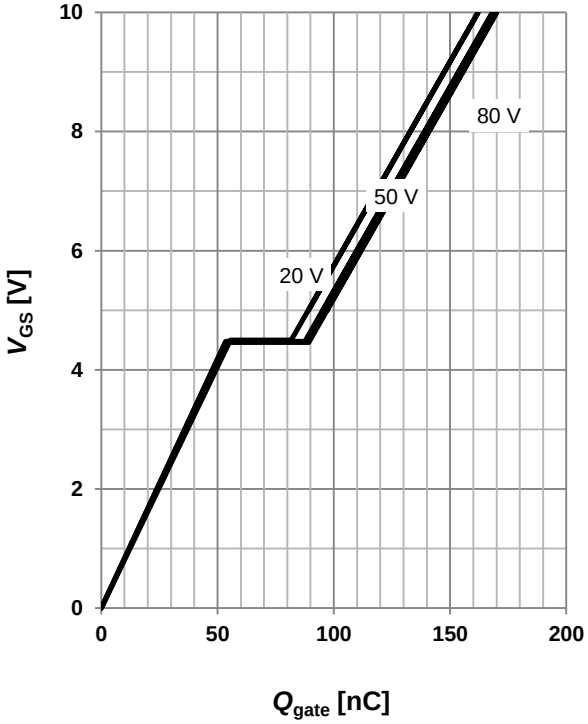
13 Avalanche characteristics

I_{AS}=f(t_{AV}); R_{GS}=25 Ω
parameter: $T_{j(start)}$



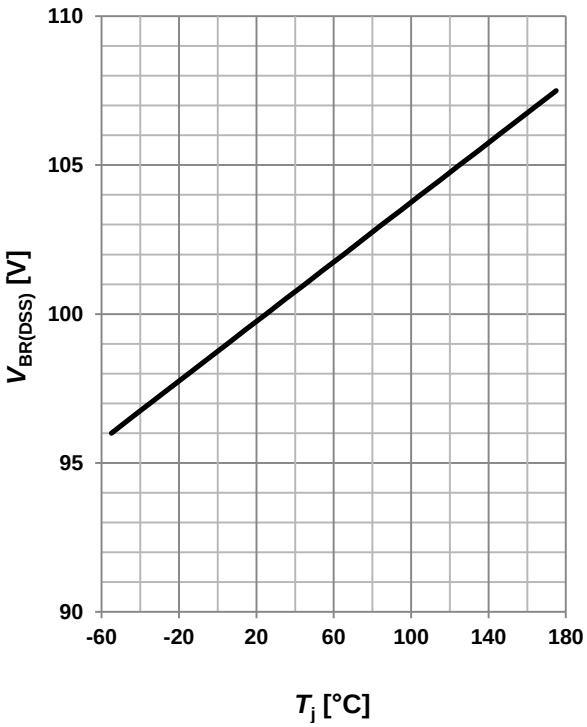
14 Typ. gate charge

V_{GS}=f(Q_{gate}); I_D=100 A pulsed
parameter: V_{DD}

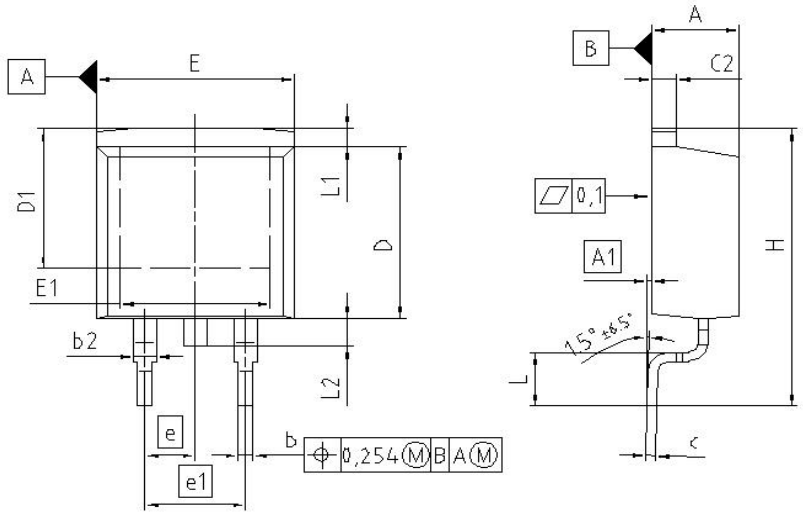


15 Drain-source breakdown voltage

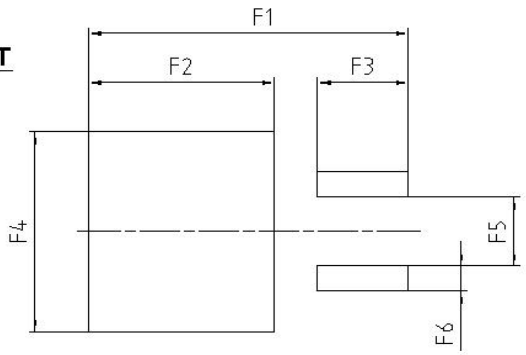
$V_{BR(DSS)}$=f(T_j); I_D=1 mA



PG-TO-263 (D²-Pak)



FOOTPRINT



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	0.000	0.254	0.000	0.010
b	0.650	0.850	0.026	0.033
b2	0.950	1.321	0.037	0.052
c	0.330	0.650	0.013	0.026
c2	0.170	1.400	0.046	0.055
D	8.509	9.450	0.335	0.372
D1	7.100	-	0.280	-
E	9.800	10.312	0.386	0.406
E1	6.500		0.256	
e	2.540		0.100	
e1	5.080		0.200	
N	2		2	
H	14.605	15.875	0.575	0.625
L	2.200	3.000	0.087	0.118
L1	-	1.600	-	0.063
L2	1.000	1.778	0.039	0.070
F1	16.050	16.250	0.632	0.640
F2	9.300	9.500	0.366	0.374
F3	4.500	4.700	0.177	0.185
F4	10.700	10.900	0.421	0.429
F5	3.630	3.830	0.143	0.151
F6	1.100	1.300	0.043	0.051

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EUROPEAN PROJECTION	
ISSUE DATE	12-02-2006
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