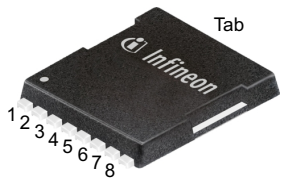
MOSFET

OptiMOS™ 5 Linear FET, 60 V

TOLL



Features

- Ideal for hot-swap and e-fuse applications
- Very low on-resistance $R_{DS(on)}$
- Wide safe operating area SOA
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

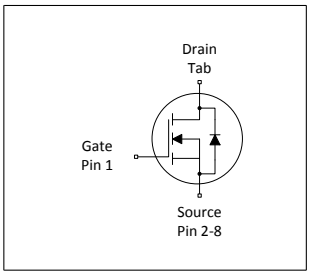


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	0.8	mΩ
I_D	454	A
I_{pulse} (V_{DS}=30 V, t_p=10 ms)	16	A

Type / Ordering Code	Package	Marking	Related Links
IPT008N06NM5LF	PG-HSOF-8	008N06LF	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	454 287 48	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10V, T_A=25°C, R_{thJA}=40°C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	1816	A	T_C=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	909	mJ	I_D=150 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	278 3.1	W	T_C=25 °C T_A=25 °C, R_{thJA}=40 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.45	°C/W	-
Device on PCB, 6 cm² cooling area[2]	R_{thJA}	-	-	40	°C/W	-
Device on PCB, minimum footprint	R_{thJA}	-	-	62	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.4	3.1	3.6	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	1 10	10 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	- -	2 -2	5 -5	µA	V_{GS}=20 V, V_{DS}=0 V V_{GS}=-10 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	0.67	0.8	mΩ	V_{GS}=10 V, I_D=150 A
Gate resistance	R_G	-	70	-	Ω	-
Transconductance	g_{fs}	-	88	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=150 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	750	980	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	2900	3800	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	36	63	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	7	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=75 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	26	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=75 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	63	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=75 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	77	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=75 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6	-	nC	V_{DD}=30 V, I_D=150 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	155	-	nC	V_{DD}=30 V, I_D=150 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	185	-	nC	V_{DD}=30 V, I_D=150 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	8.7	-	V	V_{DD}=30 V, I_D=150 A, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	199	-	nC	V_{DS}=30 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test.
[2)] See ″Gate charge waveforms″ for parameter definition

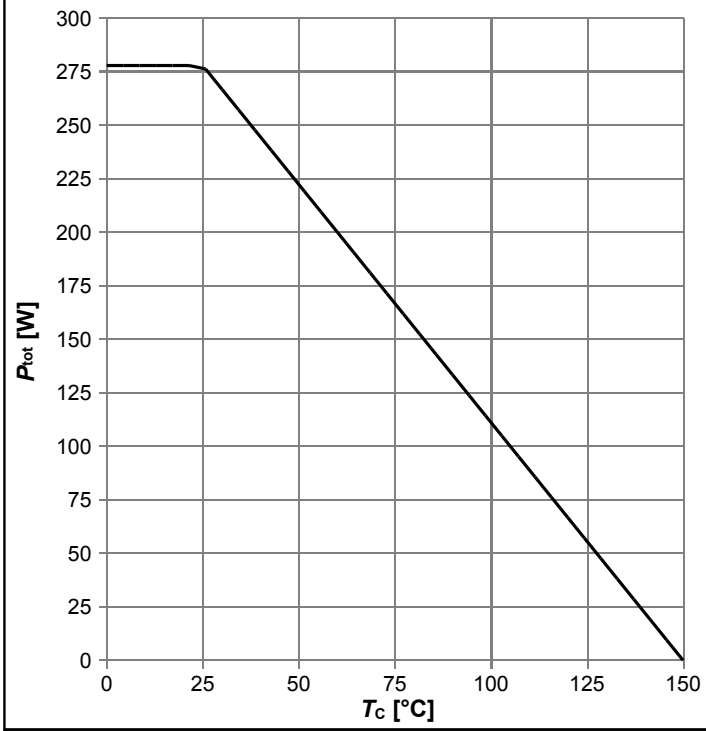
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	257	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	1816	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.88	1	V	V_{GS}=0 V, I_F=150 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	44	88	ns	V_R=30 V, I_F=150 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	198	396	nC	V_R=30 V, I_F=150 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

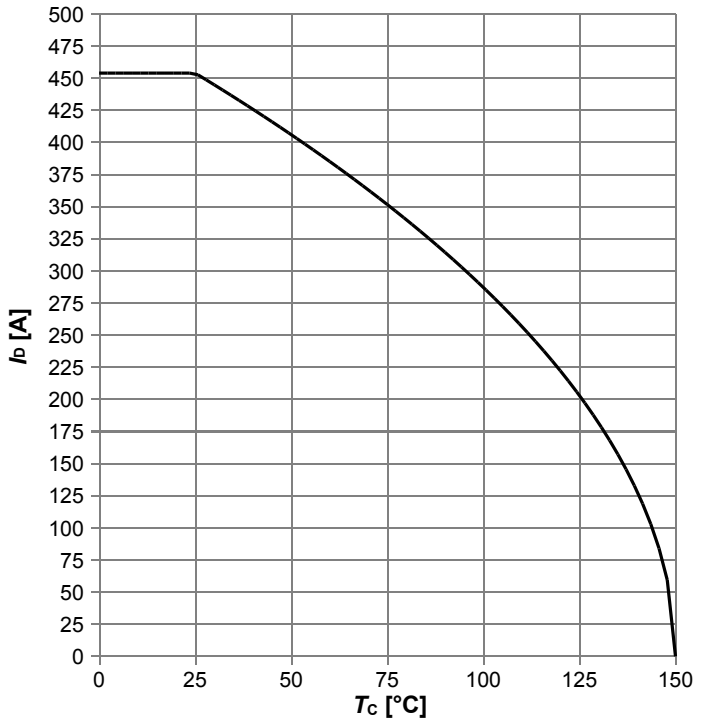
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



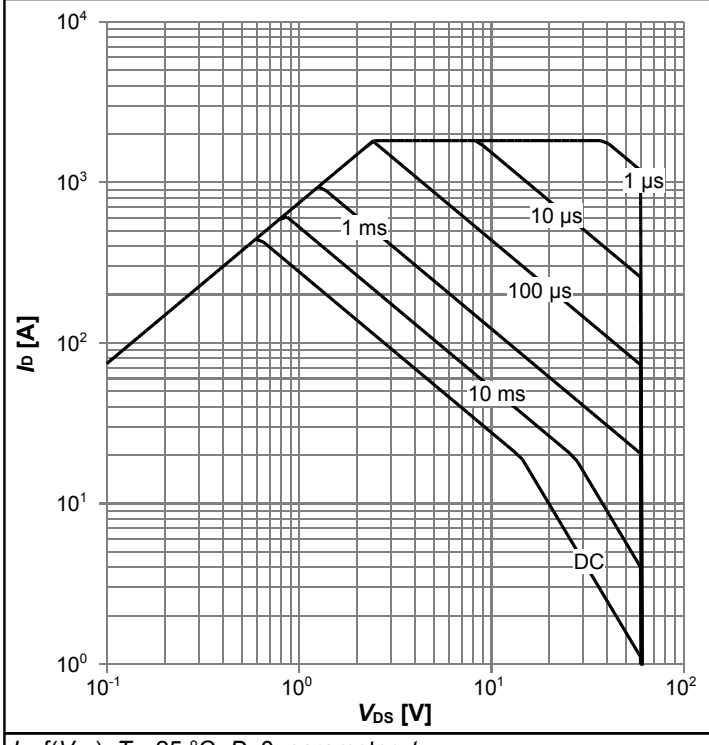
$P_{tot}=f(T_C)$

Diagram 2: Drain current



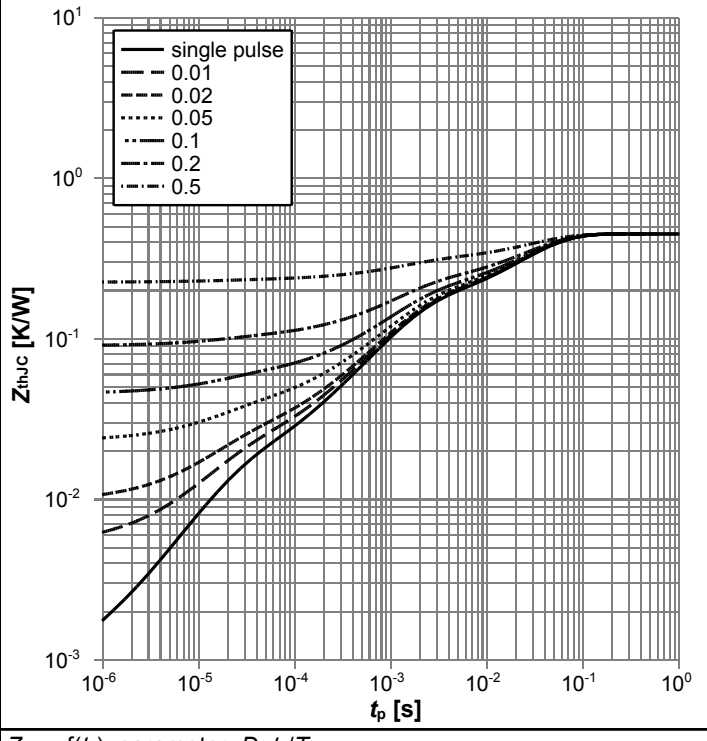
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



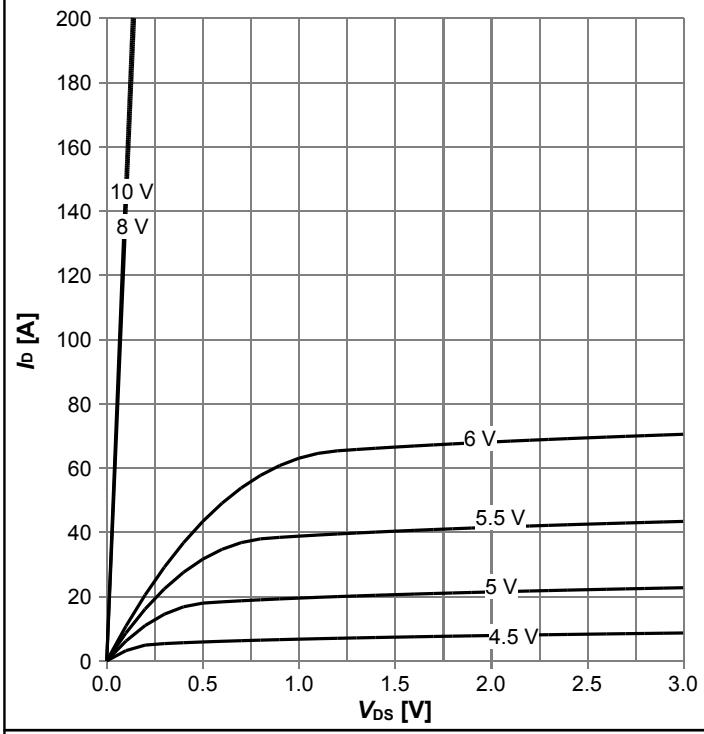
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



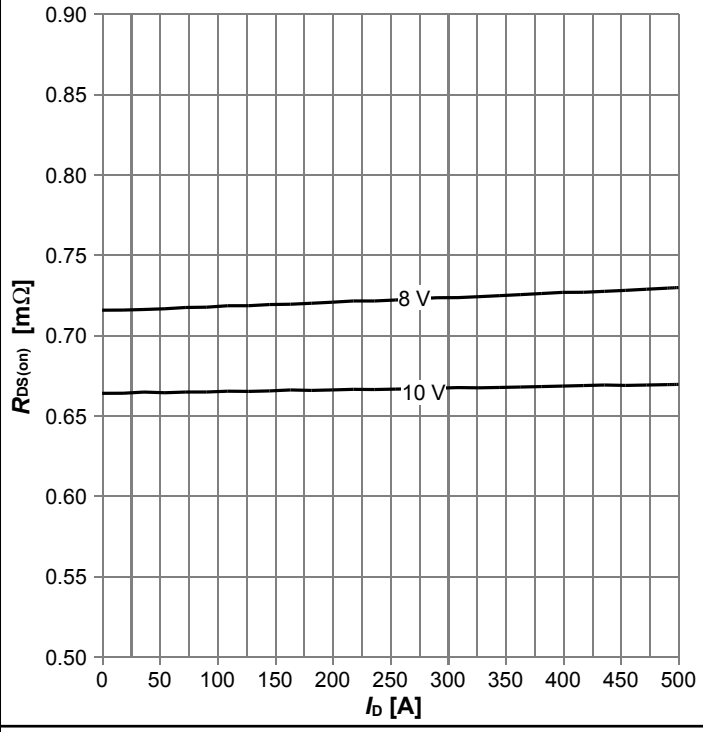
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



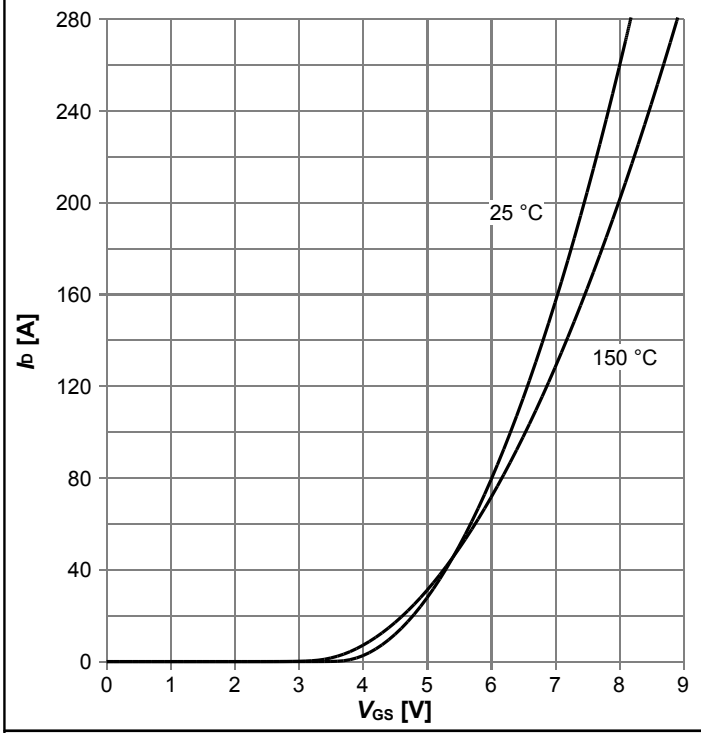
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



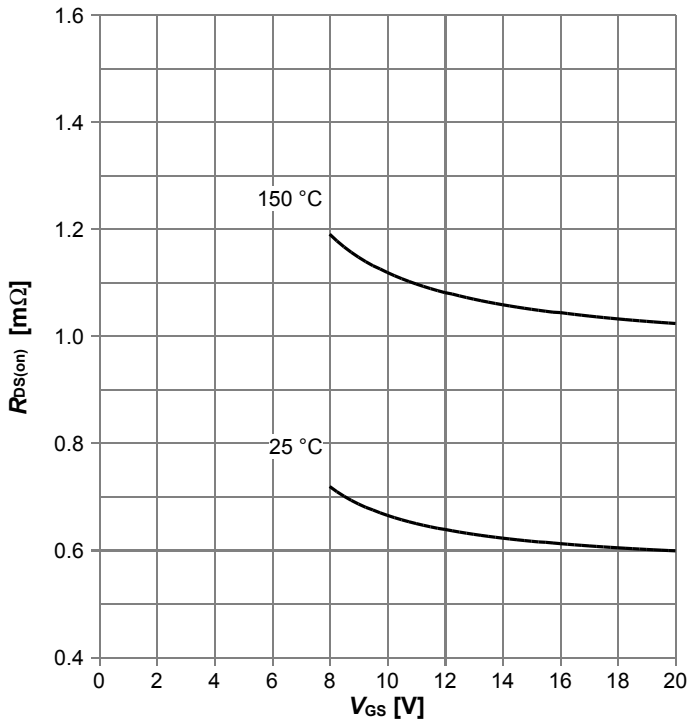
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



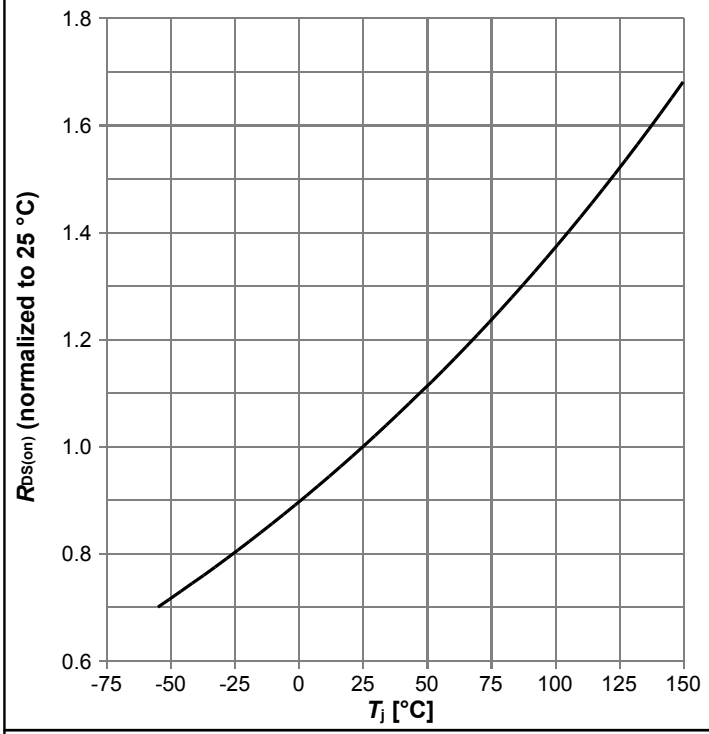
$I_D=f(V_{GS})$, $V_{DS}=10$ V; parameter: T_j

Diagram 8: Typ. drain-source on resistance



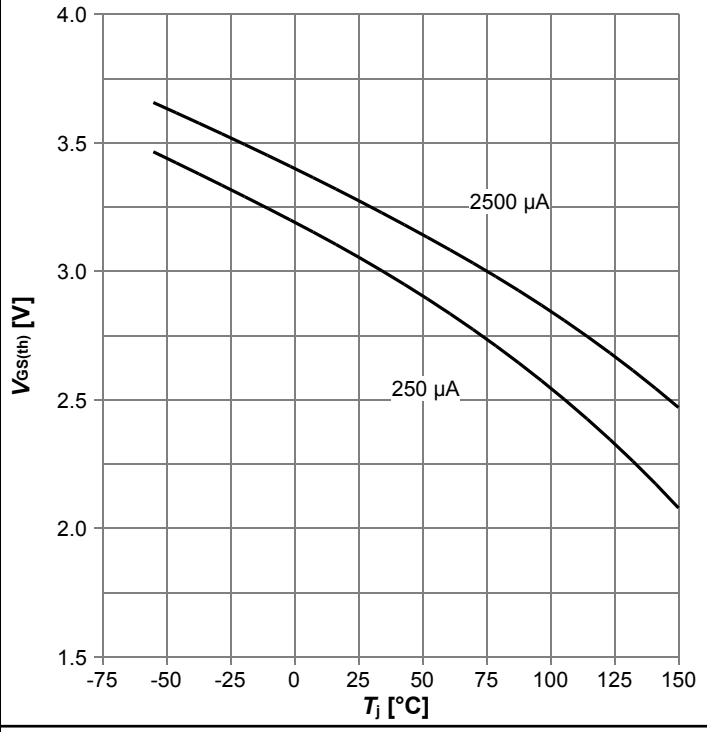
$R_{DS(on)}=f(V_{GS})$, $I_D=150$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



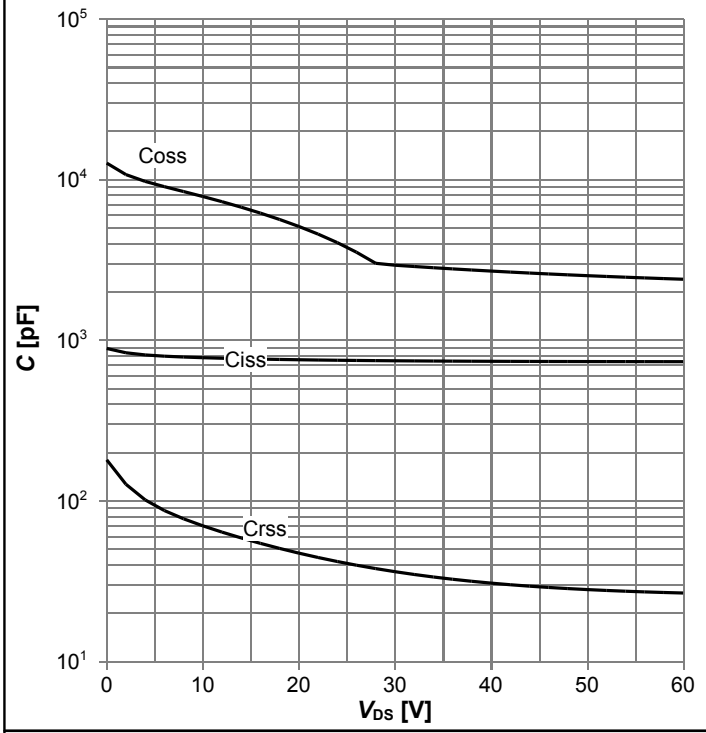
$R_{DS(on)}$=f(T_j), I_D=150 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



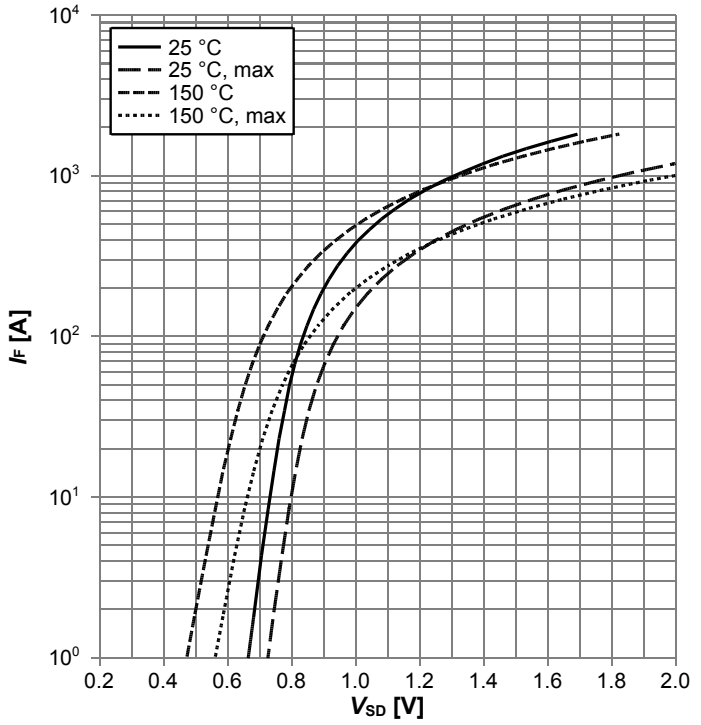
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



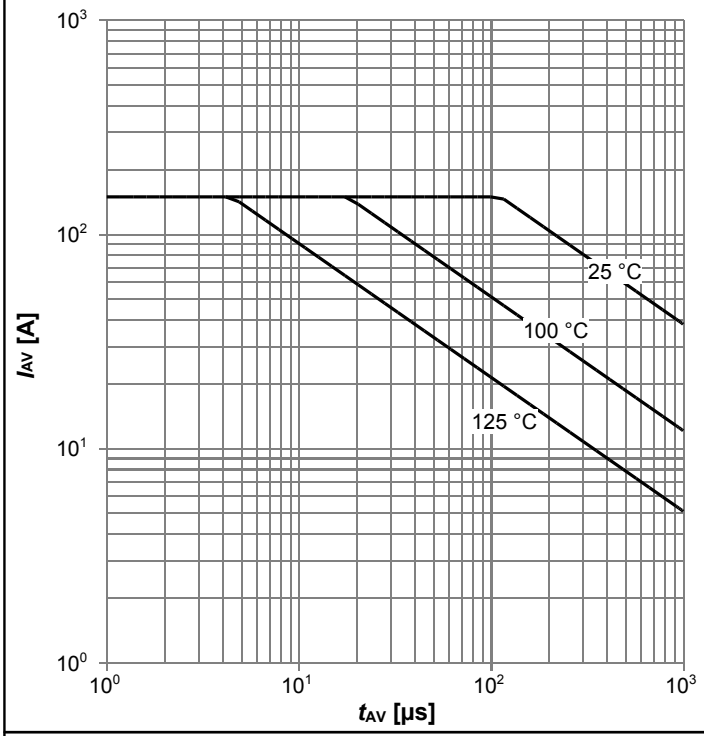
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



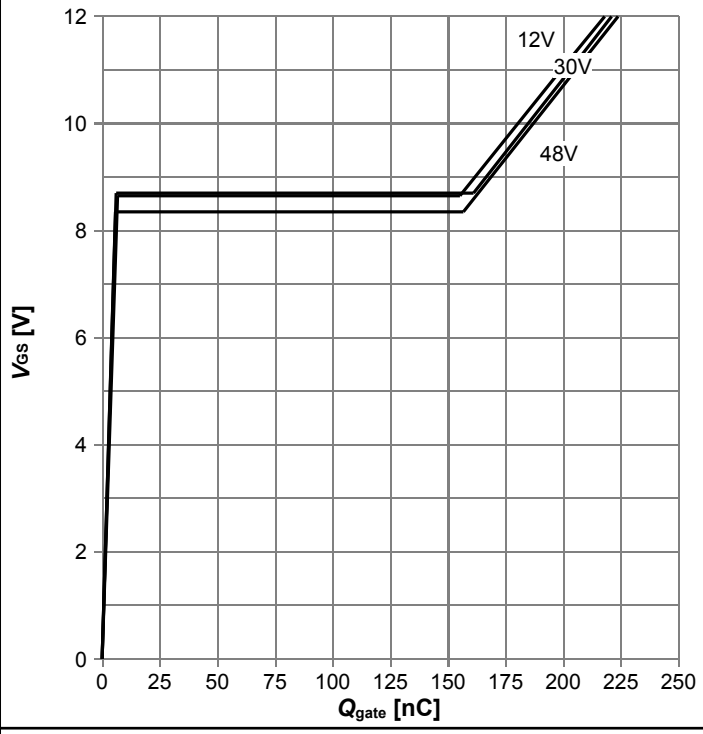
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



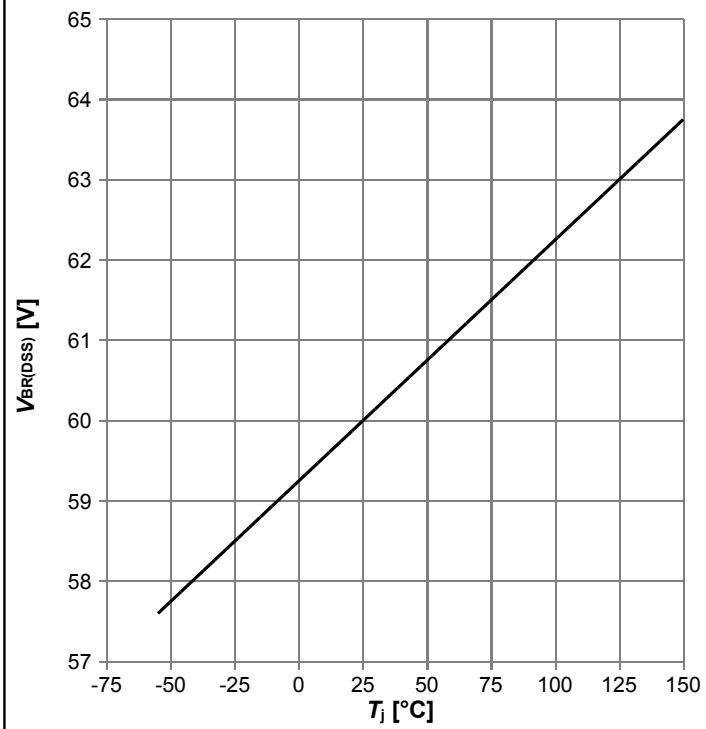
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



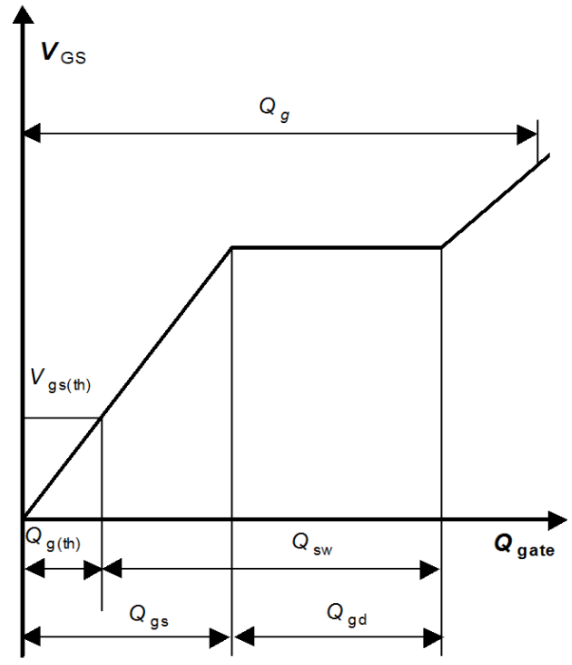
V_{GS}=f(Q_{gate}), I_D=150 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

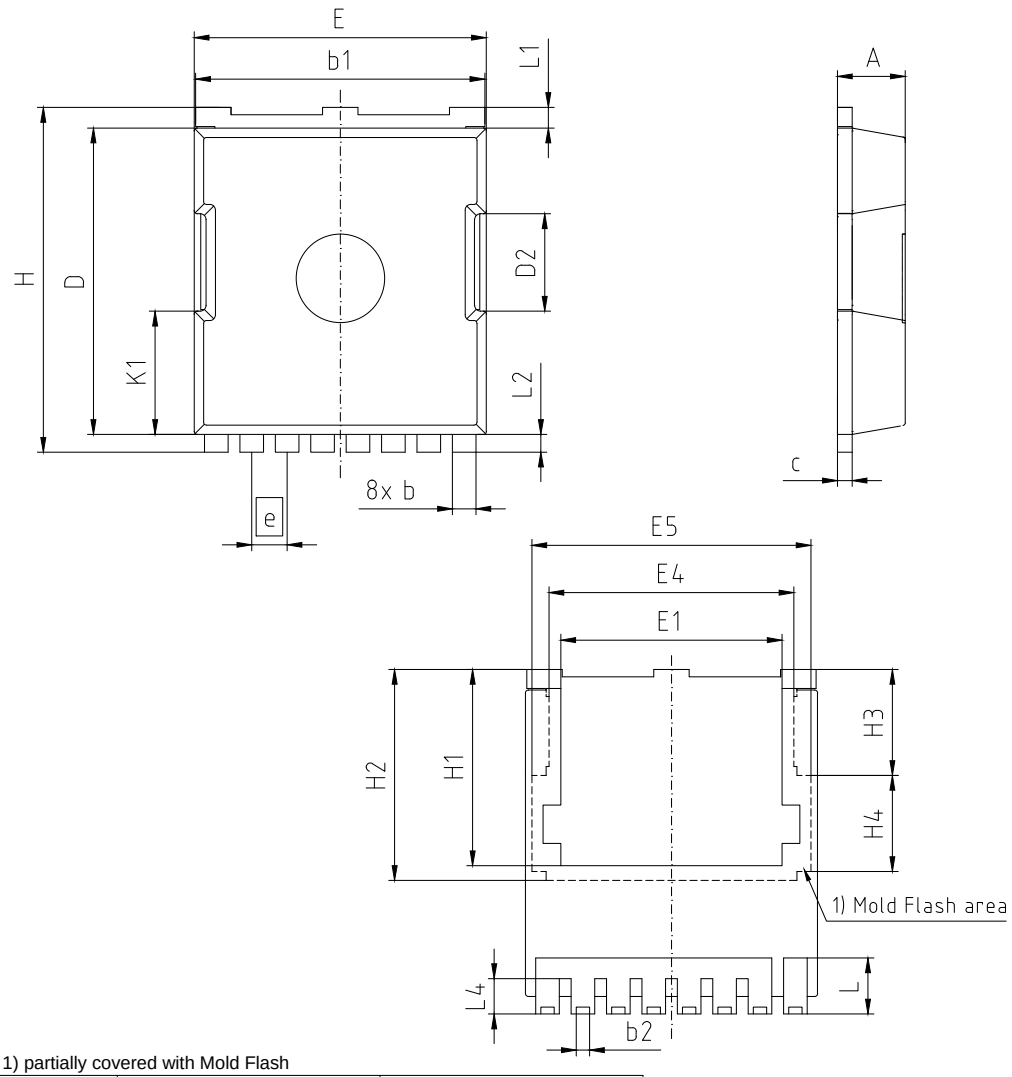


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



5 Package Outlines



1) partially covered with Mold Flash

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.40	0.087	0.094
b	0.70	0.90	0.028	0.035
b1	9.70	9.90	0.382	0.390
b2	0.42	0.50	0.017	0.020
c	0.40	0.60	0.016	0.024
D	10.28	10.58	0.405	0.416
D2	3.30		0.130	
E	9.70	10.10	0.382	0.398
E1	7.50		0.295	
E4	8.50		0.335	
E5	9.46		0.372	
e	1.20 (BSC)		0.047 (BSC)	
H	11.48	11.88	0.452	0.468
H1	6.55	6.75	0.258	0.266
H2	7.15		0.281	
H3	3.59		0.141	
H4	3.26		0.128	
N	8		8	
K1	4.18		0.165	
L	1.60	2.10	0.063	0.083
L1	0.70		0.028	
L2	0.60		0.024	
L4	1.00	1.30	0.039	0.051

DOCUMENT NO.
Z8B00169619

SCALE
0 2 0 2 4mm

EUROPEAN PROJECTION

ISSUE DATE
20-02-2014

REVISION
02

Figure 1 Outline PG-HSOF-8, dimensions in mm/inches

Revision History

IPT008N06NM5LF

Revision: 2022-09-19, Rev. 2.1

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2021-08-21	Release of final version
2.1	2022-09-19	Update Diagram 7

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Published by
Infineon Technologies AG
81726 München, Germany

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