EL7202C, EL7212C, EL7222C

High Speed, Dual Channel Power MOSFET Drivers

Features

- Industry standard driver replacement
- Improved response times
- Matched rise and fall times
- Reduced clock skew
- Low output impedance
- Low input capacitance
- High noise immunity
- Improved clocking rate
- Low supply current
- Wide operating voltage range

Applications

- Clock/line drivers
- CCD Drivers
- Ultra-sound transducer drivers
- Power MOSFET drivers
- Switch mode power supplies
- Class D switching amplifiers
- Ultrasonic and RF generators
- Pulsed circuits

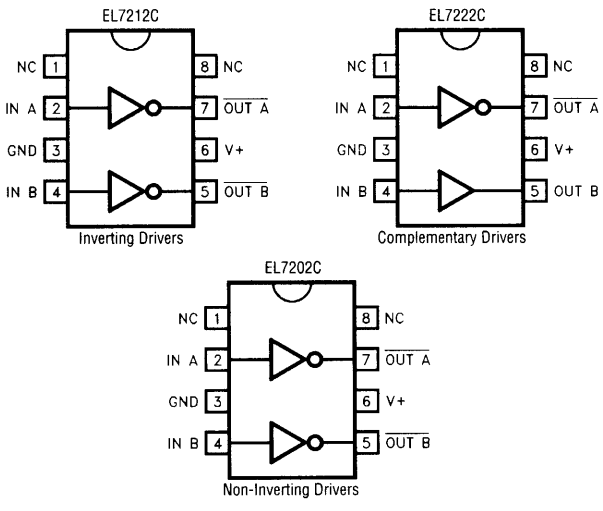
Ordering Information

Part No.	Package	Tape & Reel	Outline #
EL7202CN	PDIP-8	-	MDP0031
EL7202CS	SO-8	-	MDP0027
EL7202CS-T7	SO-8	7 in	MDP0027
EL7202CS-T13	SO-8	13 in	MDP0027
EL7212CN	PDIP-8	-	MDP0031
EL7212CS	SO-8	-	MDP0027
EL7212CS-T7	SO-8	7 in	MDP0027
EL7212CS-T13	SO-8	13 in	MDP0027
EL7222CN	PDIP-8	-	MDP0031
EL7222CS	SO-8	-	MDP0027
EL7222CS-T7	SO-8	7 in	MDP0027
EL7222CS-T13	SO-8	13 in	MDP0027

General Description

The EL7202C, EL7212C, EL7222C ICs are matched dual-drivers ICs that improve the operation of the industry standard DS0026 clock drivers. The Elantec Versions are very high speed drivers capable of delivering peak currents of 2.0 amps into highly capacitive loads. The high speed performance is achieved by means of a proprietary "Turbo-Driver" circuit that speeds up input stages by tapping the wider voltage swing at the output. Improved speed and drive capability are enhanced by matched rise and fall delay times. These matched delays maintain the integrity of input-to-output pulse-widths to reduce timing errors and clock skew problems. This improved performance is accompanied by a 10 fold reduction in supply currents over bipolar drivers, yet without the delay time problems commonly associated with CMOS devices. Dynamic switching losses are minimized with non-overlapped drive techniques.

Connection Diagrams



Manufactured under U.S. Patent Nos. 5,334,883, #5,341,047

January 1996 Rev. B

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Absolute Maximum Ratings

Supply (V+ to Gnd)	16.5V	Operating Junction Temperature	125°C
Input Pins	-0.3V to +0.3V above V+	Power Dissipation	
Combined Peak Output Current	4A	SO	570mW
Storage Temperature Range	-65°C to +150°C	PDIP	1050mW
Ambient Operating Temperature	-40°C to +85°C		

Important Note:

All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

DC Electrical Characteristics

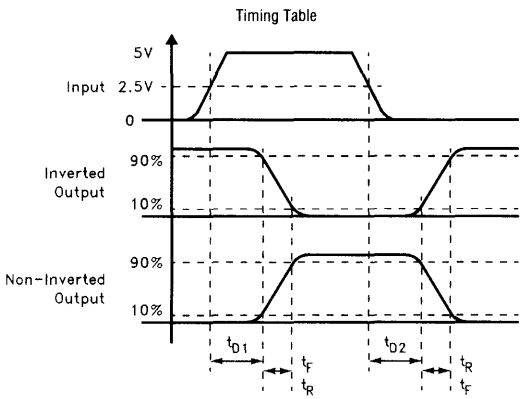
T_A = 25°C, V = 15V unless otherwise specified

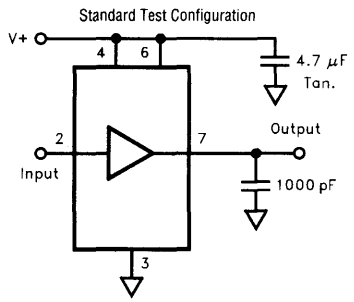
Parameter		Description	Test Conditions	Min	Typ	Max	Units
Input	V_{IH}	Logic "1" Input Voltage		2.4			V
	I_{IH}	Logic "1" Input Current	@V+		0.1	10	µA
	V_{IL}	Logic "0" Input Voltage				0.8	V
	I_{IL}	Logic "0" Input Current	@0V		0.1	10	µA
	V_{HYS}	Input Hysteresis			0.3		V
Output	R_{OH}	Pull-Up Resistance	I_{OUT} = -100mA		3	6	Ω
	R_{OL}	Pull-Down Resistance	I_{OUT} = +100mA		4	6	Ω
	I_{PK}	Peak Output Current	Source Sink		2 2		A
	I_{DC}	Continuous Output Current	Source/Sink	100			mA
Power Supply	I_S	Power Supply Current	Inputs High/7202 Inputs High/7212 Inputs High/7222		4.5 1 2.5	7.5 2.5 5.0	mA
	V_S	Operating Voltage		4.5		15	V

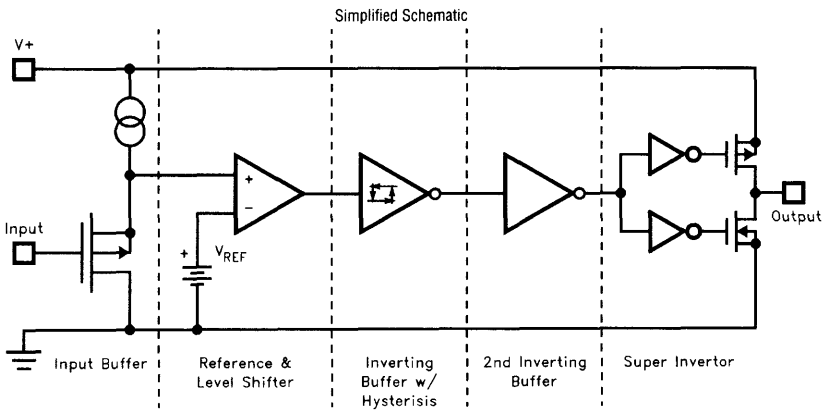
AC Electrical Characteristics

T_A = 25°C, V = 15V unless otherwise specified

Parameter		Description	Test Conditions	Min	Typ	Max	Units
Switching Characteristics	t_R	Rise Time	C_L = 500pF C_L = 1000pF		7.5 10	 20	ns
	t_F	Fall Time	C_L = 500pF C_L = 1000pF		10 13	 20	ns
	t_{D1}	Turn-On Delay Time	See Timing Table		18	25	ns
	t_{D2}	Turn-Off Delay Time	See Timing Table		20	25	ns


Timing Table
5V
Input 2.5V
0
Inverted Output
90%
10%
Non-Inverted Output
90%
10%
t_{D1}
t_F
t_R
t_{D2}
t_R
t_F


Standard Test Configuration
V+
4
6
4.7 µF Tan.
2
Input
7
Output
1000 pF
3


Simplified Schematic
V+
Input
V_{REF}
Output
Input Buffer
Reference & Level Shifter
Inverting Buffer w/ Hysterisis
2nd Inverting Buffer
Super Invertor

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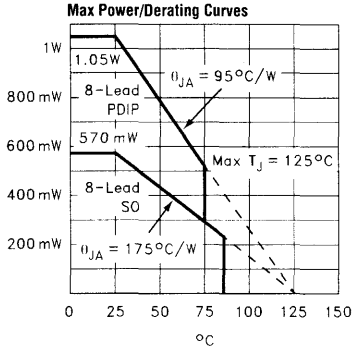
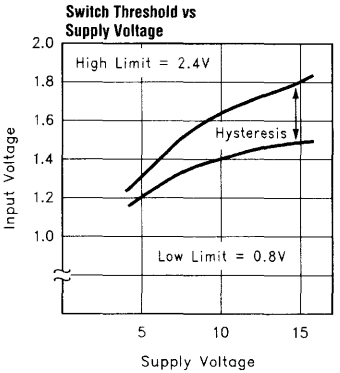
Typical Performance Curves

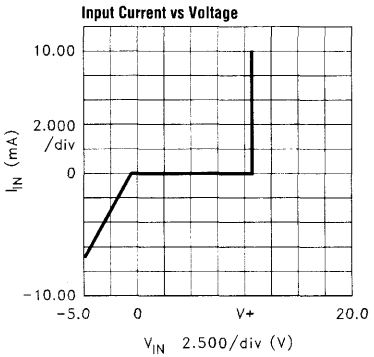
Max Power/Derating Curves



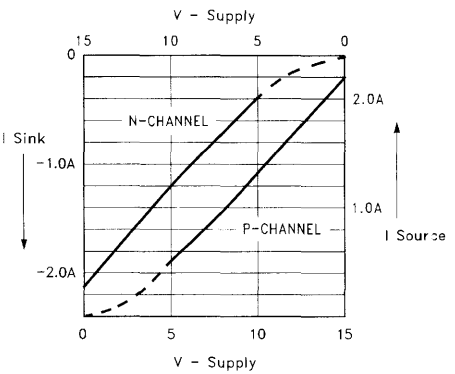
Switch Threshold vs Supply Voltage



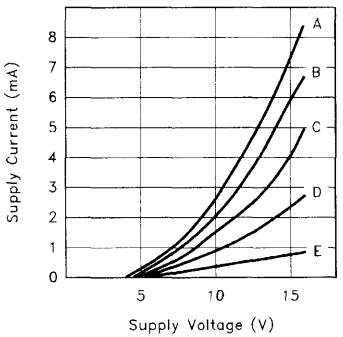
Input Current vs Voltage



Peak Drive vs Supply Voltage



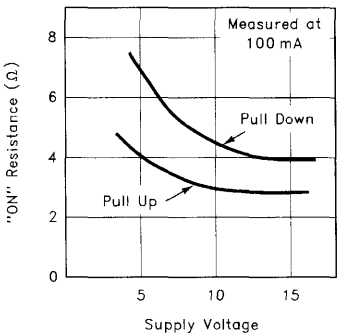
Quiescent Supply Current



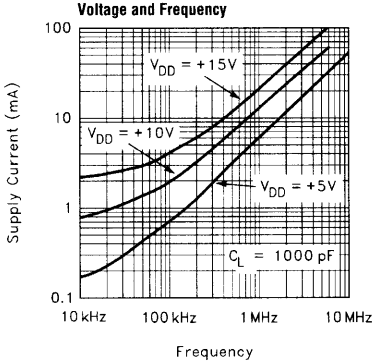
CASE:

Device	Input Level	Curve
EL7202	GND	A
EL7202	GND, V+	B
EL7202	V+	C
EL7212	GND	C
EL7212	GND, V+	D
EL7212	V+	E
EL7222	GND	B
EL7222	GND, V+	C
EL7222	V+	D

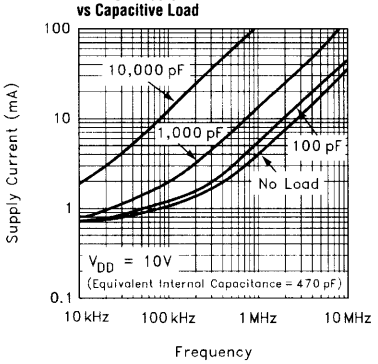
"ON" Resistance vs Supply Voltage



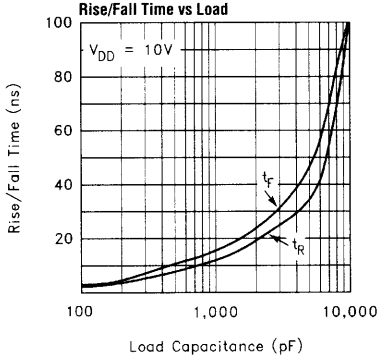
Average Supply Current vs Voltage and Frequency



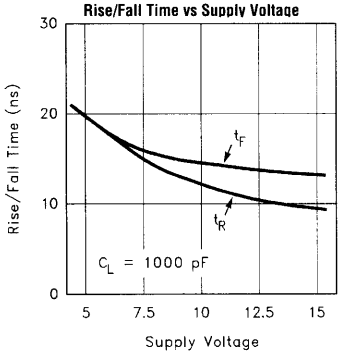
Average Supply Current vs Capacitive Load

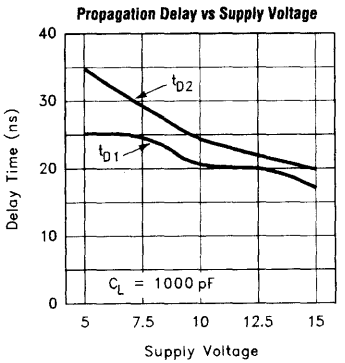


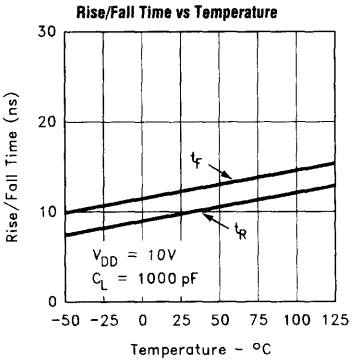
Rise/Fall Time vs Load

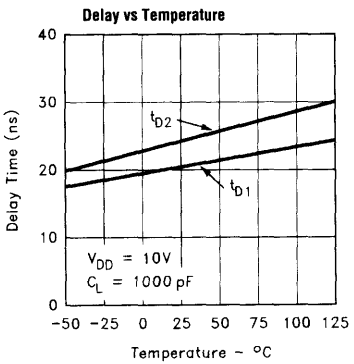


Rise/Fall Time vs Supply Voltage

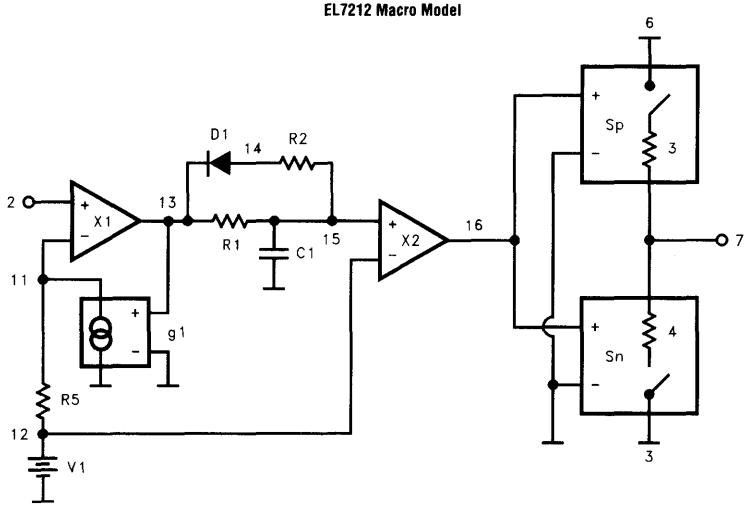



Propagation Delay vs Supply Voltage
Delay Time (ns)
40
30
20
10
0
t_{D2}
t_{D1}
C_L = 1000 pF
5
7.5
10
12.5
15
Supply Voltage


Rise/Fall Time vs Temperature
Rise/Fall Time (ns)
30
20
10
0
t_F
t_R
V_{DD} = 10V
C_L = 1000 pF
-50 -25 0 25 50 75 100 125
Temperature - °C


Delay vs Temperature
Delay Time (ns)
40
30
20
10
0
t_{D2}
t_{D1}
V_{DD} = 10V
C_L = 1000 pF
-50 -25 0 25 50 75 100 125
Temperature - °C

EL7212 Macro Model




```
**** EL7212 model ****
*                 input
*                 |     gnd
*                 |     |     Vsupply
*                 |     |     |     Vout
.subckt M7212     2     3     6     7
V1 12 3 1.6
R1 13 15 1k
R2 14 15 5k
R5 11 12 100
C1 15 3 43.3 pF
D1 14 13 dmod
X1 13 11 2 3 comp1
X2 16 12 15 3 comp1
sp 6 7 16 3 spmod
sn 7 3 16 3 snmod
g1 11 0 13 0 938µ
.model dmod d
.model spmod vswitch ron3 roff2meg von1 voff1.5
.model snmod vswitch ron4 roff2meg von3 voff2
.ends M7212
.subckt comp1 out inp inm vss
e1 out vss table { (v(inp) v(inm))* 5000}   (0,0) (3.2,3.2)
Rout out vss 10meg
Rinp inp vss 10meg
Rinm inm vss 10meg
.ends comp1
```