

## Description

The 9FGV1002C / 9FGV1006C are members of the Renesas' PhiClock™ programmable clock generator family. These devices are optimized for low phase noise spread-spectrum applications such as PCIe® Express. Four user-defined configurations may be selected via two hardware select pins or two I<sup>2</sup>C bits, allowing easy software selection of the desired configuration. Any one of the four OTP configurations may be specified as the default when operating in I<sup>2</sup>C mode.

The 9FGV1002C is available in a version targeting automotive applications with the following characteristics:

- ISO9001 compliant
- AEC-Q100 qualified
- -40°C to +105°C (grade 2 equivalent) operation
- PPAP support

## Compute/Networking Applications

- High-performance Computing (HPC)
- Enterprise Storage including eSSDs
- 10G / 25G / 100G Ethernet
- Fiber Optic Modules
- NVLink

## Automotive Applications

- Infotainment
- Gateway
- Domain Controller
- Zone Controller

## PCIe Clocking Architectures

- PCIe Gen1–6 Common Clocked (CC)
- Independent Reference (IR) without spread spectrum (SRnS)
- Independent Reference (IR) with spread spectrum (SRIS)

## Output Features

- 2 or 4 programmable output pairs plus 2 LVCMOS REF outputs
- 1MHz–325MHz LVDS or LP-HCSL outputs
- 1MHz–200MHz LVCMOS outputs

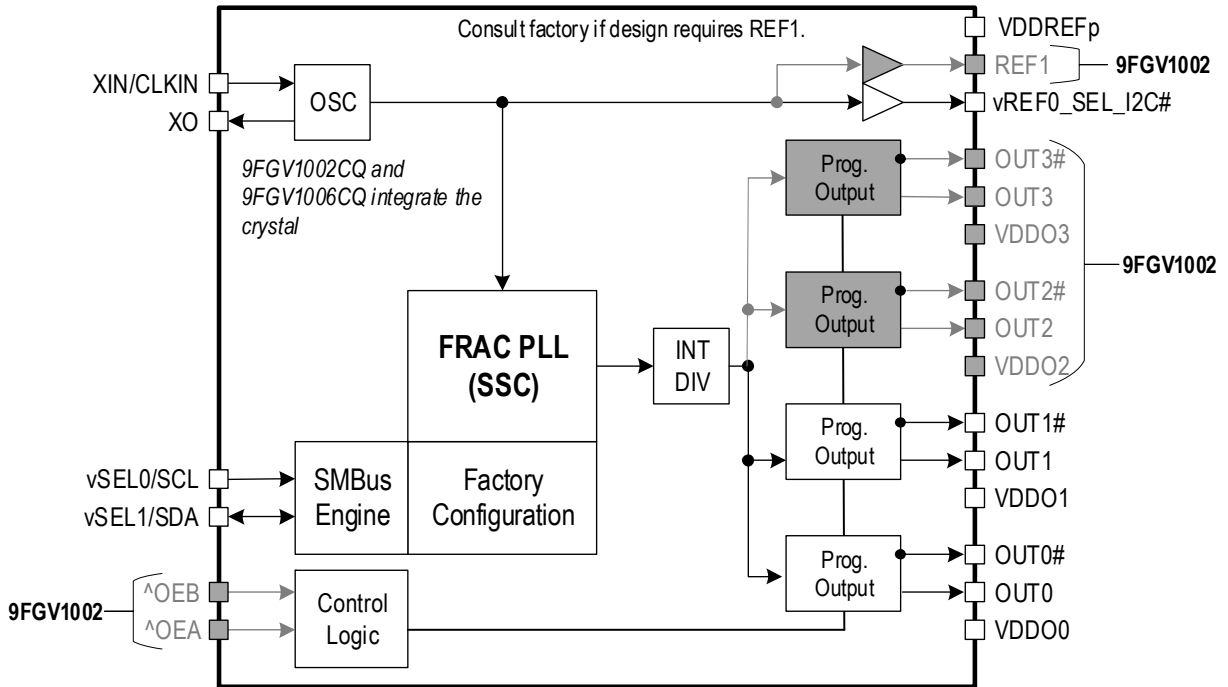
## Features

- 1.8V, 2.5V and/or 3.3V core power supplies
- Individual 1.8V, 2.5V or 3.3V V<sub>DDO</sub> for each output pair
- -40°C to +85°C operation – standard product
- -40°C to +105°C operation – 9FGV1002C automotive product
- Direct connection to HCSL, LVDS and LVCMOS I/O standards
- HCSL utilizes Renesas' LP-HCSL technology for improved performance, lower power and higher integration:
  - Programmable output impedance of 85Ω or 100Ω
- Easy AC-coupling to LVPECL and CML logic – see application note [AN-891](#) for alternate terminations
- On-board OTP supports up to 4 complete configurations
  - 1 integer, fractional or spread spectrum output frequency per configuration
  - Configuration selected via strapping pins or I<sup>2</sup>C
- Internal crystal load capacitors
- < 125mW (9FGV1002C – 1.8V with 100MHz LP-HCSL outputs)
- < 100mW (9FGV1006C – 1.8V with 100MHz LP-HCSL outputs)
- 4 programmable I<sup>2</sup>C addresses: D0, D2, D4, D6
- Easily configured with Renesas [Timing Commander™](#) software or Web Configuration tool
- 4 × 4 mm 24-VFQFPN with integrated crystal option
- 3 × 3 mm 16-LGA with integrated crystal option
- Programmable spread spectrum modulation frequency and amount

## Key Specifications

- 276fs RMS 12kHz–20MHz typical phase jitter at 156.25MHz
- PCIe Gen6 jitter (CC) < 50fs RMS

## 9FGV1002C / 9FGV1006C Block Diagram



**Table 1. OE Mapping**

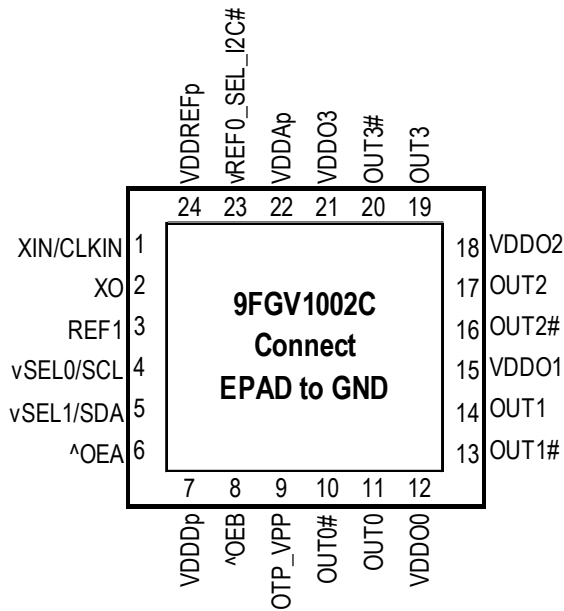
OE[B:A]	OUT0	OUT1	OUT2	OUT3	REF0	REF1
00	Running	Stopped	Stopped	Stopped	Running	Running
01	Running	Running	Stopped	Stopped	Running	Running
10	Running	Running	Running	Stopped	Running	Running
11	Running	Running	Running	Running	Running	Running

## Contents

Description	1
Compute/Networking Applications	1
Automotive Applications	1
PCIe Clocking Architectures	1
Output Features	1
Features	1
Key Specifications	1
9FGV1002C / 9FGV1006C Block Diagram	2
Pin Assignments	4
9FGV1002C Pin Descriptions	5
9FGV1006C Pin Descriptions	6
Phase Noise Plots	7
Absolute Maximum Ratings	9
Thermal Characteristics	9
Recommended Operating Conditions	10
Electrical Characteristics	11
I2C Bus Characteristics	22
Test Loads	23
Crystal Characteristics	25
Package Outline Drawings	25
Marking Diagrams	25
Standard Configurations	26
Ordering Information	27
Revision History	27

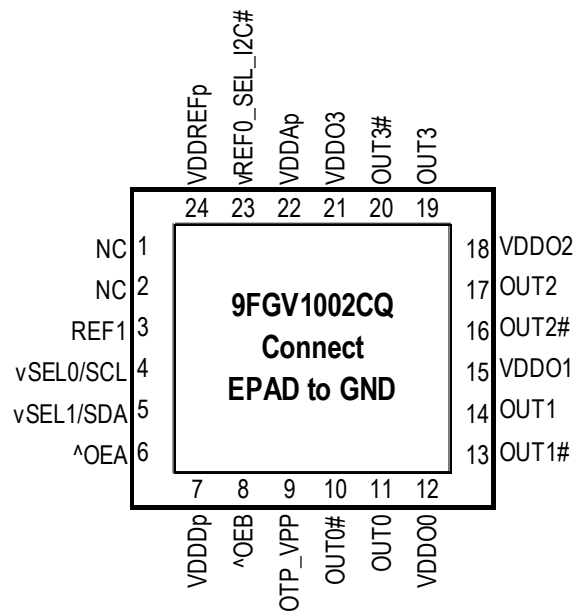
## Pin Assignments

**Figure 1. Pin Assignments for 9FGV1002C 4 × 4 mm 24-VFQFPN and 24-LGA Packages – Top View**



**4 × 4 mm 24-QFN, 0.5mm pitch**

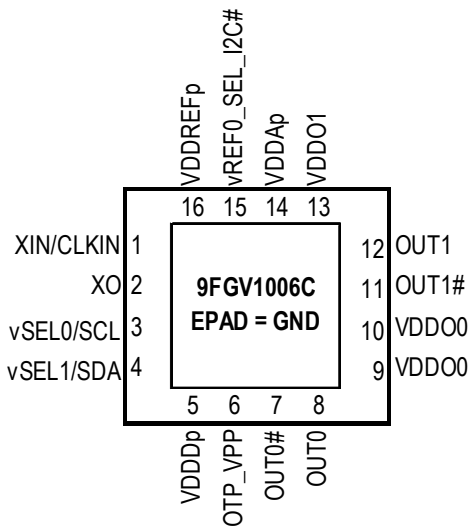
^ prefix indicates internal pull-up  
 v prefix indicates internal pull-down resistor  
 Note: The order of OUT3 is reversed from OUT[0:2]



**4 × 4 mm 24-LGA, 0.5mm pitch**

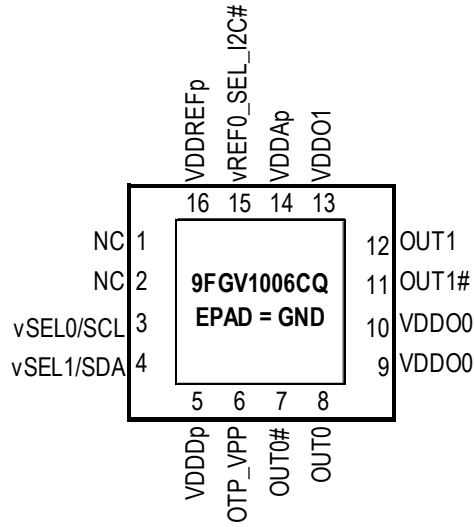
^ prefix indicates internal pull-up resistor  
 v prefix indicates internal pull-down resistor  
 Note: The order of OUT3 is reversed from OUT[0:2]

**Figure 2. Pin Assignments for 9FGV1006C 3 × 3 mm 16-LGA Package – Top View**



**16-LGA 3 x 3 mm, 0.5mm pitch**

^ prefix indicates internal pull-up resistor  
 v prefix indicates internal pull-down resistor



**16-LGA 3 x 3 mm, 0.5mm pitch**

^ prefix indicates internal pull-up resistor  
 v prefix indicates internal pull-down resistor

## 9FGV1002C Pin Descriptions

**Note:** Unused outputs can be programmed off and left floating. Output supplies  $V_{DDREF}$  and  $V_{DDO2}$  have to be connected. If OUT0 is used,  $V_{DDO1}$  must also be connected.

**Table 2. 9FGV1002C Pin Descriptions**

Number	Name	Type	Description
1 <sup>[a]</sup>	XIN/CLKIN	Input	Crystal input or reference clock input.
2 <sup>[a]</sup>	XO	Output	Crystal output.
3	REF1	Output	LVC MOS reference output.
4	vSEL0/SCL	Input	Select pin for internal frequency configurations/I <sup>2</sup> C clock pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
5	vSEL1/SDA	I/O	Select pin for internal frequency configurations/I <sup>2</sup> C data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
6	^OE A	Input	Active high input for enabling outputs. This pin has an internal pull-up resistor. 0 = disable outputs, 1 = enable outputs.
7	VDDDp	Power	Digital power. Connect to 1.8V, 2.5V or 3.3V.
8	^OE B	Input	Active high input for enabling outputs. This pin has an internal pull-up resistor. 0 = disable outputs, 1 = enable outputs.
9	OTP_VPP	Power	Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as $V_{DD}$ .
10	OUT0#	Output	Complementary output clock 0.
11	OUT0	Output	Output clock 0.
12	VDDO0	Power	Power supply for output 0.
13	OUT1#	Output	Complementary output clock 1.
14	OUT1	Output	Output clock 1.
15	VDDO1	Power	Power supply for output 1.
16	OUT2#	Output	Complementary output clock 2.
17	OUT2	Output	Output clock 2.
18	VDDO2	Power	Power supply for output 2.
19	OUT3	Output	Output clock 3.
20	OUT3#	Output	Complementary output clock 3.
21	VDDO3	Power	Power supply for output 3.
22	VDDAp	Power	Analog power. Connect to same voltage as VDDDp, with proper filtering.
23	vREF0_SEL_I2C#	Latched I/O	Latched input/LVC MOS output. At power-up, the state of this pin is latched to select the state of the I <sup>2</sup> C pins. After power-up, the pin acts as an LVC MOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA.
24	VDDREFp	Power	Power supply for REF outputs and the internal XO. Nominal voltages are 1.8V, 2.5V or 3.3V.
25	EPAD	GND	Connect to ground.

[a] These pins are 'No Connect' on 9FGV1002Q integrated quartz versions and should have no stubs.

## 9FGV1006C Pin Descriptions

**Note:** Unused outputs can be programmed off and left floating. Output supplies  $V_{DDREF}$  and  $V_{DDO1}$  have to be connected. This means that if only one output is to be used, it must be OUT1. If OUT0 is used, both pins 9 and 10 must be connected. They may share the same power filter.

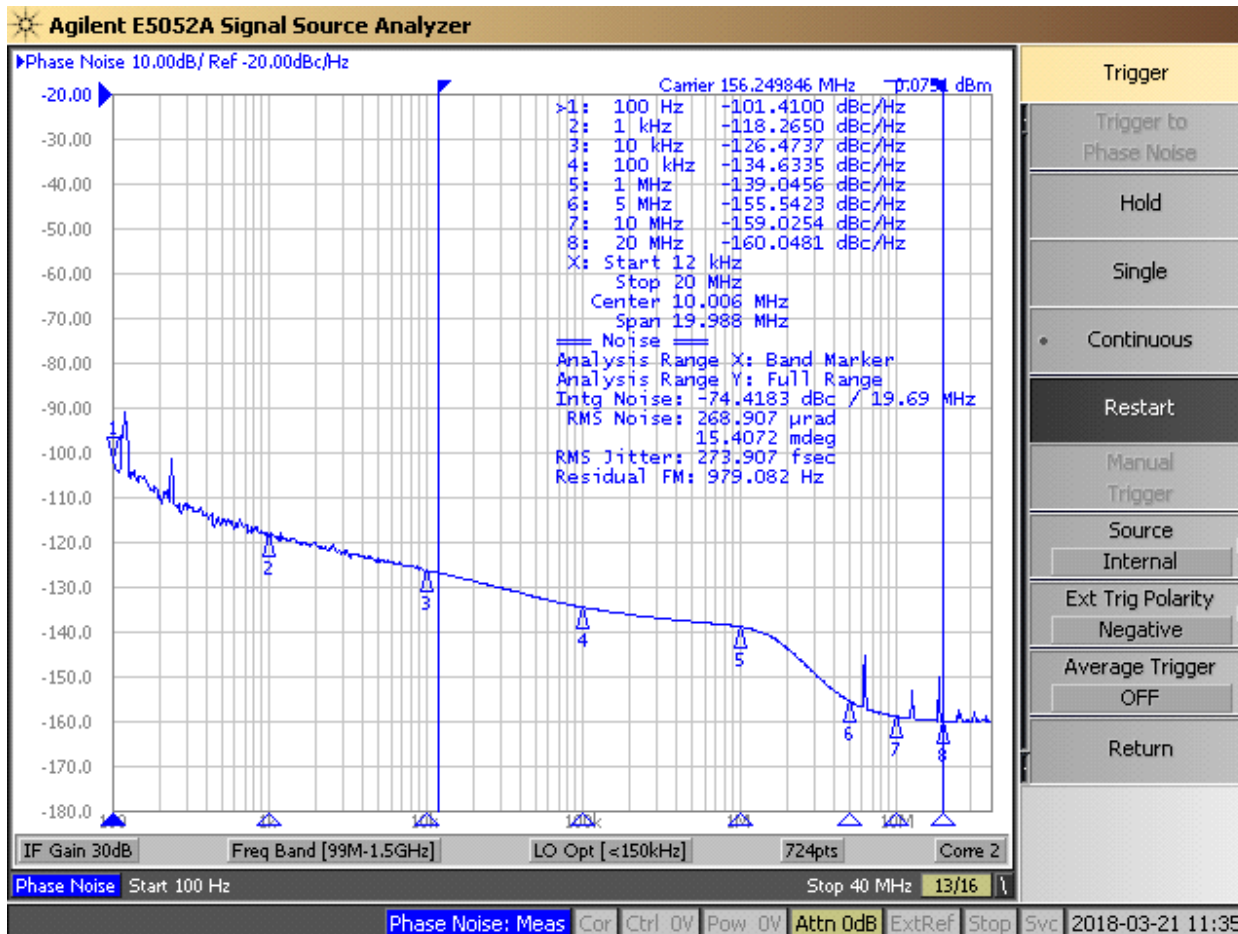
**Table 3. 9FGV1006C Pin Descriptions**

Number	Name	Type	Description
1 <sup>[a]</sup>	XIN/CLKIN	Input	Crystal input or reference clock input.
2 <sup>[a]</sup>	XO	Output	Crystal output.
3	vSEL0/SCL	Input	Select pin for internal frequency configurations/I <sup>2</sup> C Clock pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
4	vSEL1/SDA	I/O	Select pin for internal frequency configurations/I <sup>2</sup> C Data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
5	VDDDp	Power	Digital power. Connect to 1.8V, 2.5V or 3.3V.
6	OTP_VPP	Power	Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as $V_{DD}$ .
7	OUT0#	Output	Complementary output clock 0.
8	OUT0	Output	Output clock 0.
9	VDDO0	Power	Power supply for output 0.
10	VDDO0	Power	Power supply for output 0.
11	OUT1#	Output	Complementary output clock 1.
12	OUT1	Output	Output clock 1.
13	VDDO1	Power	Power supply for output 1.
14	VDDAp	Power	Analog power. Connect to same voltage as VDDDp, with proper filtering.
15	vREF0_SEL_I2C#	Latched I/O	Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the I <sup>2</sup> C pins. After power-up, the pin acts as an LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA.
16	VDDREFp	Power	Power supply for REF outputs and the internal XO. Nominal voltages are 1.8V, 2.5V or 3.3V.
17	EPAD	GND	Connect to ground.

[a] These pins are 'No Connect' on 9FGV1006Q integrated quartz version and should have no stubs.

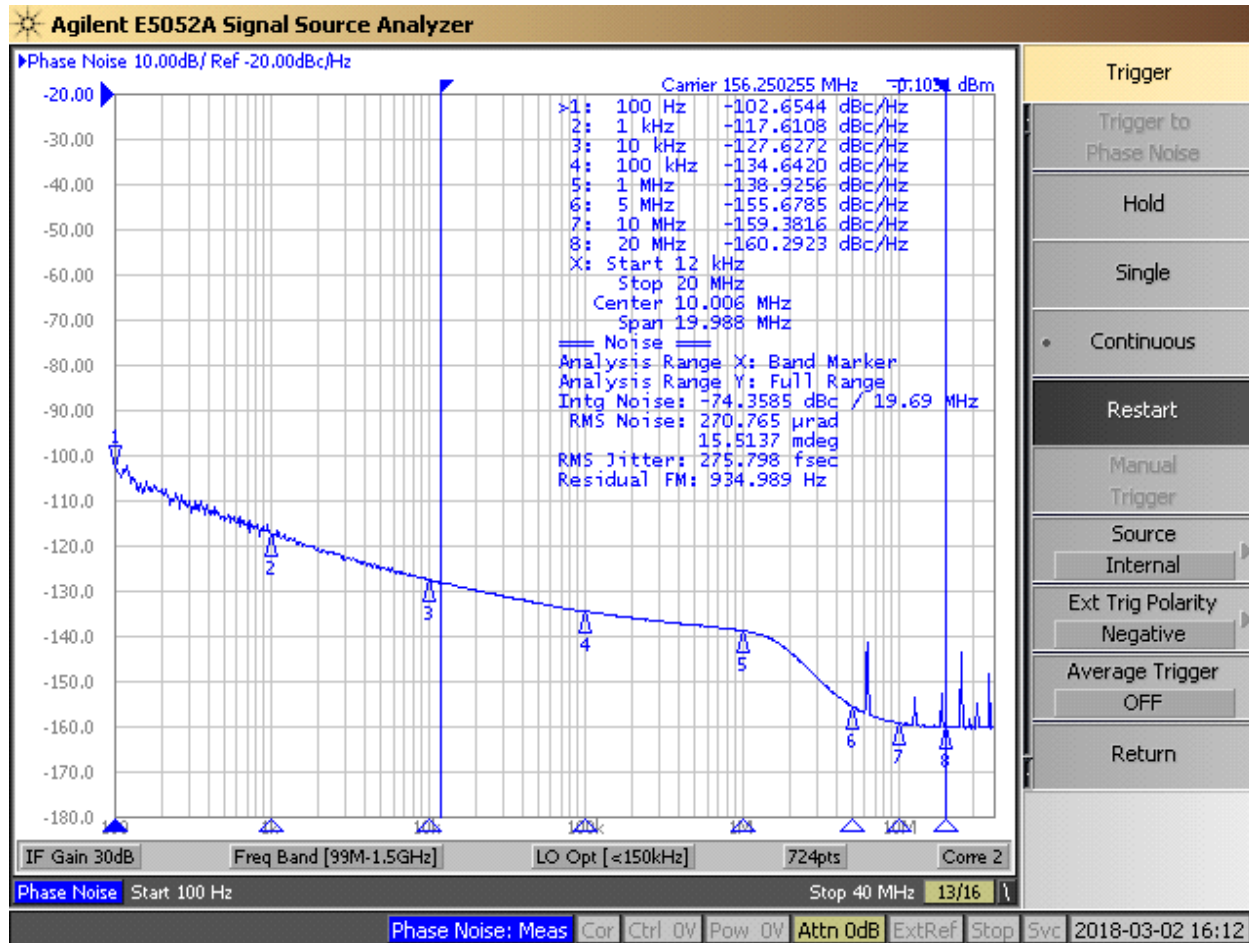
## Phase Noise Plots

Figure 3. 9FGV1002C Phase Noise Plot<sup>1</sup>, 3.3V, 25°C.



<sup>1</sup> See Test Frequencies for Jitter Measurements table for details.

**Figure 4. 9FGV1006C Phase Noise Plot<sup>1</sup>, 3.3V, 25°C.**



<sup>1</sup> See Test Frequencies for Jitter Measurements table for details.



## Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGV1002C / 9FGV1006C at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 4. Absolute Maximum Ratings**

Parameter	Rating
Supply Voltage, $V_{DDA}$ , $V_{DDD}$ , $V_{DDO}$	3.9V
Storage Temperature, $T_{STG}$	-65°C to +150°C
ESD Human Body Model	2000V
Junction Temperature	125°C
<b>Inputs</b>	
XIN/CLKIN	0V to 1.2V voltage swing
Other Inputs	-0.5V to $V_{DDD} + 0.3V$
<b>Outputs</b>	
Outputs, $V_{DDO}$ (LVCMOS)	-0.5V to $V_{DDO} + 0.5V$
Outputs, IO (SDA)	10mA

## Thermal Characteristics

**Table 5. Thermal Characteristics for 24-pin Devices (ePAD soldered to board)**

Parameter	Symbol	Conditions	Package	Typical Values	Unit
Thermal Resistance (devices with external crystal)	$\theta_{JC}$	Junction to case.	NBG24	52	°C/W
	$\theta_{Jb}$	Junction to base.		2.3	°C/W
	$\theta_{JA0}$	Junction to air, still air.		44	°C/W
	$\theta_{JA1}$	Junction to air, 1 m/s air flow.		37	°C/W
	$\theta_{JA3}$	Junction to air, 3 m/s air flow.		33	°C/W
	$\theta_{JA5}$	Junction to air, 5 m/s air flow.		32	°C/W
Thermal Resistance Q-series (devices with internal crystal)	$\theta_{JC}$	Junction to case.	LTG24	57.3	°C/W
	$\theta_{Jb}$	Junction to base.		24.3	°C/W
	$\theta_{JA0}$	Junction to air, still air.		79.8	°C/W
	$\theta_{JA1}$	Junction to air, 1 m/s air flow.		73.9	°C/W
	$\theta_{JA3}$	Junction to air, 3 m/s air flow.		69.9	°C/W
	$\theta_{JA5}$	Junction to air, 5 m/s air flow.		67.3	°C/W

**Table 6. Thermal Characteristics for 16-pin devices (ePAD soldered to board)**

Parameter	Symbol	Conditions	Package	Typical Values	Unit
Thermal Resistance (devices with external crystal)	$\theta_{JC}$	Junction to case.	LTG16	66	°C/W
	$\theta_{Jb}$	Junction to base.		5.1	°C/W
	$\theta_{JA0}$	Junction to air, still air.		63	°C/W
	$\theta_{JA1}$	Junction to air, 1 m/s air flow.		56	°C/W
	$\theta_{JA3}$	Junction to air, 3 m/s air flow.		51	°C/W
	$\theta_{JA5}$	Junction to air, 5 m/s air flow.		49	°C/W
Thermal Resistance Q-series (devices with internal crystal)	$\theta_{JC}$	Junction to case.	LTG16	82.1	°C/W
	$\theta_{Jb}$	Junction to base.		42.3	°C/W
	$\theta_{JA0}$	Junction to air, still air.		93.6	°C/W
	$\theta_{JA1}$	Junction to air, 1 m/s air flow.		87.1	°C/W
	$\theta_{JA3}$	Junction to air, 3 m/s air flow.		83.3	°C/W

## Recommended Operating Conditions

**Table 7. Recommended Operating Conditions**

Use filtered analog power supply, if available, for  $V_{DDA}$ .

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$V_{DD0x}$ ,	1.8V power supply voltage.	1.71	1.8	1.89	V
$V_{DDD}$ ,	2.5V power supply voltage.	2.375	2.5	2.625	V
$V_{DDA}$	3.3V power supply voltage.	3.135	3.3	3.465	V
$T_A$	Ambient operating temperature, standard product.	-40	-	+85	°C
	Ambient operating temperature, automotive device (9FGV1002CnnnNBG2).	-40	-	+105	°C
$C_L$	Maximum load capacitance (3.3V LVCMOS only).	-	-	15	pF
$t_{PU}$	Power-up time for all $V_{DDs}$ to reach minimum specified voltage (power ramps must be monotonic).	0.05	-	5	ms

## Electrical Characteristics

$V_{DDX} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$ ,  $1.8V \pm 5\%$ ,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$  and  $-40^{\circ}C$  to  $+105^{\circ}C$  unless noted otherwise.

**Table 8. Common Electrical Characteristics**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Input Frequency	$f_{IN}$	Crystal input frequency.	8	-	50	MHz	1
		CLKIN input frequency.	1	-	240	MHz	5
Output Frequency	$f_{OUT}$	Differential clock output (LVDS/LP-HCSL).	1	-	325	MHz	-
		Single-ended clock output (LVCMOS).	1	-	200	MHz	-
VCO Frequency	$f_{VCO}$	VCO operating frequency range.	2400	2500	2600	MHz	-
Loop Bandwidth	$f_{BW}$	Input frequency = 25MHz.	0.06	-	0.9	MHz	-
Input High Voltage	$V_{IH}$	SEL[1:0], OE[B:A].	$0.7 \times V_{DDD}$	-	$V_{DDD} + 0.3$	V	-
Input Low Voltage	$V_{IL}$	SEL[1:0], OE[B:A].	GND - 0.3	-	0.8	V	-
Input High Voltage	$V_{IH}$	REF/SEL_I2C#.	$0.65 \times V_{DDREF}$	-	$V_{DDREF} + 0.3$	V	-
Input Low Voltage	$V_{IL}$	REF/SEL_I2C#.	-0.3	-	0.4	V	-
Input High Voltage	$V_{IH}$	XIN/CLKIN.	0.8	-	1.2	V	-
		XIN/CLKIN.	-0.3	-	0.4	V	-
Input Rise/Fall Time	$T_R/T_F$	OEA, OEB (when present)	-	-	10	ns	-
		SEL1/SDA, SEL0/SCL	-	-	300		-
Input Capacitance	$C_{IN}$	SEL[1:0].	-	3	7	pF	-
Internal Pull-up Resistor	$R_{UP}$		165	229	320	k $\Omega$	-
Internal Pull-down Resistor	$R_{DOWN}$		150	212	290	k $\Omega$	-
Programmable Capacitance at XIN and XO (XIN in parallel with XO)	$C_L$	XIN/CLKIN, XO.	0	-	8	pF	-
Input Duty Cycle	$t_2$	CLKIN, measured at $V_{DDREF}/2$ .	40	50	60	%	-
Output Duty Cycle	$t_3$	LVCMOS, $f_{OUT} > 156.25MHz$ .	40	50	60	%	-
		LVCMOS, $f_{OUT} \leq 156.25MHz$ .	45	50	55	%	-
		LVDS, LP-HCSL outputs.	45	50.2	55	%	-
Clock Jitter (-40°C to +85°C)	$t_6$	Cycle-to-cycle jitter (Peak-to-Peak), See <a href="#">Test Frequencies for Jitter Measurements</a> for configurations.	-	24	-	ps	4
		Reference clock RMS phase jitter (12kHz to 20MHz integration range). See <a href="#">Test Frequencies for Jitter Measurements</a> for configurations.	-	245	-	fs rms	4
		OUTx RMS phase jitter(12kHz to 20MHz integration range) differential output. See <a href="#">Test Frequencies for Jitter Measurements</a> for configurations.	-	276	-	fs rms	4

**Table 8. Common Electrical Characteristics (Cont.)**

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Clock Jitter (-40°C to +105°C)	t6	Cycle-to-cycle jitter (Peak-to-Peak), See <a href="#">Test Frequencies for Jitter Measurements</a> for configurations.	-	35	-	ps	4
		Reference clock RMS phase jitter (12kHz to 20MHz integration range). See <a href="#">Test Frequencies for Jitter Measurements</a> for configurations.	-	287	-	fs rms	4
		OUTx RMS phase jitter(12kHz to 20MHz integration range) differential output. See <a href="#">Test Frequencies for Jitter Measurements</a> for configurations.	-	355	-	fs rms	4
Output Skew - 9FGV1006C (-40°C to +85°C)	t7	All outputs using the same driver format same V <sub>DDO</sub> voltage.	-	38	60	ps	-
Output skew - 9FGV1002C (-40°C to +85°C)	t7	All outputs using the same driver format and same V <sub>DDO</sub> voltage.	-	62	100		-
Output skew - 9FGV1002C (-40°C to +105°C)			-	62	120		
Lock Time	t8a	PLL outputs valid from V <sub>DDs</sub> reaching 1.5V.	-	5	10	ms	2,3
	t8b	REF outputs valid from V <sub>DDs</sub> reaching 1.5V.	-	5	11	ms	2,3

<sup>1</sup> Practical lower frequency is determined by loop filter settings.

<sup>2</sup> Includes loading the configuration bits from OTP to registers. This time also applies when changing configuration select.

<sup>3</sup> Actual PLL lock time depends on the loop configuration.

<sup>4</sup> Actual jitter is configuration dependent. These values are representative of what the device can achieve.

<sup>5</sup> Input doubler off. Maximum input frequency with input doubler on is 160MHz.

**Table 9. Test Frequencies for Jitter Measurements**

V<sub>DDx</sub> = 3.3V±5%, 2.5V±5%, 1.8V±5%, T<sub>AMB</sub> = -40°C to +85°C and -40°C to +105°C unless noted otherwise.

XIN/CLKIN	OUT0	OUT1	OUT2	OUT3	Unit	Notes
50	156.25				MHZ	3,4
	100				MHZ	1,2,3

<sup>1</sup> This configuration is used for 12kHz–20MHz REF phase jitter measurement, SSC off.

<sup>2</sup> This configuration is used for PCIe filtered phase jitter measurements with SSC on and off.

<sup>3</sup> Outputs configured as LP-HCSL or LVDS with REF output off, unless noted.

<sup>4</sup> This configuration is used for 12kHz–20MHz OUT phase jitter measurement. REF off, SSC off.

**Table 10. LVC MOS Output Electrical Characteristics -40°C to +85°C**

$V_{DDx} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$ .

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Slew Rate	$S_R$	3.3V $\pm 5\%$ , 20% to 80% of $V_{DDO}$ (output load = 4.7pF).	2.6	3.7	4.7	V/ns	-
		2.5V $\pm 5\%$ , 20% to 80% of $V_{DDO}$ (output load = 4.7pF).	1.5	2.4	4.7		-
		1.8V $\pm 5\%$ , 20% to 80% of $V_{DDO}$ (output load = 4.7pF).	1.0	1.7	3.2		-
Output High Voltage	$V_{OH}$	$I_{OH} = -15mA$ at 3.3V.	$0.8 \times V_{DDO}$	-	$V_{DDO}$	V	-
		$I_{OH} = -12mA$ at 2.5V.					-
		$I_{OH} = -8mA$ at 1.8V.					-
Output Low Voltage	$V_{OL}$	$I_{OL} = 15mA$ at 3.3V.	-	0.22	0.4	V	-
		$I_{OL} = 12mA$ at 2.5V.					-
		$I_{OL} = 8mA$ at 1.8V.					-
Output Leakage Current	$I_{OZDD}$	Outputs, tri-stated, $V_{DDO}, V_{DDREF} = 3.465V$ .	-	0	5	$\mu A$	-
CMOS Output Driver Impedance	$R_{OUT}$	$T_A = 25^\circ C$ .	-	17	-	$\Omega$	-

**Table 11. LVC MOS Output Electrical Characteristics -40°C to +105°C**

$V_{DDx} = 3.3V \pm 5\%, 2.5V \pm 5\%, 1.8V \pm 5\%$ .

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Slew Rate	$S_R$	3.3V $\pm 5\%$ , 20% to 80% of $V_{DDO}$ (output load = 4.7pF).	2.5	3.4	4.6	V/ns	-
		2.5V $\pm 5\%$ , 20% to 80% of $V_{DDO}$ (output load = 4.7pF).	1.5	2.4	4.6		-
		1.8V $\pm 5\%$ , 20% to 80% of $V_{DDO}$ (output load = 4.7pF).	0.9	1.7	2.6		-
Output High Voltage	$V_{OH}$	$I_{OH} = -15mA$ at 3.3V.	$0.75 \times V_{DDO}$	-	$V_{DDO}$	V	-
		$I_{OH} = -12mA$ at 2.5V.					-
		$I_{OH} = -8mA$ at 1.8V.					-
Output Low Voltage	$V_{OL}$	$I_{OL} = 15mA$ at 3.3V.	-	0.24	0.5	V	-
		$I_{OL} = 12mA$ at 2.5V.					-
		$I_{OL} = 8mA$ at 1.8V.					-
Output Leakage Current	$I_{OZDD}$	Outputs, tri-stated, $V_{DDO}, V_{DDREF} = 3.465V$ .	-	0	5	$\mu A$	-
CMOS Output Driver Impedance	$R_{OUT}$	$T_A = 25^\circ C$ .	-	17	-	$\Omega$	-

**Table 12. LVDS Output Electrical Characteristics**

$V_{DDO} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$ ,  $1.8V \pm 5\%$ ,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$  and  $-40^{\circ}C$  to  $+105^{\circ}C$  unless noted otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
Differential Output Voltage for the TRUE Binary State	$V_{OT (+)}$	-	247	328	454	mV	-
Differential Output Voltage for the FALSE Binary State	$V_{OT (-)}$	-	-454	-332	-247	mV	-
Change in $V_{OT}$ between Complementary Output States	$\Delta V_{OT}$	-	-	-	50	mV	-
Output Common Mode Voltage (Offset Voltage)	$V_{OS}$	$V_{DDO} = 2.5V \pm 5\%$ or $3.3V \pm 5\%$	1.125	1.19	1.55	V	-
Output Common Mode Voltage (Offset Voltage)	$V_{OS}$	$V_{DDO} = 1.8V \pm 5\%$	0.8	0.9	0.95	V	-
Change in $V_{OS}$ between Complementary Output States	$\Delta V_{OS}$	-	-	-	50	mV	-
Outputs Short Circuit Current, $V_{OUT+}$ or $V_{OUT-} = 0V$ or $V_{DD}$	$I_{OS}$	-	-	6	12	mA	-
Differential Outputs Short Circuit Current, $V_{OUT+} = V_{OUT-}$	$I_{OSD}$	-	-	3	12	mA	-
Rise Times Tested at 20% – 80%	$T_R$	-40°C to +85°C	-	257	375	ps	-
Fall Times Tested at 80% – 20%	$T_F$		-	287	375	ps	-
Rise Times Tested at 20% – 80%	$T_R$	-40°C to +105°C	-	315	400	ps	-
Fall Times Tested at 80% – 20%	$T_F$		-	332	400	ps	-

**Table 13. Low-Power (LP) Push-Pull HCSL Differential Outputs**

V<sub>DDO</sub> = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T<sub>AMB</sub> = -40°C to +85°C and -40°C to +105°C unless noted otherwise. See [Test Loads](#).

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limit	Unit	Notes
Slew Rate	T <sub>R/F</sub>	Scope averaging on.	1.25	2.5	4	1 to 4	V/ns	2,3,16
Slew Rate Matching	ΔT <sub>R/F</sub>	-	-	9	20	20	%	1,14,16
Crossing Voltage (abs)	V <sub>CROSS</sub>	Scope averaging off.	250	424	550	250 to 550	mV	1,4,5,16
Crossing Voltage (var)	ΔV <sub>CROSS</sub>	Scope averaging off.	-	16	50	140	mV	1,4,9,16
Average Clock Period Accuracy	T <sub>PERIOD_AVG</sub>	Outputs set to 100MHz for PCIe applications.	-100	0	+2600	-100 to +2600	-	2,10,12,13
Absolute Period	T <sub>PERIOD_ABS</sub>	Includes jitter and spread modulation.	9.998	10	10.06	9.949 to 10.101	-	2,6
Absolute Maximum Output Voltage	V <sub>MAX</sub>	-	-	-	888	1150	mV	1,7,15
Absolute Minimum Output Voltage	V <sub>MIN</sub>	-	-148	-	-	-300	mV	1,8,15
Output Voltage Swing	V <sub>SWING</sub>	V <sub>DDO</sub> = 3.3V ± 5%	1320	1520	1720	MIN = 300mV	mV	2
		V <sub>DDO</sub> = 2.5V ± 5%	1260	1460	1660			
		V <sub>DDO</sub> = 1.8V ± 5%	1180	1380	1560			

<sup>1</sup> Measured from single-ended waveform.

<sup>2</sup> Measured from differential waveform.

<sup>3</sup> Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

<sup>4</sup> Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

<sup>5</sup> Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

<sup>6</sup> Defined as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation.

<sup>7</sup> Defined as the maximum instantaneous voltage including overshoot.

<sup>8</sup> Defined as the minimum instantaneous voltage including undershoot.

<sup>9</sup> Defined as the total variation of all crossing voltages of rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in V<sub>CROSS</sub> for any particular system.

<sup>10</sup> Refer to Section 8.6 of the PCI Express Base Specification, Revision 6.0 for information regarding PPM considerations.

<sup>11</sup> System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load C<sub>L</sub> = 2pF.

<sup>12</sup> PCIe Gen1 through Gen4 specify ±300ppm frequency tolerances. The PhiClock devices already meet the tighter ±100ppm frequency tolerances for PCIe Gen5 and Gen6.

<sup>13</sup> "ppm" refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of 100Hz/ppm × 100ppm = 10kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±100ppm applies to systems that do not employ Spread Spectrum clocking, or that use common clock source. For systems employing Spread Spectrum Clocking, there is an additional 2,500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600ppm for Common Clock architectures. Separate Reference Clock architectures may have a lower allowed spread percentage.

<sup>14</sup> Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a  $\pm 75\text{mV}$  window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of REFCLK+ should be compared to the fall edge rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

<sup>15</sup> At default amplitude settings.

<sup>16</sup> Confirmed by design and characterization.

**Table 14. PCIe REFCLK Phase Jitter - 2.5V/3.3V Operation**

Supply Voltages = 2.5V/3.3V  $\pm 5\%$ ,  $T_{\text{AMB}}$  = -40°C to +85°C and -40°C to +105°C. See [Test Loads](#).

Parameter	Symbol	Conditions	Typical	Maximum	Specification Limits	Unit	Notes
PCIe Gen1 (2.5 GT/s)	$t_{\text{jph}}\text{PCIeG1-CC}$	Common Clocked Architecture SSC = 0.0% (off)	3,290	9,867	86,000	fs pk-pk	1, 2, 8
PCIe Gen2 Hi-Band (5.0 GT/s)	$t_{\text{jph}}\text{PCIeG2-CC}$		164	462	3,000	fs RMS	1, 2, 8
PCIe Gen2 Lo-Band (5.0 GT/s)			46	72	3,100	fs RMS	1, 2, 8
PCIe Gen3 (8.0 GT/s)	$t_{\text{jph}}\text{PCIeG3-CC}$		93	279	1,000	fs RMS	1, 2, 8
PCIe Gen4 (16.0 GT/s)	$t_{\text{jph}}\text{PCIeG4-CC}$		93	279	500	fs RMS	1, 2, 3, 4, 8
PCIe Gen5 (32.0 GT/s)	$t_{\text{jph}}\text{PCIeG5-CC}$		39	119	150	fs RMS	1, 2, 3, 5, 8
PCIe Gen6 (64.0 GT/s)	$t_{\text{jph}}\text{PCIeG6-CC}$		21	64	100	fs RMS	1, 2, 3, 6, 8
PCIe Gen1 (2.5 GT/s)	$t_{\text{jph}}\text{PCIeG1-CC}$	Common Clocked Architecture SSC = -0.3% or -0.5%.	6,304	9,869	86,000	fs pk-pk	1, 2, 8
PCIe Gen2 Hi-Band (5.0 GT/s)	$t_{\text{jph}}\text{PCIeG2-CC}$		235	345	3,000	fs RMS	1, 2, 8
PCIe Gen2 Lo-Band (5.0 GT/s)			227	422	3,100	fs RMS	1, 2, 8
PCIe Gen3 (8.0 GT/s)	$t_{\text{jph}}\text{PCIeG3-CC}$		139	234	1,000	fs RMS	1, 2, 8
PCIe Gen4 (16.0 GT/s)	$t_{\text{jph}}\text{PCIeG4-CC}$		139	234	500	fs RMS	1, 2, 3, 4, 8
PCIe Gen5 (32.0 GT/s)	$t_{\text{jph}}\text{PCIeG5-CC}$		49	96	150	fs RMS	1, 2, 3, 5, 8
PCIe Gen6 (64.0 GT/s)	$t_{\text{jph}}\text{PCIeG6-CC}$		31	53	100	fs RMS	1, 2, 3, 6, 8
PCIe Gen2 IR (5.0 GT/s)	$t_{\text{jph}}\text{PCIeG2-IR}$	IR (SRNS) Architecture SSC = 0%	176	381	N/A	fs RMS	1, 2, 7, 8
PCIe Gen3 IR (8.0 GT/s)	$t_{\text{jph}}\text{PCIeG3-IR}$		54	111		fs RMS	1, 2, 7, 8
PCIe Gen4 IR (16.0 GT/s)	$t_{\text{jph}}\text{PCIeG4-IR}$		55	113		fs RMS	1, 2, 7, 8
PCIe Gen5 IR (32.0 GT/s)	$t_{\text{jph}}\text{PCIeG5-IR}$		55	160		fs RMS	1, 2, 7, 8
PCIe Gen6 IR (64.0 GT/s)	$t_{\text{jph}}\text{PCIeG6-IR}$		58	154		fs RMS	1, 2, 7, 8
PCIe Gen2 IR (5.0 GT/s)	$t_{\text{jph}}\text{PCIeG2-IR}$	IR (SRIS) Architecture SSC = -0.1%, -0.3% or -0.5%.	1,017	1,510	N/A	fs RMS	1, 2, 7, 8
PCIe Gen3 IR (8.0 GT/s)	$t_{\text{jph}}\text{PCIeG3-IR}$		403	578		fs RMS	1, 2, 7, 8
PCIe Gen4 IR (16.0 GT/s)	$t_{\text{jph}}\text{PCIeG4-IR}$		318	435		fs RMS	1, 2, 7, 8
PCIe Gen5 IR (32.0 GT/s)	$t_{\text{jph}}\text{PCIeG5-IR}$	IR (SRIS) Architecture SSC = -0.1% or -0.3%	115	192	N/A	fs RMS	1, 2, 7, 8
PCIe Gen6 IR (64.0 GT/s)	$t_{\text{jph}}\text{PCIeG6-IR}$		121	225		fs RMS	1, 2, 7, 8

<sup>1</sup> The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 6.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.

<sup>2</sup> Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for



RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

- <sup>3</sup> SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
- <sup>4</sup> Note that 700fs RMS is to be used in channel simulations to account for additional noise in a real system.
- <sup>5</sup> Note that 250fs RMS is to be used in channel simulations to account for additional noise in a real system.
- <sup>6</sup> Note that 150fs RMS is to be used in channel simulations to account for additional noise in a real system.
- <sup>7</sup> While the PCI Express Base Specification 6.0, Revision 1.0 provides the filters necessary to calculate IR jitter values, it does not provide specification limits, hence the N/A in the Limit column. IR values are informative only. IR is not defined for PCIe Gen1.
- <sup>8</sup> 9FGV1002C or 9FGV1006C with 001, 015, Q505 or Q515 configurations. See the [9FGV1002C/9FGV1006C Standard Configurations](#) table for details and a selection of off-the-shelf configurations supporting PCIe Gen6.

**Table 15. PCIe Refclk Phase Jitter – 1.8V Operation**

Supply Voltages = 1.8V ±5%, T<sub>AMB</sub> = -40°C to +85°C and -40°C to +105°C. See [Test Loads](#).

Parameter	Symbol	Conditions	Typical	Maximum	Specification Limits	Unit	Notes
PCIe Gen1 (2.5 GT/s)	t <sub>jph</sub> PCIeG1-CC	Common Clocked Architecture SSC = 0.0% (off)	4,024	10,332	86,000	fs pk-pk	1, 2, 8
PCIe Gen2 Hi-Band (5.0 GT/s)	t <sub>jph</sub> PCIeG2-CC		206	481	3,000	fs RMS	1, 2, 8
PCIe Gen2 Lo-Band (5.0 GT/s)			52	79	3,100	fs RMS	1, 2, 8
PCIe Gen3 (8.0 GT/s)	t <sub>jph</sub> PCIeG3-CC		114	291	1,000	fs RMS	1, 2, 8
PCIe Gen4 (16.0 GT/s)	t <sub>jph</sub> PCIeG4-CC		114	291	500	fs RMS	1, 2, 3, 4, 8
PCIe Gen5 (32.0 GT/s)	t <sub>jph</sub> PCIeG5-CC		47	125	150	fs RMS	1, 2, 3, 5, 8
PCIe Gen6 (64.0 GT/s)	t <sub>jph</sub> PCIeG6-CC		26	67	100	fs RMS	1, 2, 3, 6, 8
PCIe Gen1 (2.5 GT/s)	t <sub>jph</sub> PCIeG1-CC	Common Clocked Architecture SSC = -0.3% or -0.5%.	5,417	9,379	86,000	fs pk-pk	1, 2, 8
PCIe Gen2 Hi-Band (5.0 GT/s)	t <sub>jph</sub> PCIeG2-CC		231	318	3,000	fs RMS	1, 2, 8
PCIe Gen2 Lo-Band (5.0 GT/s)			184	443	3,100	fs RMS	1, 2, 8
PCIe Gen3 (8.0 GT/s)	t <sub>jph</sub> PCIeG3-CC		129	253	1,000	fs RMS	1, 2, 8
PCIe Gen4 (16.0 GT/s)	t <sub>jph</sub> PCIeG4-CC		129	253	500	fs RMS	1, 2, 3, 4, 8
PCIe Gen5 (32.0 GT/s)	t <sub>jph</sub> PCIeG5-CC		49	109	150	fs RMS	1, 2, 3, 5, 8
PCIe Gen6 (64.0 GT/s)	t <sub>jph</sub> PCIeG6-CC		29	59	100	fs RMS	1, 2, 3, 6, 8
PCIe Gen2 IR (5.0 GT/s)	t <sub>jph</sub> PCIeG2-IR	IR (SRNS) Architecture SSC = 0%	226	407	N/A	fs RMS	1, 2, 7, 8
PCIe Gen3 IR (8.0 GT/s)	t <sub>jph</sub> PCIeG3-IR		65	118		fs RMS	1, 2, 7, 8
PCIe Gen4 IR (16.0 GT/s)	t <sub>jph</sub> PCIeG4-IR		67	120		fs RMS	1, 2, 7, 8
PCIe Gen5 IR (32.0 GT/s)	t <sub>jph</sub> PCIeG5-IR		68	167		fs RMS	1, 2, 7, 8
PCIe Gen6 IR (64.0 GT/s)	t <sub>jph</sub> PCIeG6-IR		74	161		fs RMS	1, 2, 7, 8

**Table 15. PCIe Refclk Phase Jitter – 1.8V Operation (Cont.)**

Supply Voltages = 1.8V ±5%, T<sub>AMB</sub> = -40°C to +85°C and -40°C to +105°C. See [Test Loads](#).

Parameter	Symbol	Conditions	Typical	Maximum	Specification Limits	Unit	Notes
PCIe Gen2 IR (5.0 GT/s)	t <sub>jphPCIeG2-IR</sub>	IR (SRIS) Architecture SSC = -0.1%, -0.3% or -0.5%.	956	1,477	N/A	fs RMS	1, 2, 7, 8
PCIe Gen3 IR (8.0 GT/s)	t <sub>jphPCIeG3-IR</sub>		375	571		fs RMS	1, 2, 7, 8
PCIe Gen4 IR (16.0 GT/s)	t <sub>jphPCIeG4-IR</sub>		283	415		fs RMS	1, 2, 7, 8
PCIe Gen5 IR (32.0 GT/s)	t <sub>jphPCIeG5-IR</sub>	IR (SRIS) Architecture	107	180		fs RMS	1, 2, 7, 8
PCIe Gen6 IR (64.0 GT/s)	t <sub>jphPCIeG6-IR</sub>	SSC = -0.1% or -0.3%	111	193		fs RMS	1, 2, 7, 8

<sup>1</sup> The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 6.0, Revision 1.0. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.

<sup>2</sup> Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

<sup>3</sup> SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

<sup>4</sup> Note that 700fs RMS is to be used in channel simulations to account for additional noise in a real system.

<sup>5</sup> Note that 250fs RMS is to be used in channel simulations to account for additional noise in a real system.

<sup>6</sup> Note that 150fs RMS is to be used in channel simulations to account for additional noise in a real system.

<sup>7</sup> While the PCI Express Base Specification 6.0, Revision 1.0 provides the filters necessary to calculate IR jitter values, it does not provide specification limits, hence the N/A in the Limit column. IR values are informative only. IR is not defined for PCIe Gen1.

<sup>8</sup> 9FGV1002C or 9FGV1006C with 002 or Q506 configurations. See the [9FGV1002C/9FGV1006C Standard Configurations](#) table for details and a selection of off-the-shelf configurations supporting PCIe Gen6.

**Table 16. 9FGV1002C Current Consumption -40°C to +85°C**

Supply Voltages = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
V <sub>DDREF</sub> Supply Current	I <sub>DDREF</sub>	50MHz REFCL, subtract 3mA for 25MHz REFCLK.	-	7	11	mA	-
Core Supply Current	I <sub>DDCORE</sub>	2400MHz VCO.	-	37	49	mA	3
Output Buffer Supply Current V <sub>DDO3</sub>	I <sub>DDOx</sub>	LVDS, 325MHz.	-	6	9	mA	2
		LP-HCSL, 100MHz.	-	6	7	mA	2
		LVC MOS, 50MHz.	-	4	6	mA	1, 2
		LVC MOS, 200MHz.	-	12	21	mA	1, 2
Output Buffer Supply Current V <sub>DDO2</sub> (includes output divider)		LVDS, 325MHz.	-	17	24	mA	2
		LP-HCSL, 100MHz.	-	16	20	mA	2
		LVC MOS, 50MHz.	-	14	18	mA	1, 2
		LVC MOS, 200MHz.	-	23	35	mA	1, 2
Output Buffer Supply Current V <sub>DDO1</sub> (this pin must be connected if OUT0 is used)		LVDS, 325MHz.	-	13	20	mA	2
		LP-HCSL, 100MHz.	-	7	13	mA	2
		LVC MOS, 50MHz.	-	4	14	mA	1, 2
		LVC MOS, 200MHz.	-	13	22	mA	1, 2
Output Buffer Supply Current V <sub>DDO0</sub>	LVDS, 325MHz.	-	6	9	mA	2	
	LP-HCSL, 100MHz.	-	6	7	mA	2	
	LVC MOS, 50MHz.	-	4	6	mA	1, 2	
	LVC MOS, 200MHz.	-	12	22	mA	1, 2	
Total Power Down Current	I <sub>DDPD</sub>	Programmable outputs in HCSL mode, B37[0] = 0.	-	20	27	mA	2
		Programmable outputs in LVDS mode, B37[0] = 0.	-	33	45	mA	2
		Programmable outputs in LVC MOS1 mode, B37[0] = 0.	-	16	22	mA	2

<sup>1</sup> Single CMOS driver active for each output pair.

<sup>2</sup> See [Test Loads](#) for details.

<sup>3</sup> I<sub>DDCORE</sub> = I<sub>DDA</sub> + I<sub>DD</sub>. For integer, fractional or spread spectrum PLL.

**Table 17. 9FGV1002C Current Consumption -40°C to +105°C**

Supply Voltages = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
V <sub>DDREF</sub> Supply Current	I <sub>DDREF</sub>	50MHz REFCL, subtract 3mA for 25MHz REFCLK.	-	7	11	mA	-
Core Supply Current	I <sub>DDCORE</sub>	2400MHz VCO.	-	43	49	mA	3
Output Buffer Supply Current V <sub>DDO3</sub>	I <sub>DDOx</sub>	LVDS, 325MHz.	-	6	9	mA	2
		LP-HCSL, 100MHz.	-	6	7	mA	2
		LVC MOS, 50MHz.	-	4	6	mA	1, 2
		LVC MOS, 200MHz.	-	12	21	mA	1, 2
Output Buffer Supply Current V <sub>DDO2</sub> (includes output divider)		LVDS, 325MHz.	-	17	24	mA	2
		LP-HCSL, 100MHz.	-	16	20	mA	2
		LVC MOS, 50MHz.	-	14	18	mA	1, 2
		LVC MOS, 200MHz.	-	23	35	mA	1, 2
Output Buffer Supply Current V <sub>DDO1</sub> (this pin must be connected if OUT0 is used)		LVDS, 325MHz.	-	13	20	mA	2
		LP-HCSL, 100MHz.	-	7	13	mA	2
		LVC MOS, 50MHz.	-	4	14	mA	1, 2
		LVC MOS, 200MHz.	-	13	22	mA	1, 2
Output Buffer Supply Current V <sub>DDO0</sub>	LVDS, 325MHz.	-	6	9	mA	2	
	LP-HCSL, 100MHz.	-	6	7	mA	2	
	LVC MOS, 50MHz.	-	4	6	mA	1, 2	
	LVC MOS, 200MHz.	-	12	22	mA	1, 2	
Total Power Down Current	I <sub>DDPD</sub>	Programmable outputs in HCSL mode, B37[0] = 0.	-	21	27	mA	2
		Programmable outputs in LVDS mode, B37[0] = 0.	-	33	45	mA	2
		Programmable outputs in LVC MOS1 mode, B37[0] = 0.	-	20	27	mA	2

<sup>1</sup> Single CMOS driver active for each output pair.

<sup>2</sup> See [Test Loads](#) for details.

<sup>3</sup> I<sub>DDCORE</sub> = I<sub>DDA</sub> + I<sub>DD</sub>. For integer, fractional or spread spectrum PLL.

**Table 18. 9FGV1006C Current Consumption -40°C to +85°C**

Supply Voltages = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit	Notes
V <sub>DDREF</sub> Supply Current	I <sub>DDREF</sub>	50MHz REFCLK.	-	3	7	mA	-
Core Supply Current	I <sub>DDCORE</sub>	2400MHz VCO.	-	37	48	mA	3
Output Buffer Supply Current (V <sub>DDO1</sub> )	I <sub>DDOx</sub>	LVDS, 350MHz.	-	19	24	mA	2
		LP-HCSL, 100MHz.	-	16	20	mA	2
		LVC MOS, 50MHz.	-	14	19	mA	1,2
		LVC MOS, 200MHz.	-	22	34	mA	1,2
Output Buffer Supply Current (V <sub>DDO0</sub> – the total for pins 9 and 10)	I <sub>DDOx</sub>	LVDS, 350MHz.	-	7	11	mA	2
		LP-HCSL, 100MHz.	-	8	10	mA	2
		LVC MOS, 50MHz.	-	8	13	mA	1,2
		LVC MOS, 200MHz.	-	8	14	mA	1,2
Total Power Down Current	I <sub>DDPD</sub>	Programmable outputs in HCSL mode, B37[0] = 0.	-	19	25	mA	2
		Programmable outputs in LVDS mode, B37[0] = 0.	-	25	34	mA	2
		Programmable outputs in LVC MOS1 mode, B37[0] = 0.	-	16	22	mA	2

<sup>1</sup> Single CMOS driver active for each output pair.

<sup>2</sup> See [Test Loads](#) for details.

<sup>3</sup> I<sub>DDCORE</sub> = I<sub>DDA</sub> + I<sub>DDD</sub> + I<sub>DDAO</sub>.

**Table 19. Spread Spectrum Generation Specifications**

V<sub>DDO</sub> = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T<sub>AMB</sub> = -40°C to +85°C and -40°C to +105°C unless noted otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Mod Frequency	f <sub>MODPCle</sub>	PCle Compliant -0.5% spread modulation.	30	31.5	33	kHz
Mod Frequency	f <sub>MOD</sub>	Modulation frequency.	30	31.5	63	kHz
Spread%	SSC%	Amount of spread value (programmable) – down spread.	-0.1	-0.5	-3.0	%
		Amount of spread value (programmable) – center spread.	±0.05	-	±1.5	

## I<sup>2</sup>C Bus Characteristics

**Table 20. I<sup>2</sup>C Bus DC Characteristics**

$V_{DDx} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$ ,  $1.8V \pm 5\%$ ,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$  and  $-40^{\circ}C$  to  $+105^{\circ}C$  unless noted otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input High Level	$V_{IH}$	-	$0.7 \times V_{DDD}$	-	-	V
Input Low Level	$V_{IL}$	-		-	$0.3 \times V_{DDD}$	V
Hysteresis of Inputs	$V_{HYS}$	-	$0.05 \times V_{DDD}$	-	-	V
Input Leakage Current	$I_{IN}$	-	12	-	25	$\mu A$
Output Low Voltage	$V_{OL}$	$I_{OL} = 3mA.$	-	-	0.4	V

**Table 21. I<sup>2</sup>C Bus AC Characteristics**

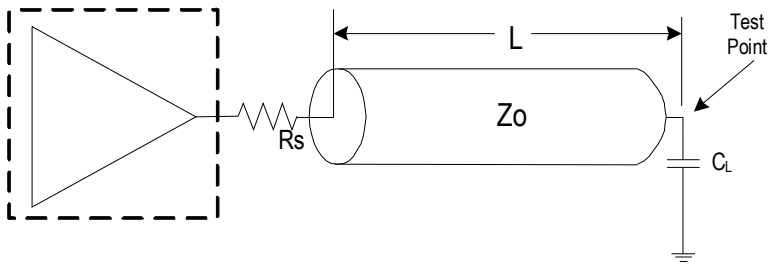
$V_{DDx} = 3.3V \pm 5\%$ ,  $2.5V \pm 5\%$ ,  $1.8V \pm 5\%$ ,  $T_{AMB} = -40^{\circ}C$  to  $+85^{\circ}C$  and  $-40^{\circ}C$  to  $+105^{\circ}C$  unless noted otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Serial Clock Frequency (SCL)	$F_{SCLK}$	-	10	-	400	kHz
Bus free time between STOP and START	$t_{BUF}$	-	1.3	-	-	$\mu s$
Setup Time, START	$t_{SU:START}$	-	0.6	-	-	$\mu s$
Hold Time, START	$t_{HD:START}$	-	0.6	-	-	$\mu s$
Setup Time, Data Input (SDA)	$t_{SU:DATA}$	-	0.1	-	-	$\mu s$
Hold Time, Data Input (SDA) 1	$t_{HD:DATA}$	-	0	-	-	$\mu s$
Output Data Valid from Clock	$t_{OVD}$	-	-	-	0.9	$\mu s$
Capacitive Load for Each Bus Line	$C_B$	-	-	-	400	pF
Rise Time, Data and Clock (SDA, SCL)	$t_R$	-	$20 + 0.1 \times C_B$	-	300	ns
Fall Time, Data and Clock (SDA, SCL)	$t_F$	-	$20 + 0.1 \times C_B$	-	300	ns
HIGH Time, Clock (SCL)	$t_{HIGH}$	-	0.6	-	-	$\mu s$
LOW Time, Clock (SCL)	$t_{LOW}$	-	1.3	-	-	$\mu s$
Setup Time, STOP	$t_{SU:STOP}$	-	0.6	-	-	$\mu s$

**Note:** A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the  $V_{IH(MIN)}$  of the SCL signal) to bridge the undefined region of the falling edge of SCL.

## Test Loads

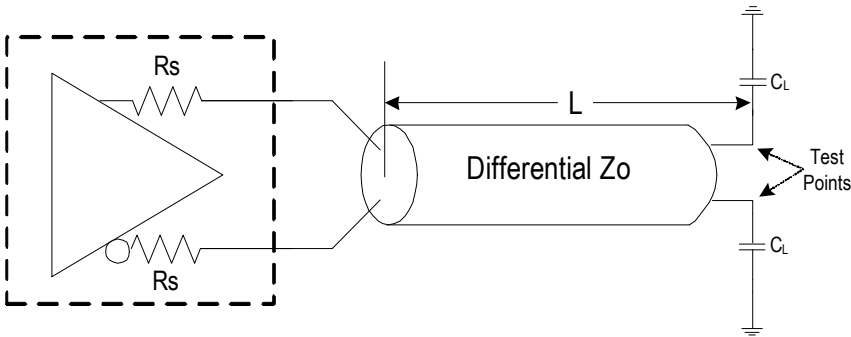
**Figure 5. LVCMOS AC/DC Test Load**



$R_s$	$Z_o$	L	$C_L$
33Ω	50Ω	5 inches	4.7pF

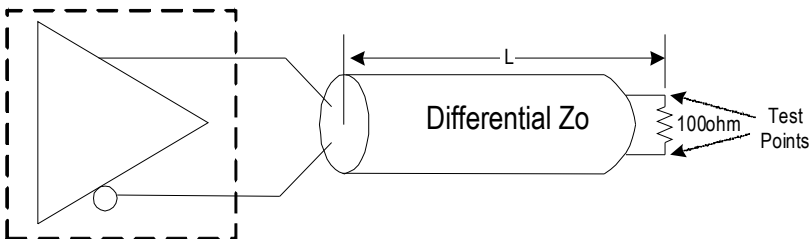
**Figure 6. LP-HCSL AC/DC Test Load**

(Standard PCIe source-terminated test load)



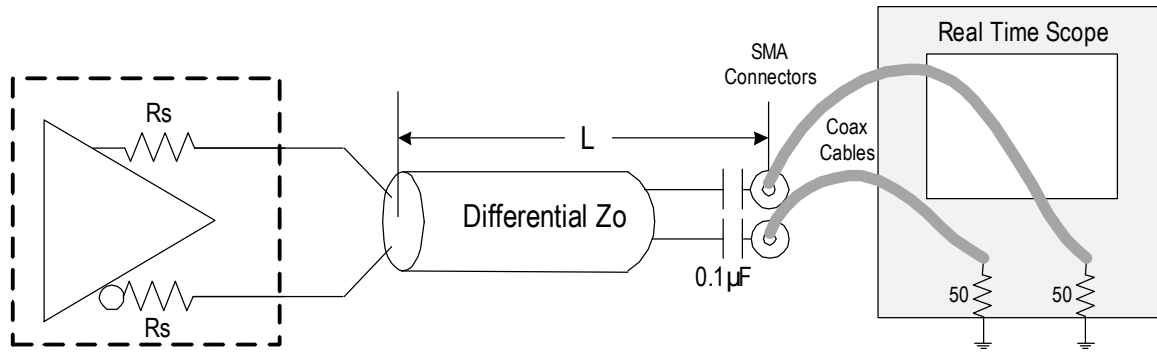
$R_s$	$Z_o$	L	$C_L$
Internal	100Ω	5 inches	2pF
Internal	85Ω	5 inches	2pF

**Figure 7. LVDS AC/DC Test Load**



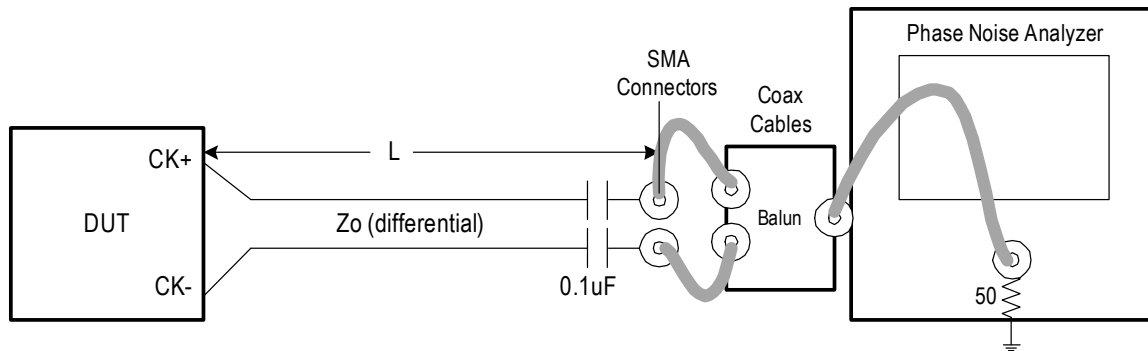
$R_s$	$Z_o$	L	$C_L$
N/A	100Ω	5 inches	N/A

**Figure 8. Test Setup for PCIe Measurement Using a Real-Time Scope**



$R_s$	$Z_o$	$L$	$C_L$
Internal	100Ω	5 inches	N/A

**Figure 9. Test Setup for PCIe Measurement Using a Phase Noise Analyzer**



$R_s$	$Z_o$	$L$	$C_L$
Internal	100Ω	5 inches	N/A



## Crystal Characteristics

**Table 22. Recommended Crystal Characteristics**

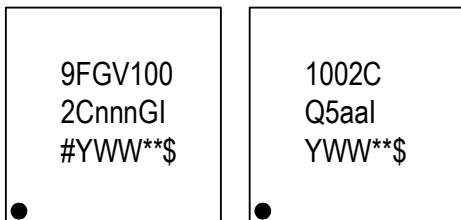
Parameter	Value	Unit
Frequency	8–50	MHz
Resonance Mode	Fundamental	-
Frequency Tolerance at 25°C	±20	ppm maximum
Frequency Stability, REF at 25°C Over Operating Temperature Range	±20	ppm maximum
Temperature Range (commercial)	0 to +70	°C
Temperature Range (industrial)	-40 to +85	°C
Temperature Range (automotive)	-40 to +105	°C
Equivalent Series Resistance (ESR)	50	Ω maximum
Shunt Capacitance (C <sub>O</sub> )	7	pF maximum
Load Capacitance (C <sub>L</sub> )	8	pF maximum
Drive Level	0.1	mW maximum
Aging Per Year	±5	ppm maximum

## Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

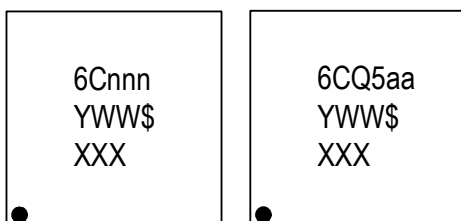
## Marking Diagrams

**Figure 10. 9FGV1002C Marking Diagrams**



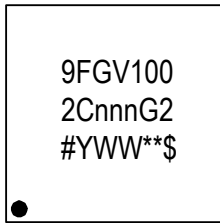
- Lines 1 and 2 are the truncated part number:
  - “nnn” denotes the decimal digits indicating a specific configuration.
  - “aa” denotes the alphanumeric digits indicating a specific Q5 configuration.
- Line 3:
  - “#” denotes the stepping number.
  - “YWW” denotes the last digits of the year and week the part was assembled.
  - “\*\*\*” denotes the lot sequence; “\$” denotes the mark code.

**Figure 11. 9FGV1006C Marking Diagrams**



- Line 1: truncated part number
  - “nnn” denotes the decimal digits indicating a specific configuration.
  - “aa” denotes the alphanumeric digits indicating a specific Q5 configuration.
- Line 2: “YWW” denotes the last digits of the year and week the part was assembled; “\$” denotes mark code.
- Line 3: “XXX” denotes the last three characters of the lot number.

**Figure 12. 9FGV1002C Marking Diagram - Automotive Device**



- Lines 1 and 2 are the truncated part number:
  - “nnn” denotes the decimal digits indicating a specific configuration..
- Line 3:
  - “#” denotes the stepping number.
  - “YWW” denotes the last digits of the year and week the part was assembled.
  - “\*\*” denotes the lot sequence; “\$” denotes the mark code.

## Standard Configurations

**Table 23. 9FGV1002C/9FGV1006C Standard Configurations**

Supply Voltage—all pins (V)	Output Impedance (ohms)	Number of PCIe Clock Outputs	XTAL Frequency (MHz)	Orderable Part Number (Bulk)	Orderable Part Number (Tape and Reel)
3.3	100	4	25 – external	9FGV1002C001NBGI	9FGV1002C001NBGI8
			50 – internal	9FGV1002CQ505LTGI	9FGV1002CQ505LTGI8
		2	25 – external	9FGV1006C001LTGI	9FGV1006C001LTGI8
			50 – internal	9FGV1006CQ505LTGI	9FGV1006CQ505LTGI8
	85	4	25 – external	9FGV1002C015NBGI	9FGV1002C015NBGI8
			50 – internal	9FGV1002CQ515LTGI	9FGV1002CQ515LTGI8
		2	25 – external	9FGV1006C015LTGI	9FGV1006C015LTGI8
			50 – internal	9FGV1006CQ515LTGI	9FGV1006CQ515LTGI8
1.8	100	4	25 – external	9FGV1002C002NBGI	9FGV1002C002NBGI8
			50 – internal	9FGV1002CQ506LTGI	9FGV1002CQ506LTGI8
		2	25 – external	9FGV1006C002LTGI	9FGV1006C002LTGI8
			50 – internal	9FGV1006CQ506LTGI	9FGV1006CQ506LTGI8

**Table 24. Common Features of 9FGV1002C/9FGV1006C Standard Configurations**

Output Freq (MHz)	Output Type	REF Outputs	Configuration	SSC amount (%)	CC	SRNS, SRIS
100	LP-HCSL	Off	0	0	PCIe Gen1–6	PCIe Gen1–6
			1	-0.1	PCIe Gen1–6	PCIe Gen1–6
			2	-0.3	PCIe Gen1–6	PCIe Gen1–6
			3	-0.5	PCIe Gen1–6	PCIe Gen1–4

## Ordering Information

Part Number	Package	Carrier Type	Temperature Range	Crystal
9FGV1002CnnnNBGI	4 × 4 mm, 0.5mm pitch <a href="#">24-VFQFPN</a>	Tray	-40 to +85°C	External
9FGV1002CnnnNBGI8	4 × 4 mm, 0.5mm pitch <a href="#">24-VFQFPN</a>	Tape and Reel	-40 to +85°C	External
9FGV1002CnnnNBG2	4 × 4 mm, 0.5mm pitch <a href="#">24-VFQFPN</a>	Tray	-40 to +105°C	External
9FGV1002CnnnNBG28	4 × 4 mm, 0.5mm pitch <a href="#">24-VFQFPN</a>	Tape and Reel	-40 to +105°C	External
9FGV1002CQ5aaLTGI	4 × 4 mm, 0.5mm pitch <a href="#">24-LGA</a>	Tray	-40 to +85°C	50MHz Internal
9FGV1002CQ5aaLTGI8	4 × 4 mm, 0.5mm pitch <a href="#">24-LGA</a>	Tape and Reel	-40 to +85°C	50MHz Internal
9FGV1006CnnnLTGI	3 × 3 mm, 0.5mm pitch <a href="#">16-LGA</a>	Tray	-40 to +85°C	External
9FGV1006CnnnLTGI8	3 × 3 mm, 0.5mm pitch <a href="#">16-LGA</a>	Tape and Reel	-40 to +85°C	External
9FGV1006CQ5aaLTGI	3 × 3 mm, 0.5mm pitch <a href="#">16-LGA</a>	Tray	-40 to +85°C	50MHz Internal
9FGV1006CQ5aaLTGI8	3 × 3 mm, 0.5mm pitch <a href="#">16-LGA</a>	Tape and Reel	-40 to +85°C	50MHz Internal

“G” indicates RoHS 6.6 compliance.

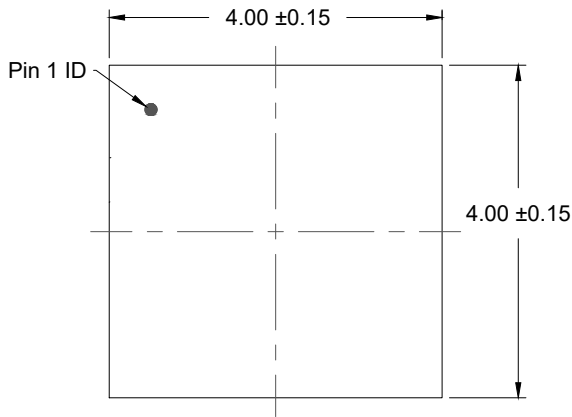
“nnn” are decimal digits indicating a specific configuration.

“aa” are alphanumeric digits indicating a specific configuration.

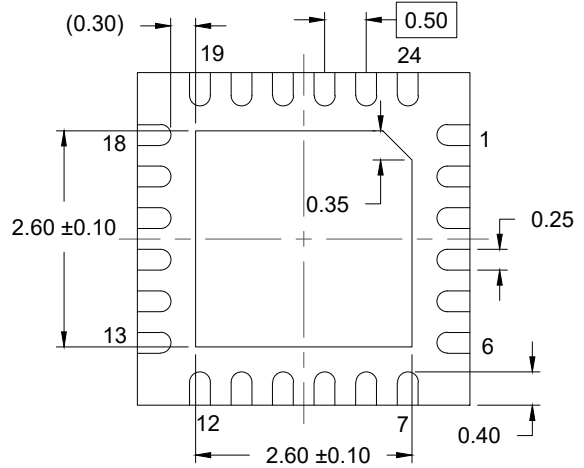
“Q5” indicates internal 50MHz crystal.

## Revision History

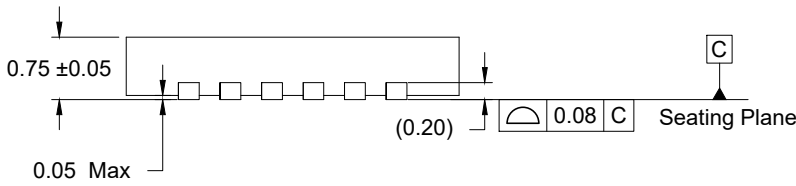
Revision Date	Description of Change
June 23, 2023	<ul style="list-style-type: none"> <li>▪ Added 9FGV1002nnnNBG2/8 automotive device to datasheet.</li> <li>▪ Updated front page text.</li> <li>▪ Updated existing electrical tables where necessary and added separate tables for -40°C to +105°C where necessary.</li> <li>▪ Added marking diagram and ordering information.</li> </ul>
March 29, 2023	Updated footnote 2 in <a href="#">Table 8</a> .
March 23, 2022	<ul style="list-style-type: none"> <li>▪ Separated PCIe Refclk Jitter table into separate 3.3V and 1.8V tables (<a href="#">Table 13</a> and <a href="#">Table 15</a>).</li> <li>▪ Updated both tables to show PCIe Gen6 support.</li> <li>▪ Minor updates to front page text.</li> </ul>
January 24, 2022	<ul style="list-style-type: none"> <li>▪ Typo correction: changed unit specification in <a href="#">Key Specifications</a> from 276ps to 276fs.</li> <li>▪ Updated <a href="#">Package Outline Drawings</a> section; moved package drawing links to <a href="#">Ordering Information</a>.</li> </ul>
November 30, 2020	Removed “Output Frequency” parameter from Spread Spectrum Generation Specifications table.
October 29, 2020	Updated pin descriptions for VDDAp and VDDDp.
October 9, 2020	Added a condition and values for REF outputs to the Lock Time parameter.
September 28, 2020	Removed “PCIe Gen5” from the standard configuration tables titles and the relative heading title.
August 18, 2020	Updated 9FGV1006CQ marking diagram.
August 14, 2020	Updated Slew Rate 1.8V minimum value from 0.8 to 1.0V/ns.
August 13, 2020	Updated Carrier Type in Ordering Information table from “Cut-Tape” to “Tray”.
July 16, 2020	Corrected internal resistors on SEL0/SCL and SEL1/SDA to be pull-downs.
July 10, 2020	Initial release.



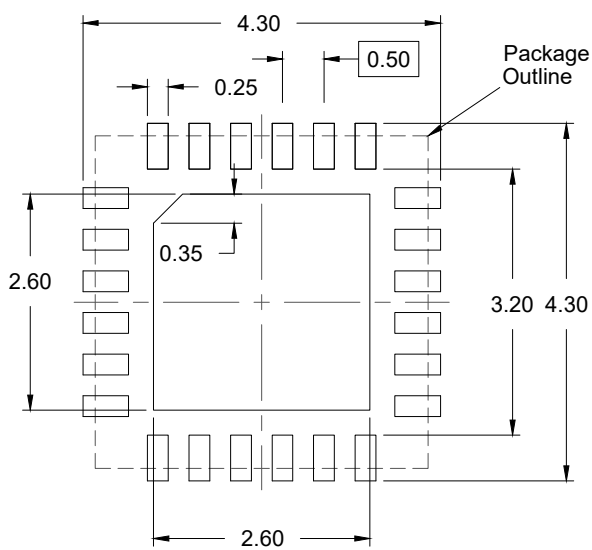
TOP VIEW



BOTTOM VIEW



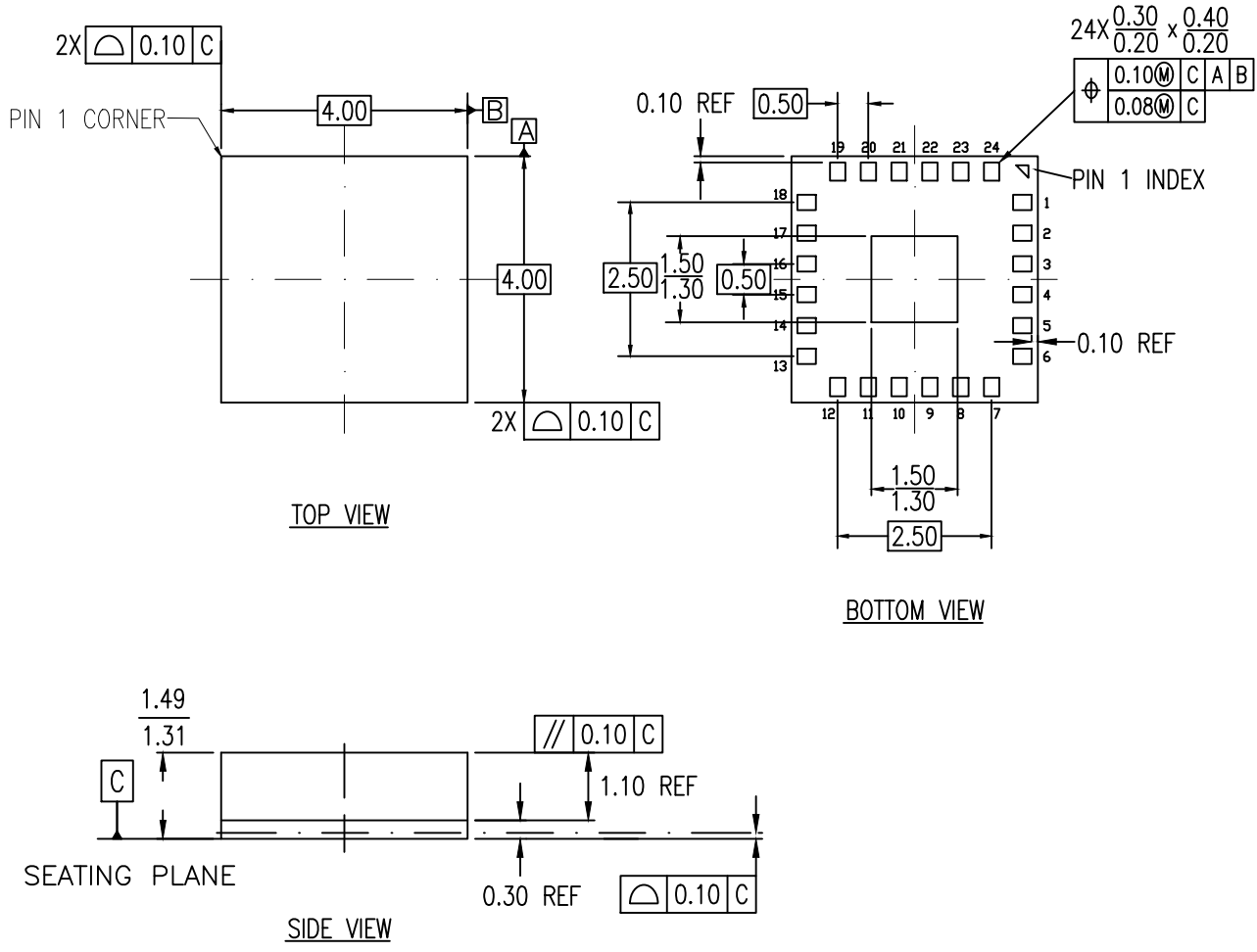
SIDE VIEW



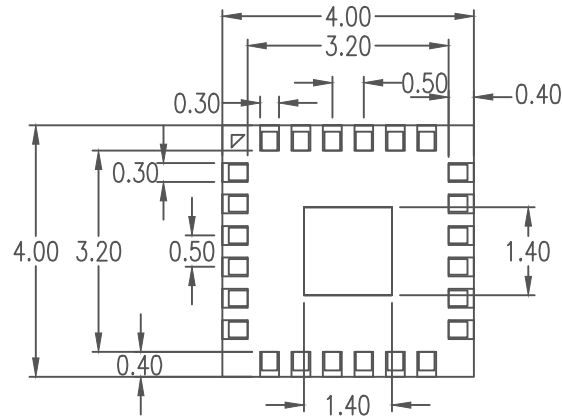
RECOMMENDED LAND PATTERN  
 (PCB Top View, NSMD Design)

**NOTES:**

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use  $\pm 0.05$  mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.



- NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
  2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 15, 2017	Rev 00	Initial Release







