

Monolithic, Quad SPST, CMOS Analog Switches

August 1997

Features

- ON-Resistance (Max) 85Ω
- Low Power Consumption (P_D) <35μW
- Fast Switching Action
 - t_{ON} <250ns
 - t_{OFF} (DG444) <120ns
- Low Charge Injection
- Upgrade from DG211/DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE | PKG. NO. |
|-------------|------------------|------------|----------|
| DG444DJ | -40 to 85 | 16 Ld PDIP | E16.3 |
| DG444DY | -40 to 85 | 16 Ld SOIC | M16.15 |
| DG445DJ | -40 to 85 | 16 Ld PDIP | E16.3 |
| DG445DY | -40 to 85 | 16 Ld SOIC | M16.15 |

Description

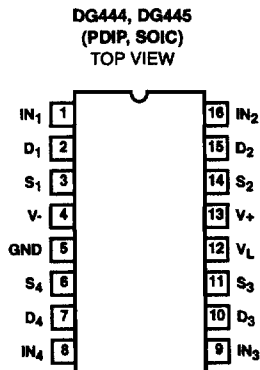
The DG444 and DG445 monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole single throw (SPST) analog switches and TTL and CMOS compatible digital inputs.

These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} <250ns) compared to the DG211 and DG212. Charge injection has been reduced, simplifying sample and hold applications.

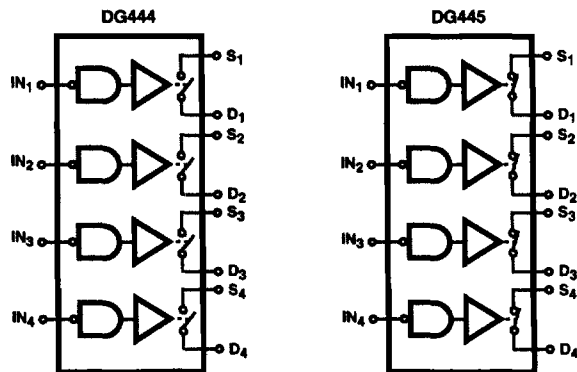
The improvements in the DG444 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling ±20V signals when operating with ±20V power supplies.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG444 and DG445 are identical, differing only in the polarity of the selection logic.

Pinout

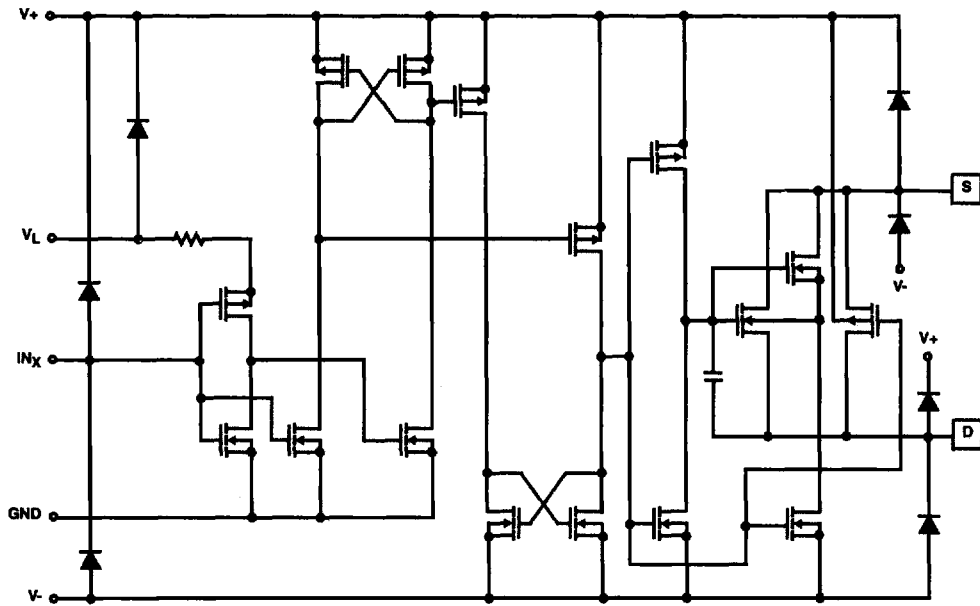


Functional Diagrams



SWITCHES SHOWN FOR LOGIC "1" INPUT

Typical Schematic Diagram (One Channel)



DG444, DG445

Absolute Maximum Ratings

| | |
|--|--|
| V+ to V- | 44V |
| GND to V- | 25V |
| V _L | (GND - 0.3V) to (V+) + 0.3V |
| Digital Inputs, V _S , V _D (Note 1) | (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First |
| Continuous Current (Any Terminal) | 30mA |
| Current, S or D (Pulsed 1ms, 10% Duty Cycle) | 100mA |

Thermal Information

| | |
|--|----------------------------------|
| Thermal Resistance (Typical, Note 2) | θ_{JA} (°C/W) |
| PDIP Package | 100 |
| SOIC Package | 115 |
| Maximum Junction Temperature (PDIP, SOIC) | 150°C |
| Maximum Storage Temperature Range (D Suffix) | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) | 300°C (SOIC - Lead Tips Only) |

Operating Conditions

| | |
|--------------------------------|----------------|
| Temperature (D Suffix) | -40°C to 85°C |
| Voltage Range | ±20V (Max) |
| Temperature Range | -55°C to 125°C |
| Input Low Voltage | 0.8V (Max) |
| Input High Voltage | 2.4V (Min) |
| Input Rise and Fall Time | ≤20ns |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Signals on S_X, D_X, or I_{NX} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | (NOTE 4) TEMP (°C) | D SUFFIX -40°C TO 85°C | | | UNITS |
|--|--|--------------------------|------------------------|-----------------|-----------------|----------|
| | | | (NOTE 5) MIN | (NOTE 6) TYP | (NOTE 5) MAX | |
| DYNAMIC CHARACTERISTICS | | | | | | |
| Turn-ON Time, t _{ON} | R _L = 1k Ω , C _L = 35pF, V _S = ±10V (See Figure 18) | 25 | - | 120 | 250 | ns |
| Turn-OFF Time, t _{OFF} | | 25 | - | 110 | 140 | ns |
| DG444 | | 25 | - | 160 | 210 | ns |
| Charge Injection, Q | C _L = 1nF, V _S = 0V, V _{GEN} = 0V, R _{GEN} = 0 Ω | 25 | - | -1 | - | pC |
| OFF Isolation | R _L = 50 Ω , C _L = 5pF, f = 1MHz | 25 | - | 60 | - | dB |
| Crosstalk (Channel-to-Channel) | Any Other Channel Switches R _L = 50 Ω , C _L = 5pF, f = 1MHz | 25 | - | 100 | - | dB |
| Source OFF Capacitance, C _{S(OFF)} | f = 1MHz | 25 | - | 4 | - | pF |
| Drain OFF Capacitance, C _{D(OFF)} | f = 1MHz | 25 | - | 4 | - | pF |
| Channel ON Capacitance, C _{D(ON)} + C _{S(ON)} | V _{ANALOG} = 0 | 25 | - | 16 | - | pF |
| DIGITAL CONTROL | | | | | | |
| Input Current V _{IN} Low, I _{IL} | V _{IN} Under Test = 0.8V, All Others = 2.4V | Full | -0.5 | -0.00001 | 0.5 | μ A |
| Input Current V _{IN} High, I _{IH} | V _{IN} Under Test = 2.4V, All Others = 0.8V | Full | -0.5 | 0.00001 | 0.5 | μ A |
| ANALOG SWITCH | | | | | | |
| Analog Signal Range, V _{ANALOG} | | Full | -15 | - | 15 | V |
| Drain-Source ON Resistance, r _{DS(ON)} | V _S = \mp 10mA, V _D = ±8.5V, V+ = 13.5V, V- = -13.5V | 25 | - | 50 | 85 | Ω |
| Switch OFF Leakage Current, I _{S(OFF)} | V+ = 16.5V, V- = -16.5V, V _D = ±15.5V, V _S = \mp 15.5V | 25 | -0.5 | 0.01 | 0.5 | nA |
| Switch OFF Leakage Current, I _{D(OFF)} | V+ = 16.5V, V- = -16.5V, V _D = ±15.5V, V _S = \mp 15.5V | 25 | -0.5 | 0.01 | 0.5 | nA |
| | | Hot | -5 | - | 5 | nA |

DG444, DG445

Electrical Specifications Test Conditions: $V_+ = +15V$, $V_- = -15V$, $V_L = 5V$, $V_{IN} = 2.4V, 0.8V$ (Note 3),
Unless Otherwise Specified (Continued)

| PARAMETER | TEST CONDITIONS | (NOTE 4) TEMP (°C) | D SUFFIX -40°C TO 85°C | | | UNITS |
|--|---|--------------------------|------------------------|-----------------|-----------------|---------|
| | | | (NOTE 5) MIN | (NOTE 6) TYP | (NOTE 5) MAX | |
| Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$ | $V_+ = 16.5V$, $V_- = -16.5V$ $V_S = V_D = \pm 15.5V$ | 25 | -0.5 | 0.08 | 0.5 | nA |
| | | Hot | -10 | - | 10 | nA |
| POWER SUPPLIES | | | | | | |
| Positive Supply Current, I_+ | $V_+ = 16.5V$, $V_- = -16.5V$, $V_{IN} = 0V$ or $5V$ | 25 | - | 0.001 | 1 | μA |
| | | Hot | - | - | 5 | μA |
| Negative Supply Current, I_- | | 25 | -1 | -0.0001 | - | μA |
| | | Hot | -5 | - | - | μA |
| Logic Supply Current, I_L | | 25 | - | 0.001 | 1 | μA |
| | | Hot | - | - | 5 | μA |
| Ground Current, I_{GND} | | 25 | -1 | -0.001 | - | μA |
| | | Hot | -5 | - | - | μA |

Electrical Specifications (Unipolar Supplies) Test Conditions: $V_+ = +12V$, $V_- = 0V$, $V_L = 5V$, $V_{IN} = 2.4V, 0.8V$ (Note 3),
Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | (NOTE 4) TEMP (°C) | D SUFFIX -40°C TO 85°C | | | UNITS |
|--|---|--------------------------|------------------------|-----------------|-----------------|----------|
| | | | (NOTE 5) MIN | (NOTE 6) TYP | (NOTE 5) MAX | |
| DYNAMIC CHARACTERISTICS | | | | | | |
| Turn-ON Time, t_{ON} | $R_L = 1k\Omega$, $C_L = 35pF$, $V_S = 8V$, (See Figure 18) | 25 | - | 300 | 450 | ns |
| Turn-OFF Time, t_{OFF} | | 25 | - | 60 | 200 | ns |
| Charge Injection, Q | $C_L = 1nF$, $V_{GEN} = 6V$, $R_{GEN} = 0\Omega$ | 25 | - | 2 | - | pC |
| ANALOG SWITCH | | | | | | |
| Analog Signal Range, V_{ANALOG} | | Full | 0 | - | 12 | V |
| Drain-Source ON Resistance, $r_{DS(ON)}$ | $I_S = -10mA$, $V_D = 3V, 8V$ $V_+ = 10.8V$, $V_L = 5.25V$ | 25 | - | 100 | 160 | Ω |
| | | Full | - | - | 200 | Ω |
| POWER SUPPLIES | | | | | | |
| Positive Supply Current, I_+ | $V_+ = 13.2V$, $V_{IN} = 0V$ or $5V$ | 25 | - | 0.001 | 1 | μA |
| | | Full | - | - | 5 | μA |
| Negative Supply Current, I_- | $V_{IN} = 0V$ or $5V$ | 25 | -1 | -0.0001 | - | μA |
| | | Full | -5 | - | - | μA |
| Logic Supply Current, I_L | $V_L = 5.25V$, $V_{IN} = 0V$ or $5V$ | 25 | - | 0.001 | 1 | μA |
| | | Full | - | - | 5 | μA |
| Ground Current, I_{GND} | $V_{IN} = 0V$ or $5V$ | 25 | -1 | -0.001 | - | μA |
| | | Full | -5 | - | - | μA |

NOTES:

3. V_{IN} = Input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Typical Performance Curves

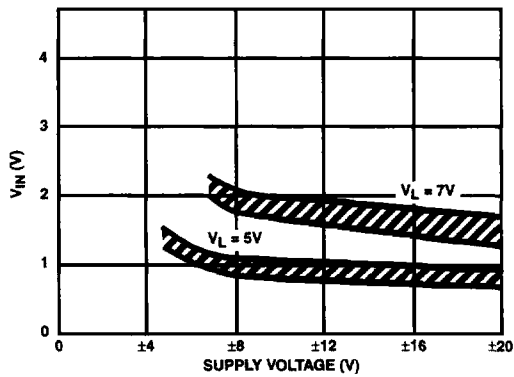


FIGURE 1. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

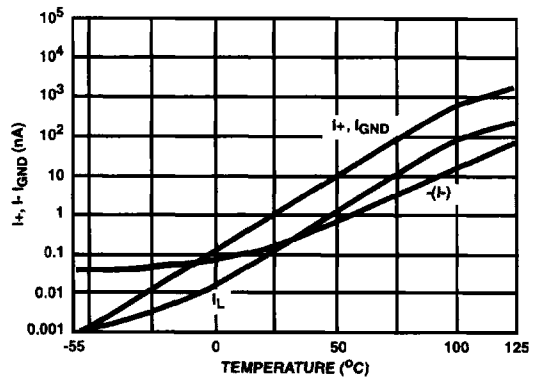


FIGURE 2. SUPPLY CURRENT vs TEMPERATURE

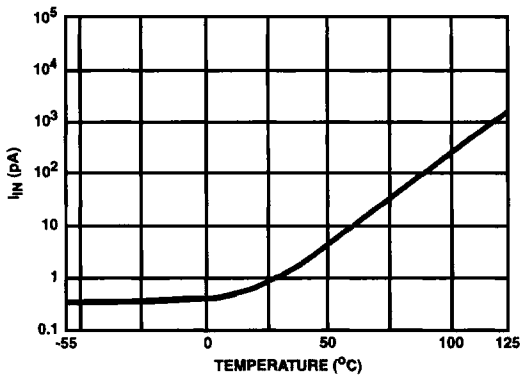


FIGURE 3. INPUT CURRENT vs TEMPERATURE

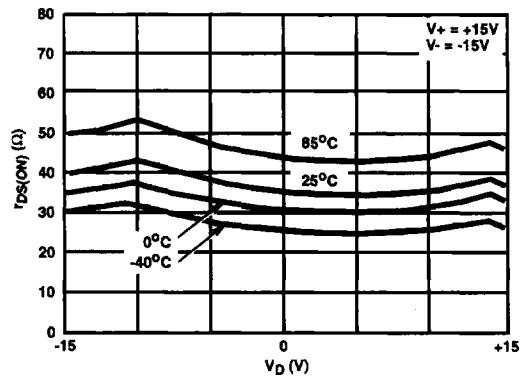


FIGURE 4. $r_{DS(ON)}$ vs V_D AND TEMPERATURE

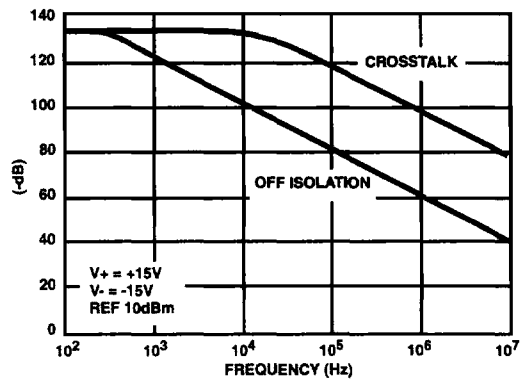


FIGURE 5. CROSSTALK AND OFF ISOLATION vs FREQUENCY

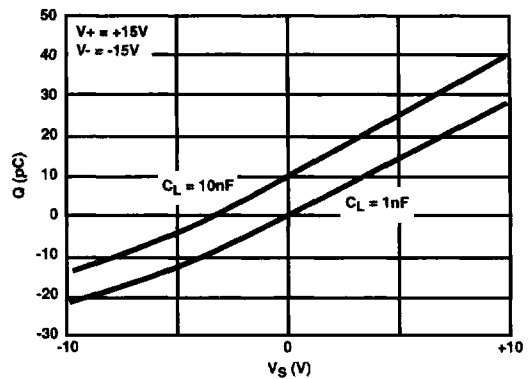


FIGURE 6. CHARGE INJECTION vs SOURCE VOLTAGE

Typical Performance Curves (Continued)

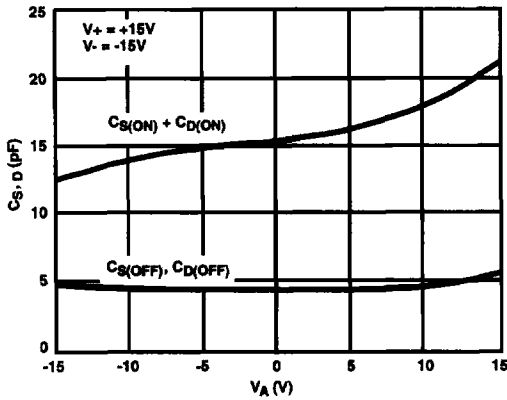


FIGURE 7. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

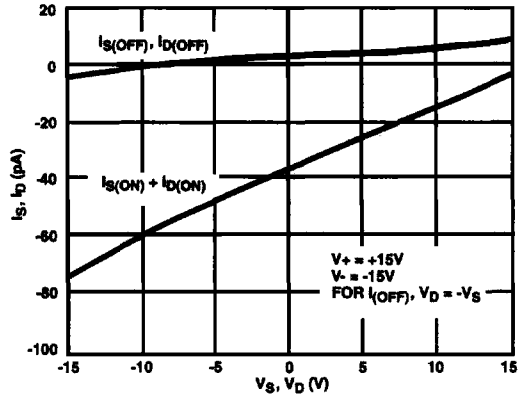


FIGURE 8. SOURCE/DRAIN LEAKAGE CURRENTS

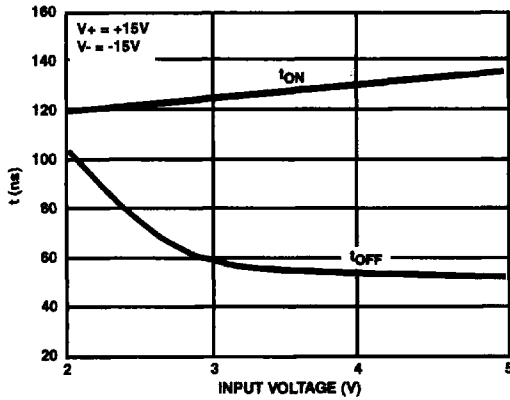


FIGURE 9. SWITCHING TIME vs INPUT VOLTAGE

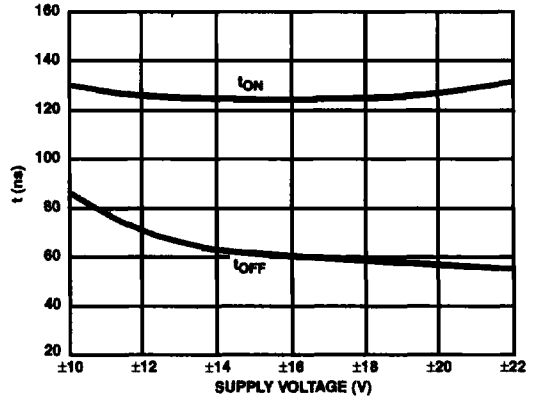


FIGURE 10. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG444)

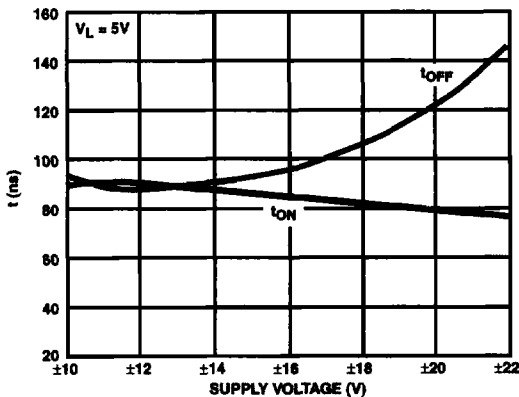


FIGURE 11. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG445)

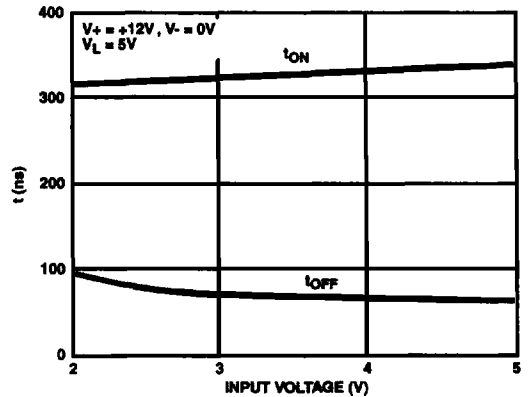


FIGURE 12. SWITCHING TIME vs INPUT VOLTAGE (DG444)

Typical Performance Curves (Continued)

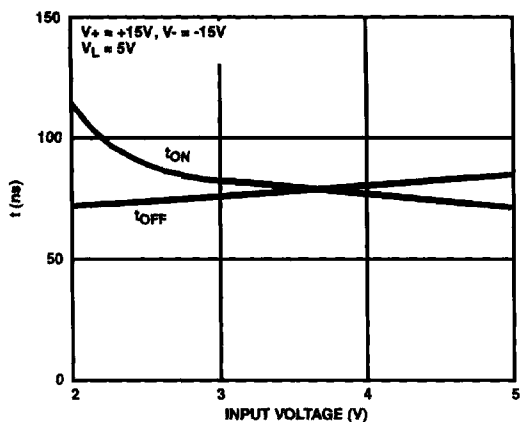


FIGURE 13. SWITCHING TIME vs INPUT VOLTAGE (DG445)

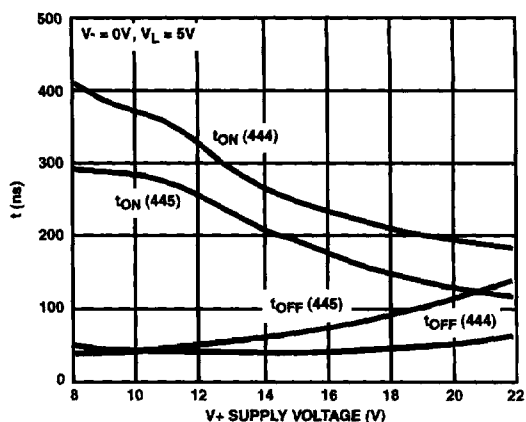


FIGURE 14. SWITCHING TIMES vs POWER SUPPLY VOLTAGE

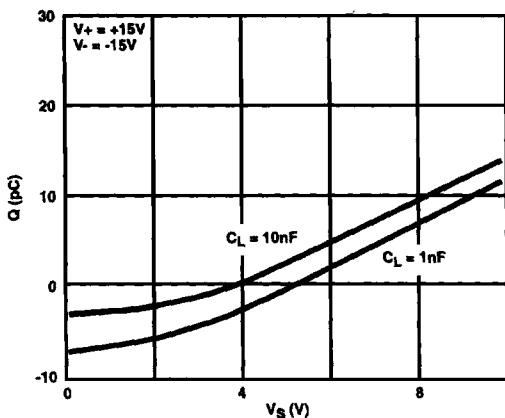


FIGURE 15. CHARGE INJECTION vs SOURCE VOLTAGE (SINGLE 12V SUPPLY)

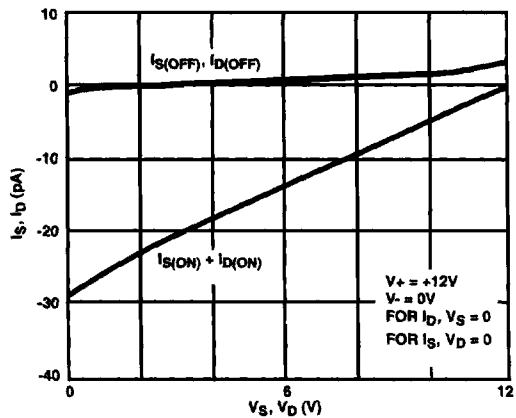


FIGURE 16. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

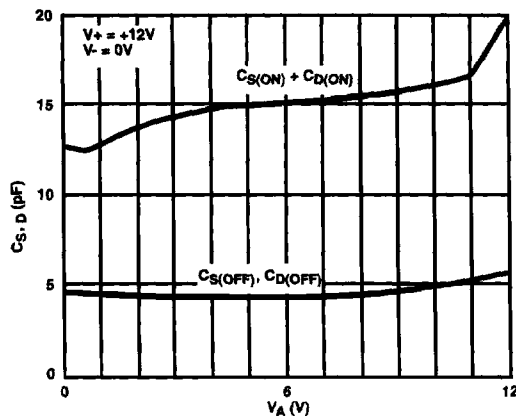


FIGURE 17. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

Pin Descriptions

| PIN | SYMBOL | DESCRIPTION |
|-----|-----------------|--|
| 1 | IN ₁ | Logic Control for Switch 1 |
| 2 | D ₁ | Drain (Output) Terminal for Switch 1 |
| 3 | S ₁ | Source (Input) Terminal for Switch 1 |
| 4 | V- | Negative Power Supply Terminal |
| 5 | GND | Ground Terminal (Logic Common) |
| 6 | S ₄ | Source (Input) Terminal for Switch 4 |
| 7 | D ₄ | Drain (Output) Terminal for Switch 4 |
| 8 | IN ₄ | Logic Control for Switch 4 |
| 9 | IN ₃ | Logic Control for Switch 3 |
| 10 | D ₃ | Drain (Output) Terminal for Switch 3 |
| 11 | S ₃ | Source (Input) Terminal for Switch 3 |
| 12 | V _L | Logic Reference Voltage. |
| 13 | V+ | Positive Power Supply Terminal (Substrate) |
| 14 | S ₂ | Source (Input) Terminal for Switch 2 |
| 15 | D ₂ | Drain (Output) Terminal for Switch 2 |
| 16 | IN ₂ | Logic Control for Switch 2 |

TRUTH TABLE

| LOGIC | V _{IN} | DG444 | DG445 |
|-------|-----------------|-------|-------|
| 0 | ≤0.8V | ON | OFF |
| 1 | ≥2.4V | OFF | ON |

Test Circuits and Waveforms

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

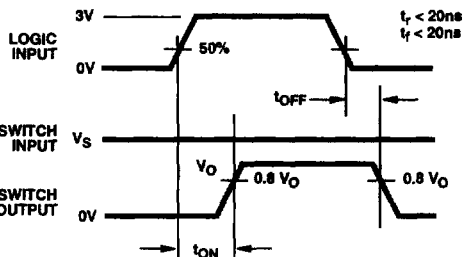
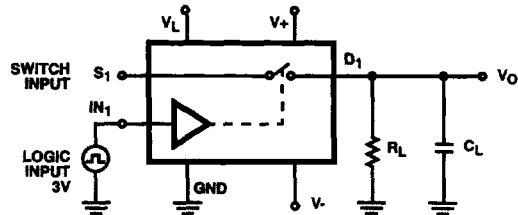


FIGURE 18A.

NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.



Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications C_L (includes fixture and stray capacitance).

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 18B.

FIGURE 18. SWITCHING TIME

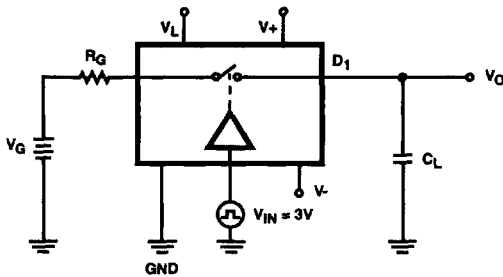


FIGURE 19A.

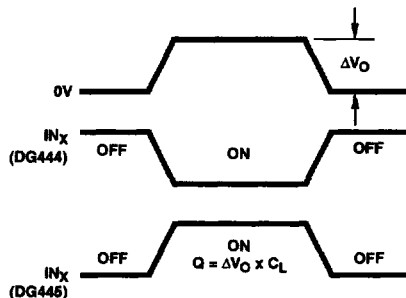


FIGURE 19B.

FIGURE 19. CHARGE INJECTION

Test Circuits and Waveforms (Continued)

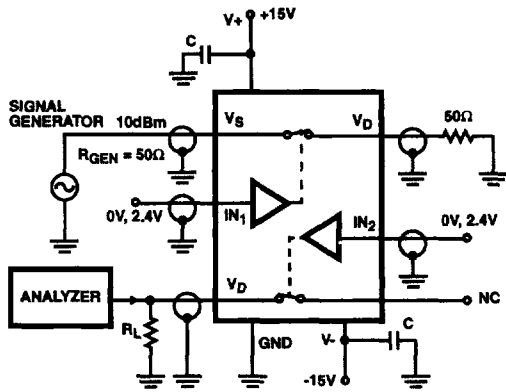


FIGURE 20. CROSSTALK

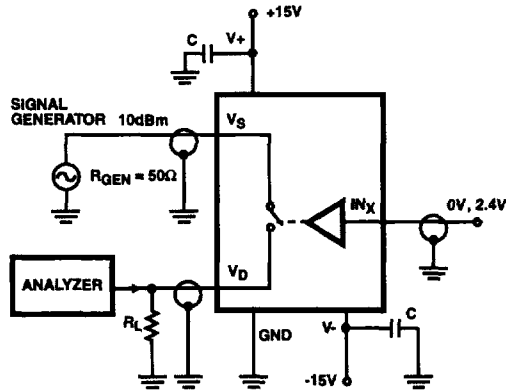


FIGURE 21. OFF ISOLATION

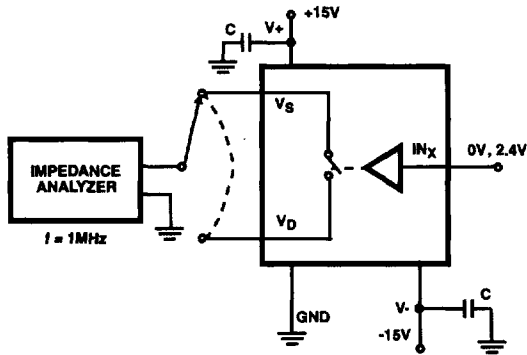
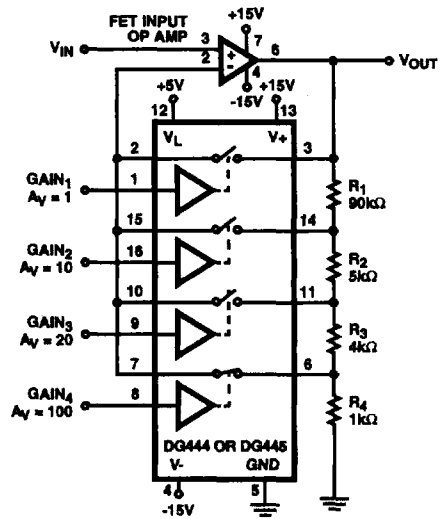


FIGURE 22. SOURCE/DRAIN CAPACITANCES

Typical Applications



GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE, OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OR CIRCUIT

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

WITH SW₄ CLOSED

FIGURE 23. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

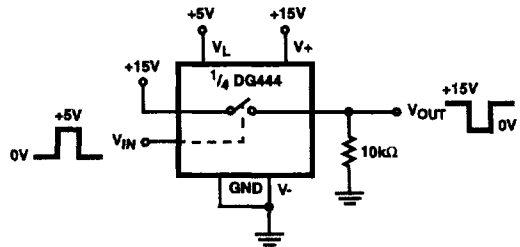


FIGURE 24. LEVEL SHIFTER

DG444, DG445

Die Characteristics

DIE DIMENSIONS:

2160 μm x 1760 μm x 485 \pm 25 μm

METALLIZATION:

Type: SiAl
Thickness: 12k \AA \pm 1k \AA

PASSIVATION:

Type: Nitride
Thickness: 8k \AA \pm 1k \AA

WORST CASE CURRENT DENSITY:

9.1 x 10⁴ A/cm²

Metallization Mask Layout

