

One out of two analog switch circuit

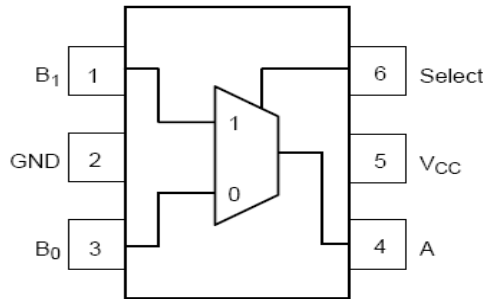
**summary**

TS5A63157 is an analog switch based on CMOS technology. It has low power consumption, low transmission delay and low output impedance. The voltage output range of analog signal and digital signal can be from  $V_{CC}$  or GND. The select input terminal has over-voltage protection, which allows the input voltage to be higher than  $V_{CC}$ , up to 7V, and the pin will not be burned.

**Functional features**

- low power consumption
- High transmission speed
- Flip standard CMOS logic level
- High bandwidth, high linearity
- Switch for NTSC / PAL video, audio, SPDIF and HDTV
- It can be used for clock switch and data selection switch
- Low output impedance
- First break and then open protection to prevent short circuit
- Working temperature - 55 °C ~ + 125 °C

**Pin layout**



SC70-6 /SOT23-6

One out of two analog switch circuit

Pin description

Pin	I/O	function
A, B <sub>0</sub> , B <sub>1</sub>	I/O	Data port
Select	I	Control selection
V <sub>CC</sub>	—	Power supply terminal
GND	—	land

Function description

Select input	function
L	B <sub>0</sub> to A
H	B <sub>1</sub> to A

Thermal resistance data

parameter	Symbol	numerical value	Company
thermal resistance	$\theta_{JA}$	270	°C/W

Limit parameter

parameter	Symbol	Range	Company
supply voltage	V <sub>CC</sub>	-0.5~+7.0	V
Switching voltage (Note 1)	V <sub>S</sub>	-0.5~V <sub>CC</sub> +0.5	V
Input voltage (Note 1)	V <sub>IN</sub>	-0.5~+7.0	V
Vin @ 0V input current clamp diode	I <sub>IK</sub>	-50	mA
Output current	I <sub>out</sub>	128	mA
Power to ground current	I <sub>CC</sub> /I <sub>GND</sub>	100	mA
Storage temperature range	T <sub>stg</sub>	-65~+150	°C
Maximum junction temperature	T <sub>J</sub>	150	°C
Wire temperature (welding, 10 seconds)	T <sub>L</sub>	260	°C
Total power consumption (85 °C)	P <sub>D</sub>	180	mW

Exceeding the maximum value of DC limit parameters may cause irreparable damage to the circuit. If there is no special case, ensure that the power supply voltage, operating temperature and load characteristics of input / output of the whole working system are within the above range.

Note 1: the negative voltage of I / O can be exceeded according to the clamping diode current range of input / output.

Working environment (Note 2)

parameter	Symbol	MID	MXA	Company
supply voltage	V <sub>CC</sub>	1.65	5.5	V
Select terminal input voltage	V <sub>IN</sub>	0	V <sub>CC</sub>	V
Switch input voltage	V <sub>IN</sub>	0	V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	0	V <sub>CC</sub>	V
Working temperature	T <sub>A</sub>	-55	+125	
Enter the rising and falling time. Input voltage VCC = 2.3V - 3.6V.	t <sub>r</sub> , t <sub>f</sub>	0	10	ns/V
Input voltage VCC = 4.5V - 5.5V.		0	5.0	

Note: The input voltage of 2:Select terminal must be set to a high level or a low level, and cannot be left floating.

One out of two analog switch circuit

Electrical parameter

parameter	sign	test condition	V <sub>CC</sub>	T <sub>A</sub> =25°C			T <sub>A</sub> =-40°C~+85°C		Company	
				mid	standard	max	min	max		
<b>DC characteristic</b>										
V <sub>IH</sub>	High level input		1.65-1.95				0.75V <sub>CC</sub>		V	
			2.3-2.8				1.5			
			3-4.2				2.4			
			4.5-5.5				0.6V <sub>CC</sub>			
V <sub>IL</sub>	Input low level		1.65-1.95					0.25V <sub>CC</sub>	V	
			2.3-2.8					0.4		
			3-5.5					0.3V <sub>CC</sub>		
I <sub>IN</sub>	Leakage current input	0<V <sub>IN</sub> <5.5V	0-5.5		± 0.05	± 0.1		± 1	uA	
I <sub>OFF</sub>	Closed state leakage electric current	0<A,B<V <sub>CC</sub>	1.65-5.5		± 0.05	± 0.1		± 1	uA	
I <sub>CC</sub>	Quiescent current	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0	5.5			1.0		10	uA	
	Analog level input Into the scope		V <sub>CC</sub>	0		V <sub>CC</sub>	0	V <sub>CC</sub>	V	
R <sub>ON</sub>	Switch on resistance (Note 3)	V <sub>IN</sub> =0V, I <sub>O</sub> =30mA	4.5			3.0			7.0	Ω
		V <sub>IN</sub> =2.4V, I <sub>O</sub> =-30mA				5.0			12	Ω
		V <sub>IN</sub> =4.5V, I <sub>O</sub> =-30mA				7.0			15	Ω
		V <sub>IN</sub> =0V, I <sub>O</sub> =24mA	3.0			4.0			9.0	Ω
		V <sub>IN</sub> =3V, I <sub>O</sub> =-24mA				10			20	Ω
		V <sub>IN</sub> =0V, I <sub>O</sub> =8mA	2.3			5.0			12	Ω
		V <sub>IN</sub> =2.3V, I <sub>O</sub> =-8mA				13			30	Ω
		V <sub>IN</sub> =0V, I <sub>O</sub> =4mA	1.65			6.5			20	Ω
V <sub>IN</sub> =1.65V, I <sub>O</sub> =-4mA				17			50	Ω		
R <sub>RANGE</sub>	Full signal range on resistance (Note 3 ) (Note 7)	I <sub>A</sub> =-30mA 0≤V <sub>Bn</sub> ≤V <sub>CC</sub>	4.5						25	Ω
		I <sub>A</sub> =-24mA 0≤V <sub>Bn</sub> ≤V <sub>CC</sub>	3						50	Ω
		I <sub>A</sub> =-8mA 0≤V <sub>Bn</sub> ≤V <sub>CC</sub>	2.3						100	Ω
		I <sub>A</sub> =-4mA 0≤V <sub>Bn</sub> ≤V <sub>CC</sub>	1.65						300	Ω

One out of two analog switch circuit

$\Delta R_{ON}$	On resistance matching between channels (Note 3) (Note 4) (Note 5)	$I_A = -30mA$ $V_{Bn} = 3.15$	4.5		0.15			$\Omega$
		$I_A = -24mA$ $V_{Bn} = 2.1$	3		0.2			$\Omega$
		$I_A = -8mA$ $V_{Bn} = 1.6$	2.3		0.5			$\Omega$
		$I_A = -4mA$ $V_{Bn} = 1.15$	1.65		0.5			$\Omega$
$R_{FLAT}$	On-resistance flatness (Note 3) (Note 4) (Note 6)	$I_A = -30mA$ $0 \leq V_{Bn} \leq V_{CC}$	5		6.0			$\Omega$
		$I_A = -24mA$ $0 \leq V_{Bn} \leq V_{CC}$	3.3		12			$\Omega$
		$I_A = -8mA$ $0 \leq V_{Bn} \leq V_{CC}$	2.5		28			$\Omega$
		$I_A = -4mA$ $0 \leq V_{Bn} \leq V_{CC}$	1.8		125			$\Omega$
<b>AC characteristics</b>								
$t_{PHL}$ $t_{PLH}$	Transmission Delay (Note 8)	Fig. 1 $V_I = OPEN$	1.65-1.95					nS
			2.3-2.7				1.2	nS
			3.0-3.5				0.8	nS
			4.5-5.5				0.3	nS
$t_{PZL}$ $t_{PZH}$	Open time (a to Bn)	Fig. 1 $V_I = 2 * V_{CC}$ for $t_{PZL}$ , $V_I = 0V$ for $t_{PZH}$	1.65-1.95		23	7.0	24	nS
			2.3-2.7		13	3.5	14	nS
			3.0-3.5		6.9	2.5	7.6	nS
			4.5-5.5		5.2	1.7	5.7	nS
$t_{PLZ}$ $t_{PHZ}$	turn - off time (port a to port b)	Fig. 1 $V_I = 2 * V_{CC}$ for $t_{PLZ}$ , $V_I = 0V$ for $t_{PHZ}$	1.65-1.95		12.5	3.0	13	nS
			2.3-2.7		7.0	2.0	7.5	nS
			3.0-3.5		5.0	1.5	5.3	nS
			4.5-5.5		3.5	0.8	3.8	nS
$t_{B-M}$	Break before connect time (Note 7)	Fig. 2, $C_L = 50pF$ , $R_L = 600\Omega$	1.65-1.95			0.5		nS
			2.3-2.7			0.5		nS
			3.0-3.5			0.5		nS
			4.5-5.5			0.5		nS
Q	Charge injection (Note 7)	Fig. 3, $C_L = 0.1nF$ , $V_{GEN} = 0V$ $R_{GEN} = 0\Omega$	5.0		7.0			pC
			3.3		3.0			pC
OIRR	Close (note 9) Release	Fig. 4, $r_L = 50\omega$ , $f = 10MHz$	1.65-5.5		-57			dB
Xtalk	cross talk	Fig. 5, $r_L = 50\omega$ , $f =$	1.65-5.5		-54			dB

One out of two analog switch circuit

		10MHz						
BW	-3dB bandwidth	Fig. 8, $r_L = 50 \omega$	1.65-5.5		350M			Hz
THD	total harmonic distortion (Note 7)	$R_L=600\Omega$ , $0.5V_{P-P}$ $f=600\text{Hz}-20\text{kHz}$	5.0		0.011			%
$C_{IN}$	Input terminal capacitance (Note 10)		0		2.3			pF
$C_{IOB}$	B disconnection capacitance when the port is turned off (Note 10)	Figure 6	5.0		5.0			pF
$C_{IOAON}$	A conduction capacitance when the port is open (Note 10)	Figure 7	5.0		15.5			pF

Note3: It is obtained by measuring the ratio of the voltage difference between the two ports A and B to the current flowing through the two ports. On-resistance is determined by the lower voltage port of port A and B

Note4: The load characteristics introduced by encapsulation are not included.

Note5:  $\Delta RON = RON_{max} - RON_{min}$  in the given VCC, temperature and level range.

Note6: On-resistance flatness refers to the difference between the maximum value and the minimum value of on-resistance under specified conditions.

Note 7: Design simulation value.

Note 8: This parameter is the design simulation value rather than the measured value. In the case of an ideal voltage source (zero output load), the transmission delay will be better than that of a 50pF load capacitor.

Note 9: Turn off isolation  $=20\log_{10}[VA/VBn]$ .

Note 10:  $T_A=+25^\circ\text{C}$ ,  $f=1\text{MHz}$ , excluding the load capacitance introduced by packaging.

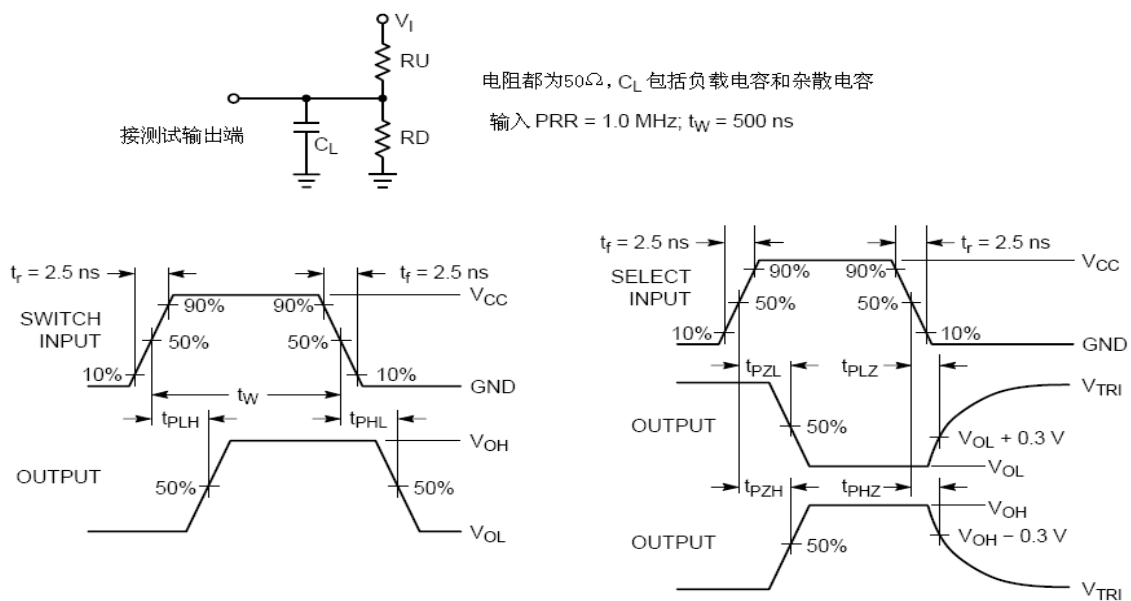


Figure 1 Transmission delay,

One out of two analog switch circuit



Figure 2: Break first and

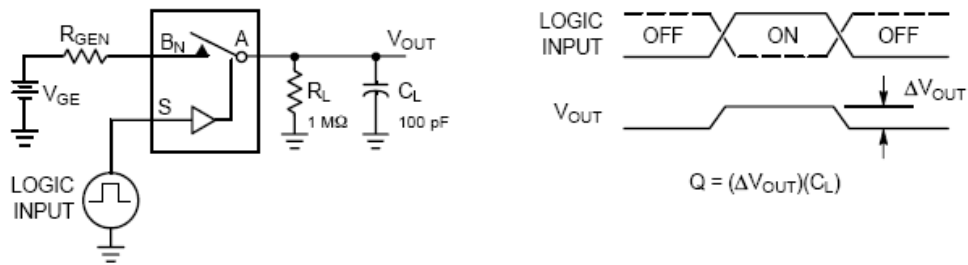


Figure 3 Charge

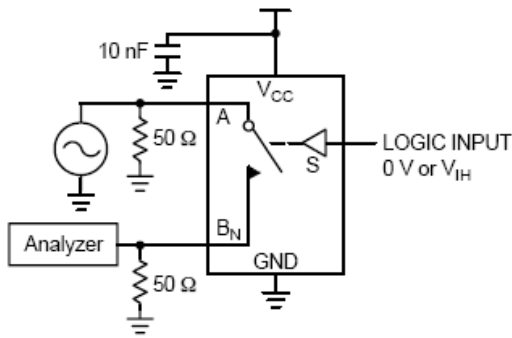


Figure 4 Turning off

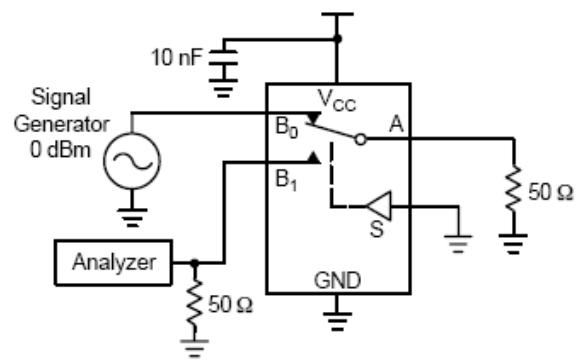


Figure 5 Crosstalk

One out of two analog switch circuit

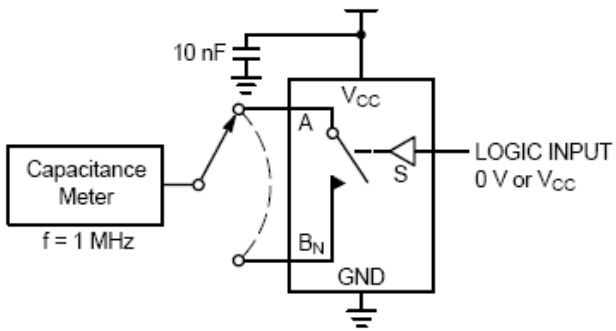


Figure 6 Output

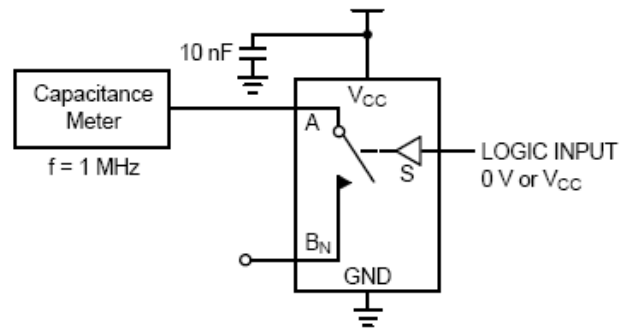


Figure 7 Output

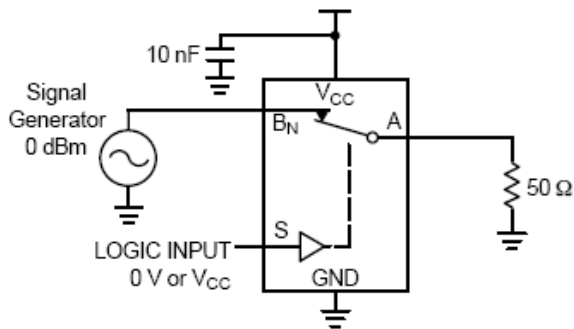
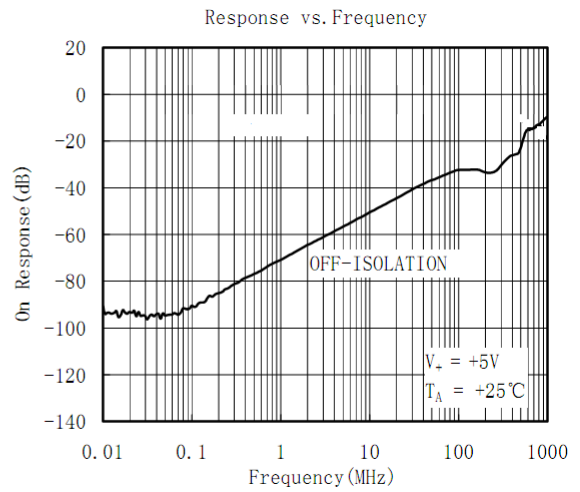
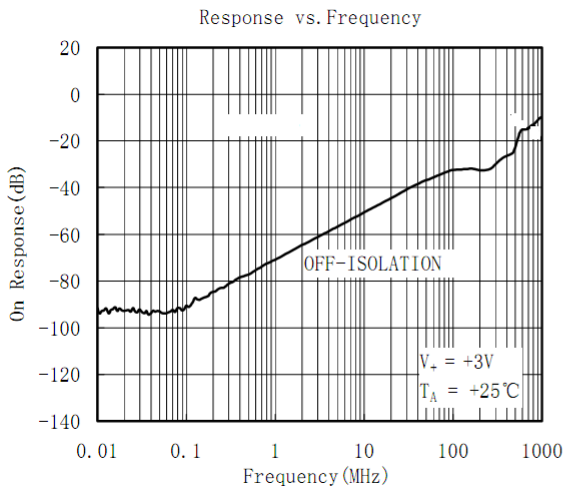
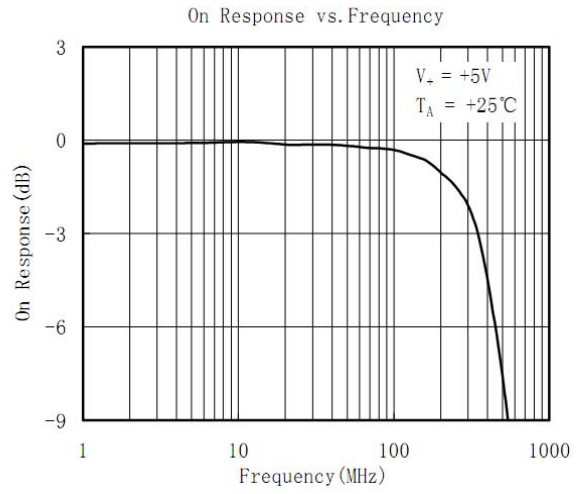
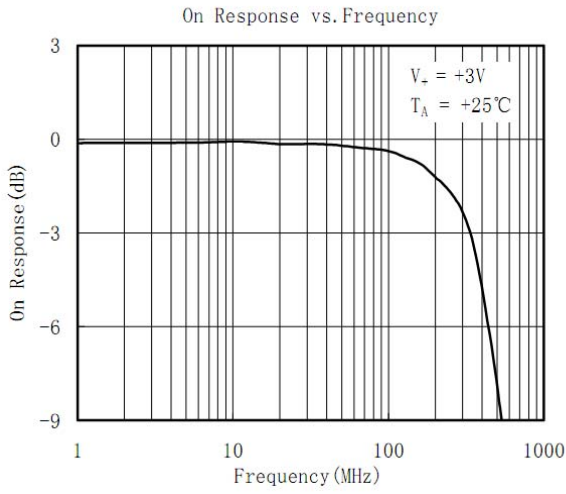


Figure 8 Bandwidth

One out of two analog switch circuit

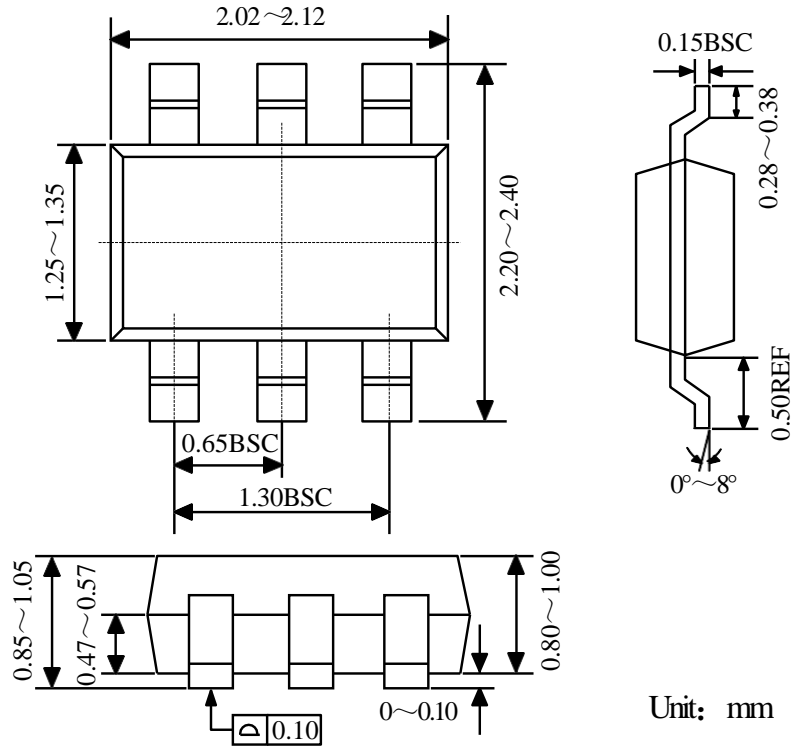




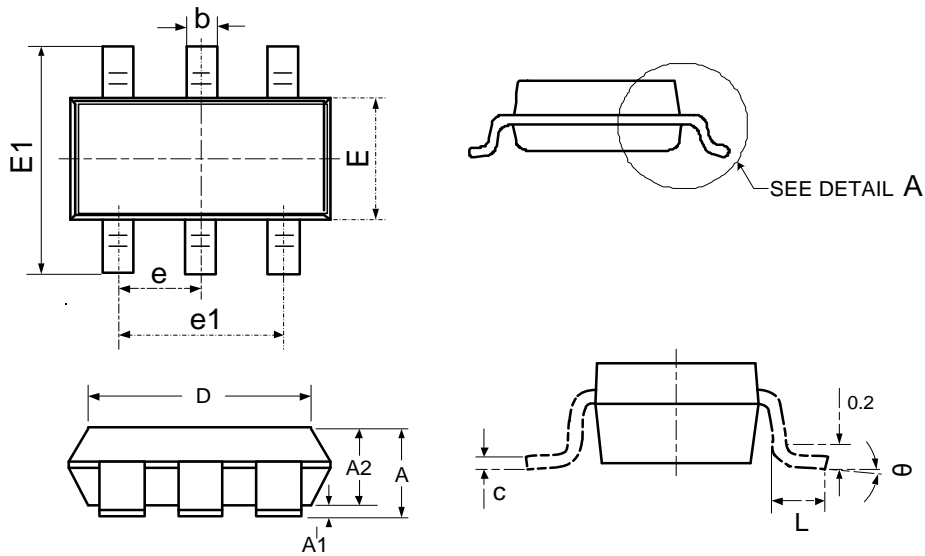
One out of two analog switch circuit

Package size

SC70 - 6



SOT23-6



Order information

Order code	Package	Baseqty	Deliverymode	Marking
UMW TS5A63157DCKR	SC70-6	3000	Tape and reel	J75 U
UMW TS5A63157DBVR	SOT23-6	3000	Tape and reel	JBEF U