Quad Digitally Programmable Potentiometers (DPP™) with 64 Taps and I²C Interface

HALOGEN FREE LEAD FREE™ RoHS Compliance

FEATURES

- **Four linear taper digitally programmable potentiometers**
- **64 resistor taps per potentiometer**
- **End to end resistance 2.5kΩ, 10kΩ, 50kΩ or 100kΩ**
- **I²C interface**
- **Low wiper resistance, typically 80Ω**
- **Four non-volatile wiper settings for each potentiometer**
- **Recall of saved wiper settings at power-up**
- **2.5 to 6.0 volt operation**
- **Standby current less than 1µA**
- **1,000,000 nonvolatile WRITE cycles**
- **100 year nonvolatile memory data retention**
- **24-lead SOIC and 24-lead TSSOP**
- **Write protection for data register**

For Ordering Information details, see page 15.

DESCRIPTION

The CAT5409 is four Digitally Programmable Potentiometers (DPP™) integrated with control logic and 16 bytes of NVRAM memory.

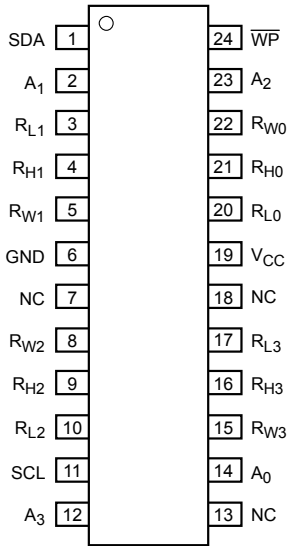
A separate 6-bit control register (WCR) independently controls the wiper tap position for each DPP. Associated with each wiper control register are four 6-bit non-volatile memory data registers (DR) used for storing up to four wiper settings. Writing to the wiper control register or any of the non-volatile data registers is via a I²C serial bus. On power-up, the contents of the first data register (DR0) for each of the four potentiometers is automatically loaded into its respective wiper control register (WCR).

The Write Protection ($\overline{WP}$) pin protects against inadvertent programming of the data register.

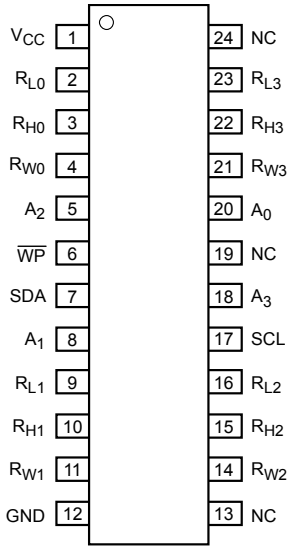
The CAT5409 can be used as a potentiometer or as a two terminal, variable resistor. It is intended for circuit level or system level adjustments in a wide variety of applications.

PIN CONFIGURATION

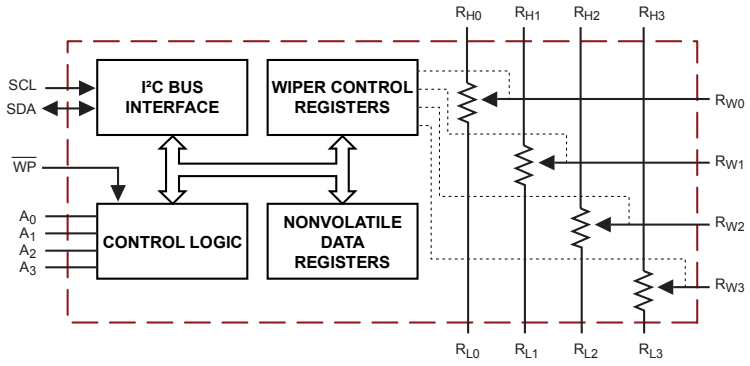
SOIC (W)



TSSOP (Y)



FUNCTIONAL DIAGRAM



PIN DESCRIPTIONS

Pin# (SOIC)	Pin# (TSSOP)	Name	Function
19	1	V_{CC}	Supply Voltage
20	2	R_{L0}	Low Reference Terminal for Potentiometer 0
21	3	R_{H0}	High Reference Terminal for Potentiometer 0
22	4	R_{W0}	Wiper Terminal for Potentiometer 0
23	5	A2	Device Address
24	6	$\overline{WP}$	Write Protection
1	7	SDA	Serial Data Input/Output
2	8	A1	Device Address
3	9	R_{L1}	Low Reference Terminal for Potentiometer 1
4	10	R_{H1}	High Reference Terminal for Potentiometer 1
5	11	R_{W1}	Wiper Terminal for Potentiometer 1
6	12	GND	Ground
7	13	NC	No Connect
8	14	R_{W2}	Wiper Terminal for Potentiometer 2
9	15	R_{H2}	High Reference Terminal for Potentiometer 2
10	16	R_{L2}	Low Reference Terminal for Potentiometer 2
11	17	SCL	Bus Serial Clock
12	18	A3	Device Address
13	19	NC	No Connect
14	20	A0	Device Address, LSB
15	21	R_{W3}	Wiper Terminal for Potentiometer 3
16	22	R_{H3}	High Reference Terminal for Potentiometer 3
17	23	R_{L3}	Low Reference Terminal for Potentiometer 3
18	24	NC	No Connect

SCL: Serial Clock

The CAT5409 serial clock input pin is used to clock all data transfers into or out of the device.

SDA: Serial Data

The CAT5409 bidirectional serial data pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-Ored with the other open drain or open collector outputs.

A0, A1, A2, A3: Device Address Inputs

These inputs set the device address when addressing multiple devices. A total of sixteen devices can be addressed on a single bus. A match in the slave address must be made with the address input in order to initiate communication with the CAT5409.

R_H, R_L: Resistor End Points

The four sets of R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer.

R_W: Wiper

The four R_W pins are equivalent to the wiper terminal of a mechanical potentiometer.

$\overline{WP}$: Write Protect Input

The $\overline{WP}$ pin when tied low prevents non-volatile writes to the data registers (change of wiper control register is allowed) and when tied high or left floating normal read/write operations are allowed. *See Write Protection* on page 7 for more details.

DEVICE OPERATION

The CAT5409 is four resistor arrays integrated with I²C serial interface logic, four 6-bit wiper control registers and sixteen 6-bit, non-volatile memory data registers. Each resistor array contains 63 separate resistive elements connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L). R_H and R_L are symmetrical and may be interchanged. The tap positions between and at the ends of the series resistors are connected to the output wiper terminals (R_W) by a CMOS transistor switch. Only one tap point for each potentiometer is connected to its wiper terminal at a time and is determined by the value of the wiper control register. Data can be read or written to the wiper control registers or the non-volatile memory data registers via the I²C bus. Additional instructions allows data to be transferred between the wiper control registers and each respective potentiometer's non-volatile data registers. Also, the device can be instructed to operate in an "increment/decrement" mode.

ABSOLUTE MAXIMUM RATINGS[1]

Parameters	Ratings	Units
Temperature Under Bias	-55 to +125	ºC
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to V_{SS} [1] [2]	-2.0 to +V_{CC} + 2.0	V
V_{CC} with Respect to Ground	-2.0 to +7.0	V
Package Power Dissipation Capability (T_A = 25ºC)	1.0	W
Lead Soldering Temperature (10sec)	300	ºC
Wiper Current	±12	mA

RECOMMENDED OPERATING CONDITIONS

Parameters	Ratings	Units
V_{CC}	+2.5 to +6	V
Industrial Temperature	-40 to +85	°C

POTENTIOMETER CHARACTERISTICS

Over recommended operating conditions unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance (-00)			100		kΩ
R_{POT}	Potentiometer Resistance (-50)			50		kΩ
R_{POT}	Potentiometer Resistance (-10)			10		kΩ
R_{POT}	Potentiometer Resistance (-2.5)			2.5		kΩ
	Potentiometer Resistance Tolerance				±20	%
	R_{POT} Matching				1	%
	Power Rating	25°C, each pot			50	mW
I_W	Wiper Current				±6	mA
R_W	Wiper Resistance	I_W = ±3mA @ V_{CC} = 3V			300	Ω
R_W	Wiper Resistance	I_W = ±3mA @ V_{CC} = 5V		80	150	Ω
V_{TERM}	Voltage on any R_H or R_L Pin	V_{SS} = 0V	GND		V_{CC}	V
	Resolution			1.6		%
	Absolute Linearity [5]	$R_{W(n)(actual)}$ - $R_{(n)(expected)}$ [8]			±1	LSB [7]
	Relative Linearity [6]	$R_{W(n+1)}$ - [$R_{W(n)}$ + LSB] [8]			±0.2	LSB [7]
TC_{RPOT}	Temperature Coefficient of R_{POT}	(4)		±300		ppm/ºC
TC_{RATIO}	Ratiometric Temp. Coefficient	(4)			20	ppm/ºC
$C_H/C_L/C_W$	Potentiometer Capacitances	(4)		10/10/25		pF
fc	Frequency Response	R_{POT} = 50kΩ [4]		0.4		MHz

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} +2.0V for periods of less than 20ns.

(3) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} +1V.

(4) This parameter is tested initially and after a design or process change that affects the parameter.

(5) Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.

(6) Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.

(7) LSB = R_{TOT} / 63 or (R_H - R_L) / 63, single pot.

(8) n = 0, 1, 2, ..., 63

D.C. OPERATING CHARACTERISTICS

Over recommended operating conditions unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC}	Power Supply Current	f_{SCL} = 400kHz		1	mA
I_{SB}	Standby Current (V_{CC} = 5.0V)	V_{IN} = GND or V_{CC}, SDA Open		1	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}		10	µA
V_{IL}	Input Low Voltage		-1	V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7	V_{CC} + 1.0	V
V_{OL1}	Output Low Voltage (V_{CC} = 3.0V)	I_{OL} = 3 mA		0.4	V

CAPACITANCE (1)

T_A = 25ºC, f = 1.0MHz, V_{CC} = 5V

Symbol	Test	Conditions	Max.	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, A3, SCL, $\overline{WP}$)	V_{IN} = 0V	6	pF

A.C. CHARACTERISTICS

Over recommended operating conditions unless otherwise stated.

Symbol	Parameter	Min	Typ	Max	Units
f_{SCL}	Clock Frequency			400	kHz
T_I (1)	Noise Suppression Time Constant at SCL, SDA Inputs			50	ns
t_{AA}	SLC Low to SDA Data Out and ACK Out			0.9	µs
t_{BUF} (1)	Time the bus must be free before a new transmission can start	1.2			µs
$t_{HD:STA}$	Start Condition Hold Time	0.6			µs
t_{LOW}	Clock Low Period	1.2			µs
t_{HIGH}	Clock High Period	0.6			µs
$t_{SU:STA}$	Start Condition SetupTime (for a Repeated Start Condition)	0.6			µs
$t_{HD:DAT}$	Data in Hold Time	0			ns
$t_{SU:DAT}$	Data in Setup Time	100			ns
t_R (1)	SDA and SCL Rise Time			0.3	µs
t_F (1)	SDA and SCL Fall Time			300	ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6			µs
t_{DH}	Data Out Hold Time	50			ns

POWER UP TIMING (1)

Symbol	Parameter	Max	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

WRITE CYCLE LIMITS

Symbol	Parameter	Max	Units
t_{WR}	Write Cycle Time	5	ms

The write cycle is the time from a valid stop condition of a write sequence to the end of the internal program/erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N_{END} (1)	Endurance	MIL-STD-883, Test Method 1033	1,000,000		Cycles/Byte
T_{DR} (1)	Data Retention	MIL-STD-883, Test Method 1008	100		Years
V_{ZAP} (1)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000		V
I_{LTH} (1) (2)	Latch-Up	JEDEC Standard 17	100		mA

Figure 1. Bus Timing

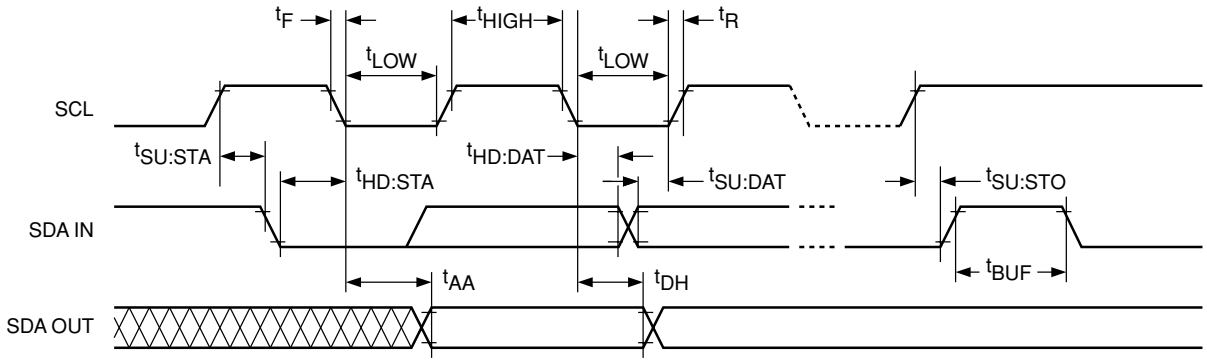


Figure 2. Write Cycle Timing

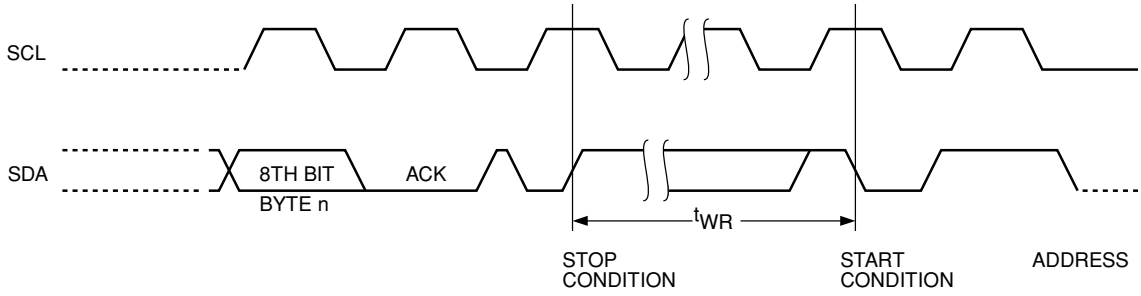
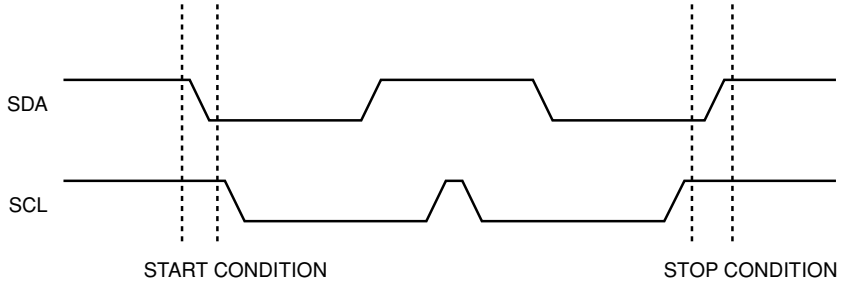


Figure 3. Start/Stop Timing



Notes:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are delays required from the time V_{CC} is stable until the specified operation can be initiated.

SERIAL BUS PROTOCOL

The following defines the features of the I²C bus protocol:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock is high will be interpreted as a START or STOP condition.

The device controlling the transfer is a master, typically a processor or controller, and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the CAT5409 will be considered a slave device in all applications.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT5409 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed as 0101 for the CAT5409 (see Figure 5). The next four significant bits (A3, A2, A1, A0) are the device address bits and define which device the Master is accessing. Up to sixteen devices may be individually addressed by the system. Typically, +5V and ground are hard-wired to these pins to establish the device's address.

After the Master sends a START condition and the slave address byte, the CAT5409 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address.

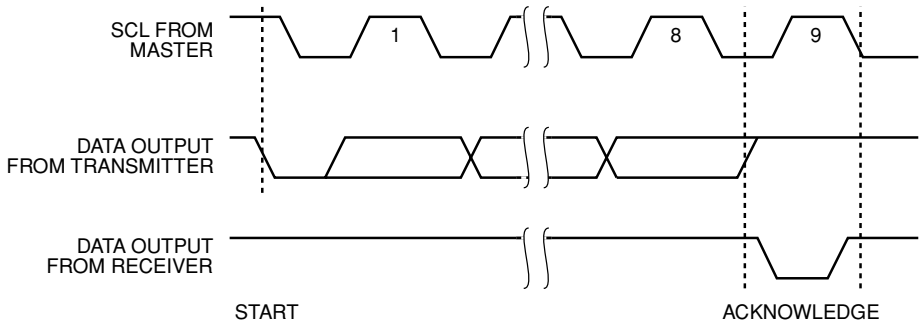
Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT5409 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT5409 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT5409 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Acknowledge Timing



WRITE OPERATIONS

In the Write mode, the Master device sends the START condition and the slave address information to the Slave device. After the Slave generates an acknowledge, the Master sends the instruction byte that defines the requested operation of CAT5409. The instruction byte consist of a four-bit opcode followed by two register selection bits and two pot selection bits. After receiving another acknowledge from the Slave, the Master device transmits the data to be written into the selected register. The CAT5409 acknowledges once more and the Master generates the STOP condition, at which time if a non-volatile data register is being selected, the device begins an internal programming cycle to non-volatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT5409 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address. If the CAT5409 is still busy with the write operation, no ACK will be returned. If the CAT5409 has completed the write operation, an ACK will be returned and the host can then proceed with the next instruction operation.

WRITE PROTECTION

The Write Protection feature allows the user to protect against inadvertent programming of the non-volatile data registers. If the $\overline{WP}$ pin is tied to LOW, the data registers are protected and become read only. Similarly, the $\overline{WP}$ pin going low after start but after start will interrupt non-volatile write to data registers, while the $\overline{WP}$ pin going low after internal write cycle has started, will have no effect on any write operation. The CAT5409 will accept both slave addresses and instructions, but the data registers are protected from programming by the device's failure to send an acknowledge after data is received.

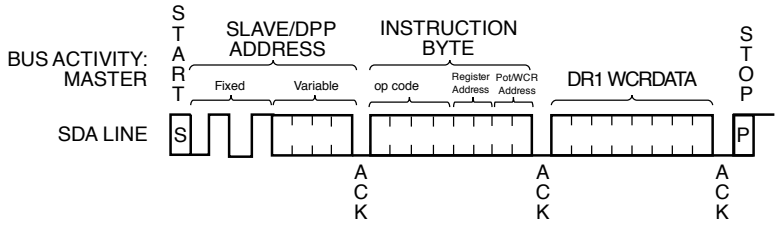
Figure 5. Slave Address Bits

CAT5409	0	1	0	1	A3	A2	A1	A0

* A0, A1, A2 and A3 correspond to pin A0, A1, A2 and A3 of the device.

** A0, A1, A2 and A3 must compare to its corresponding hard wired input pins.

Figure 6. Write Timing



INSTRUCTION AND REGISTER DESCRIPTION

SLAVE ADDRESS BYTE

The first byte sent to the CAT5409 from the master/ processor is called the Slave/DPP Address Byte. The most significant four bits of the Device Type address are a device type identifier. These bits for the CAT5409 are fixed at 0101[B] (refer to Table 1).

The next four bits, A3 - A0, are the internal slave address and must match the physical device address which is defined by the state of the A3 - A0 input pins for the CAT5409 to successfully continue the command sequence. Only the device which slave address matches the incoming device address sent by the master executes the instruction. The A3 - A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

INSTRUCTION BYTE

The next byte sent to the CAT5409 contains the instruction and register pointer information. The four most significant bits used provide the instruction opcode I [3:0]. The R1 and R0 bits point to one of the four data registers of each associated potentiometer. The least two significant bits point to one of four Wiper Control Registers. The format is shown in Table 2.

Data Register Selection

Data Register Selected	R1	R0
DR0	0	0
DR1	0	1
DR2	1	0
DR3	1	1

Table 1. Identification Byte Format

Device Type Identifier				Slave Address			
ID3	ID2	ID1	ID0	A3	A2	A1	A0
0	1	0	1				
(MSB)							(LSB)

Table 2. Instruction Byte Format

Instruction Opcode				Data Register Selection		WCR/Pot Selection	
I3	I2	I1	I0	R1	R0	P1	P0
(MSB)							(LSB)

WIPER CONTROL AND DATA REGISTERS

Wiper Control Register (WCR)

The CAT5409 contains four 6-bit Wiper Control Registers, one for each potentiometer. The Wiper Control Register output is decoded to select one of 64 switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written by the host via Write Wiper Control Register instruction; it may be written by transferring the contents of one of four associated Data Registers via the XFR Data Register instruction, it can be modified one step at a time by the Increment/decrement instruction (see Instruction section for more details). Finally, it is loaded with the content of its data register zero (DR0) upon power-up.

The Wiper Control Register is a volatile register that loses its contents when the CAT5409 is powered-down. Although the register is automatically loaded with the value in DR0 upon power-up, this may be different from the value present at power-down.

Data Registers (DR)

Each potentiometer has four 6-bit non-volatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Control Register. Any data changes in one of the Data Registers is a non-volatile operation and will take a maximum of 5ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as standard memory locations for system parameters or user preference data.

INSTRUCTIONS

Four of the nine instructions are three bytes in length. These instructions are:

— **Read Wiper Control Register** – read the current wiper position of the selected potentiometer in the WCR

— **Write Wiper Control Register** – change current wiper position in the WCR of the selected potentiometer

— **Read Data Register** – read the contents of the selected Data Register

— **Write Data Register** – write a new value to the selected Data Register

The basic sequence of the three byte instructions is illustrated in Figure 8. These three-byte instructions exchange data between the WCR and one of the Data Registers. The WCR controls the position of the wiper. The response of the wiper to this action will be de-layed by t_{WRL}. A transfer from the WCR (current wiper

Table 3. Instruction Set

Note: 1/0 = data is one or zero

Instruction	Instruction Set								Operation
	I3	I2	I1	I0	R1	R0	WCR1/ P1	WCR0/ P0	
Read Wiper Control Register	1	0	0	1	0	0	1/0	1/0	Read the contents of the Wiper Control Register pointed to by P1-P0
Write Wiper Control Register	1	0	1	0	0	0	1/0	1/0	Write new value to the Wiper Control Register pointed to by P1-P0
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Data Register pointed to by P1-P0 and R1-R0
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Data Register pointed to by P1-P0 and R1-R0
XFR Data Register to Wiper Control Register	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the Data Register pointed to by P1-P0 and R1-R0 to its associated Wiper Control Register
XFR Wiper Control Register to Data Register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the Wiper Control Register pointed to by P1-P0 to the Data Register pointed to by R1-R0
Gang XFR Data Registers to Wiper Control Registers	0	0	0	1	1/0	1/0	0	0	Transfer the contents of the Data Registers pointed to by R1-R0 of all four pots to their respective Wiper Control Registers
Gang XFR Wiper Control Registers to Data Register	1	0	0	0	1/0	1/0	0	0	Transfer the contents of both Wiper Control Registers to their respective data Registers pointed to by R1-R0 of all four pots
Increment/Decrement Wiper Control Register	0	0	1	0	0	0	1/0	1/0	Enable Increment/decrement of the Control Latch pointed to by P1-P0

position), to a Data Register is a write to non-volatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometers and one of its associated registers; or the transfer can occur between all potentiometers and one associated register.

Four instructions require a two-byte sequence to complete, as illustrated in Figure 7. These instructions transfer data between the host/processor and the CAT5409; either between the host and one of the data registers or directly between the host and the Wiper Control Register. These instructions are:

— **XFR Data Register to Wiper Control Register**
This transfers the contents of one specified Data Register to the associated Wiper Control Register.

— **XFR Wiper Control Register to Data Register**
This transfers the contents of the specified Wiper Control Register to the specified associated Data Register.

— **Global XFR Data Register to Wiper Control Register**
This transfers the contents of all specified Data Registers to the associated Wiper Control Registers.

— **Global XFR Wiper Counter Register to Data Register**
This transfers the contents of all Wiper Control Registers to the specified associated Data Registers.

INCREMENT/DECREMENT COMMAND

The final command is Increment/Decrement (Figure 5 and 9). The Increment/Decrement command is different from the other commands. Once the command is issued and the CAT5409 has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby providing a fine tuning capability to the host. For each SCL clock pulse (t_{HIGH}) while SDA is HIGH, the selected wiper will move one resistor segment towards the R_H terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the R_L terminal.

See Instructions format for more detail.

Figure 7. Two-Byte Instruction Sequence

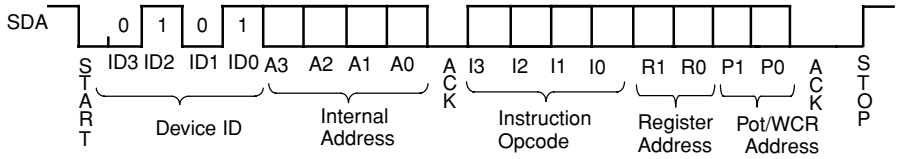


Figure 8. Three-Byte Instruction Sequence

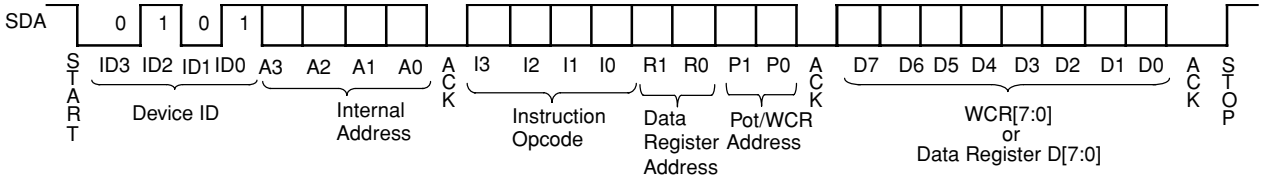


Figure 9. Increment/Decrement Instruction Sequence

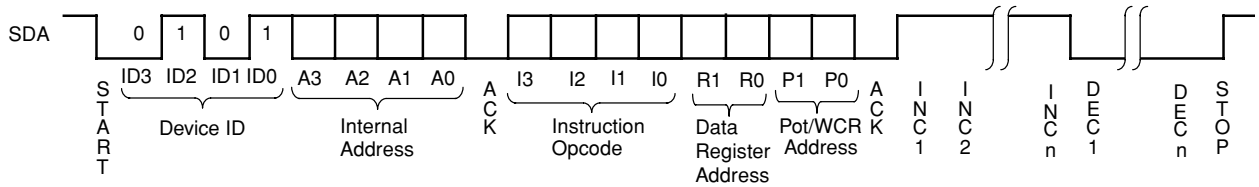
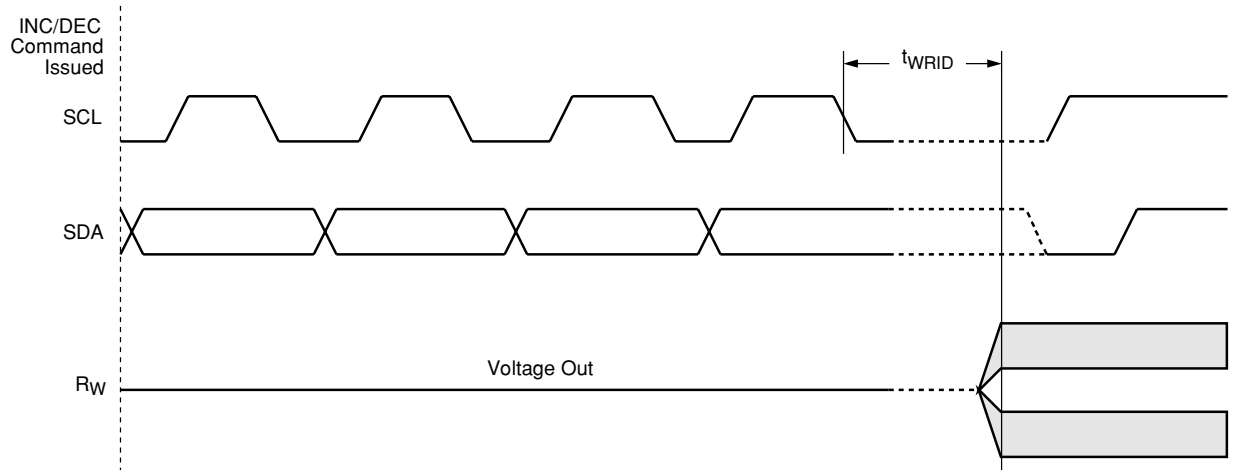


Figure 10. Increment/Decrement Timing Limits



INSTRUCTION FORMAT

Read Wiper Control Register (WCR)

S	DEVICE ADDRESSES								A	INSTRUCTION								A	DATA								A	S
T	0	1	0	1	A3	A2	A1	A0	C	1	0	0	1	0	0	P1	P0	C	7	6	5	4	3	2	1	0	C	T
A									K									K	0	0							K	O
R																												P
T																												

Write Wiper Control Register (WCR)

S	DEVICE ADDRESSES								A	INSTRUCTION								A	DATA								A	S
T	0	1	0	1	A3	A2	A1	A0	C	1	0	1	0	0	0	P1	P0	C	7	6	5	4	3	2	1	0	C	T
A									K									K	0	0							K	O
R																												P
T																												

Read Data Register (DR)

S	DEVICE ADDRESSES								A	INSTRUCTION								A	DATA								A	S
T	0	1	0	1	A3	A2	A1	A0	C	1	0	1	1	R1	R0	P1	P0	C	7	6	5	4	3	2	1	0	C	T
A									K									K	0	0							K	O
R																												P
T																												

Write Data Register (DR)

S	DEVICE ADDRESSES								A	INSTRUCTION								A	DATA								A	S
T	0	1	0	1	A3	A2	A1	A0	C	1	1	0	0	R1	R0	P1	P0	C	7	6	5	4	3	2	1	0	C	T
A									K									K	0	0							K	O
R																												P
T																												

INSTRUCTION FORMAT (continued)

Global Transfer Data Register (DR) to Wiper Control Register (WCR)

S	DEVICE ADDRESSES								A	INSTRUCTION								A	S
T	0	1	0	1	A3	A2	A1	A0	C	0	0	0	1	R1	R0	0	0	C	T
A									K									K	O
R																			P
T																			

Global Transfer Wiper Control Register (WCR) to Data Register (DR)

S	DEVICE ADDRESSES								A	INSTRUCTION								A	S
T	0	1	0	1	A3	A2	A1	A0	C	1	0	0	0	R1	R0	0	0	C	T
A									K									K	O
R																			P
T																			

Transfer Wiper Control Register (WCR) to Data Register (DR)

S	DEVICE ADDRESSES								A	INSTRUCTION								A	S
T	0	1	0	1	A3	A2	A1	A0	C	1	1	1	0	R1	R0	P1	P0	C	T
A									K									K	O
R																			P
T																			

Transfer Data Register (DR) to Wiper Control Register (WCR)

S	DEVICE ADDRESSES								A	INSTRUCTION								A	S
T	0	1	0	1	A3	A2	A1	A0	C	1	1	0	1	R1	R0	P1	P0	C	T
A									K									K	O
R																			P
T																			

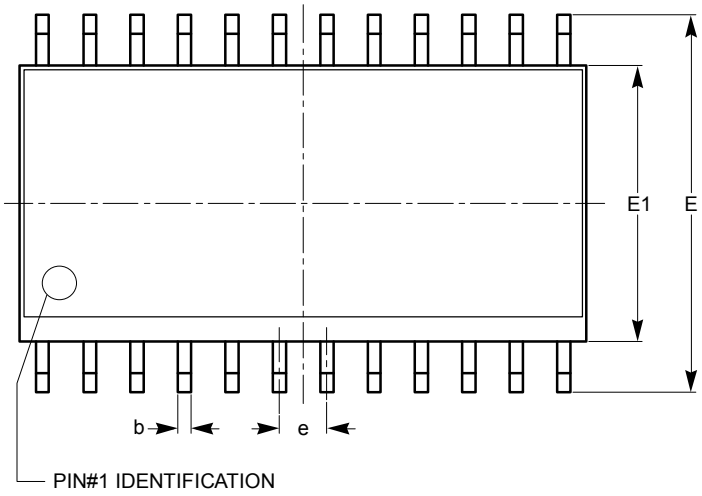
Increment (I)/Decrement (D) Wiper Control Register (WCR)

S	DEVICE ADDRESSES								A	INSTRUCTION								A	DATA					S
T	0	1	0	1	A3	A2	A1	A0	C	0	0	1	0	0	0	P1	P0	C	I/D	I/D	. . .	I/D	I/D	T
A									K									K						O
R																								P
T																								

Note:
(1) Any write or transfer to the Non-volatile Data Registers is followed by a high voltage cycle after a STOP has been issued.

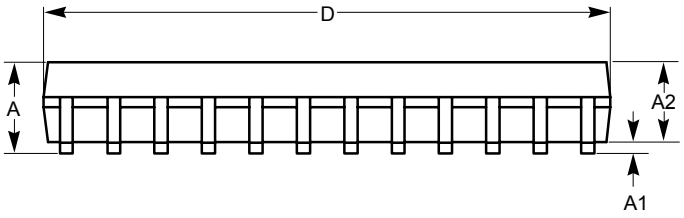
PACKAGE OUTLINE DRAWINGS

SOIC 24-Lead 300mils (W) (1)(2)

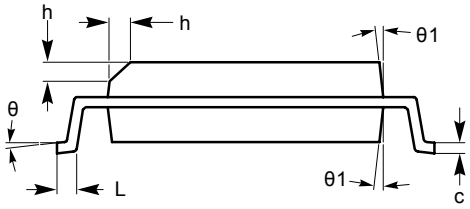


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.35		2.65
A1	0.10		0.30
A2	2.05		2.55
b	0.31		0.51
c	0.20		0.33
D	15.20		15.40
E	10.11		10.51
E1	7.34		7.60
e		1.27 BSC	
h	0.25		0.75
L	0.40		1.27
θ	0°		8°
θ1	5°		15°



SIDE VIEW

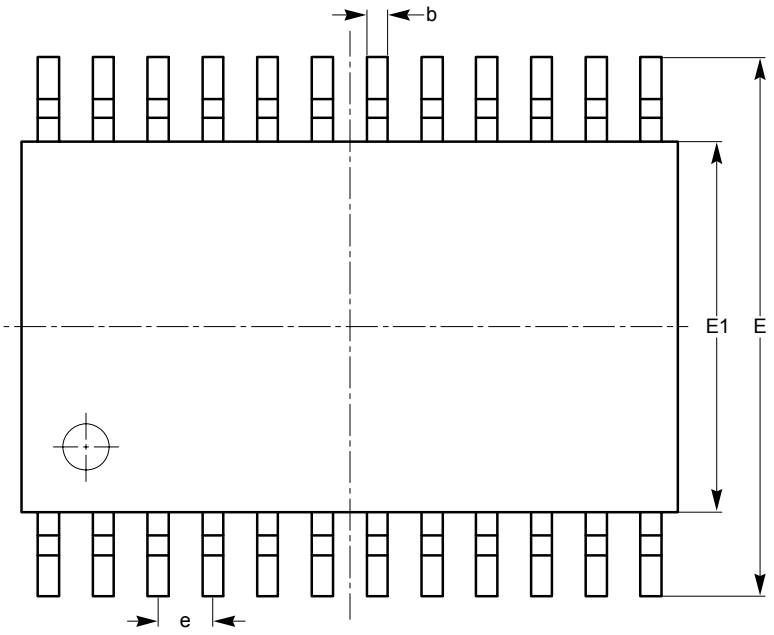


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

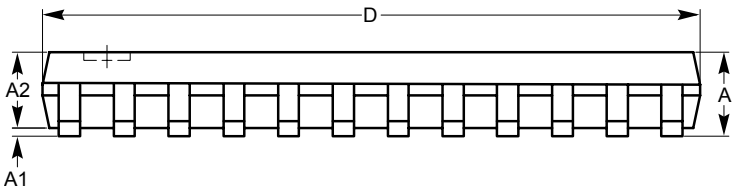
Notes:
(1) All dimensions in millimeters. Angle in degrees.
(2) Compiles with JEDEC standard MS-013.

TSSOP 24-Lead 4.4mm (Y) (1)(2)

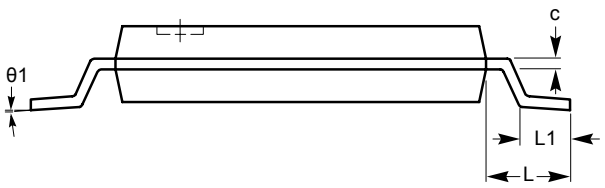


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
E	6.25	6.40	6.55
E1	4.30	4.40	4.50
e		0.65 BSC	
L		1.00 REF	
L1	0.50	0.60	0.70
θ1	0°		8°



SIDE VIEW

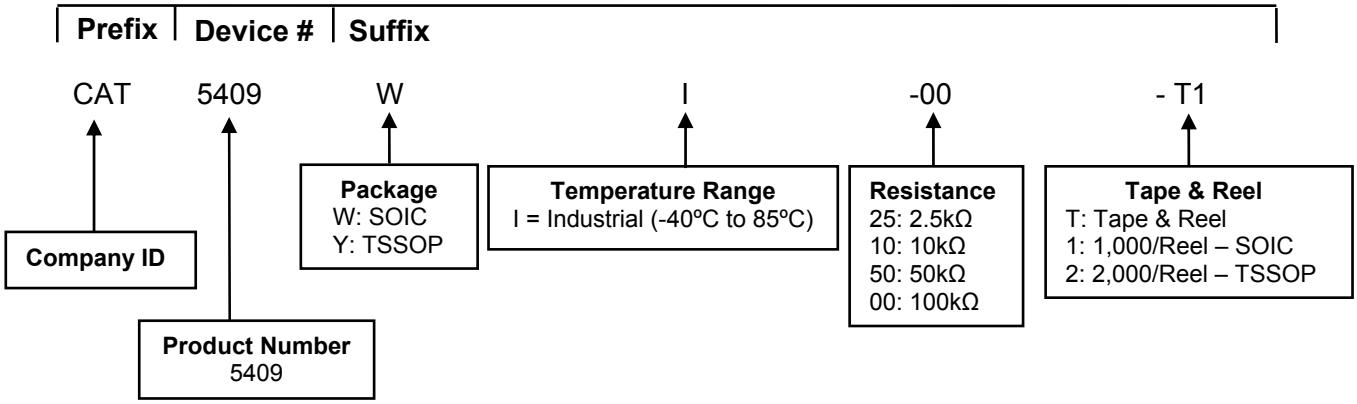


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
(1) All dimensions in millimeters. Angle in degrees.
(2) Compiles with JEDEC standard MO-153.

EXAMPLE OF ORDERING INFORMATION



ORDERING PART NUMBER

Part Number	Resistance	Package
CAT5409WI-25	2.5kΩ	SOIC
CAT5409WI-10	10kΩ	
CAT5409WI-50	50kΩ	
CAT5409WI-00	100kΩ	
CAT5409YI-25	2.5kΩ	TSSOP
CAT5409YI-10	10kΩ	
CAT5409YI-50	50kΩ	
CAT5409YI-00	100kΩ	

Notes:
(1) All packages are RoHS-compliant (Lead-free, Halogen-free).
(2) The standard lead finish is Matte-Tin.
(3) The device used in the above example is a CAT5409WI-00-T1 (SOIC, Industrial Temperature, 100kΩ, Tape & Reel, 1,000/Reel).
(4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

REVISION HISTORY

Date	Rev.	Reason
10/8/2003	H	Updated Features Updated Description
04/29/06	I	Changed Preliminary designation to Final Eliminated Commercial temp range in all areas Updated $\overline{WP}$ Pin Description Updated notes in Absolute Max Ratings and Potentiometer Characteristics
02/05/2008	J	Deleted BGA package Updated Potentiometer Characteristics table Update Package Outline Drawings Updated Example of Ordering Information Added MD- to document number
04/07/2008	K	Change 2-wire with I²C Update Ordering Part Number table

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