MP6516

35V, 2.8A, ½-H control H-Bridge Motor Driver in a TSSOP-16 EP Package

The Future of Analog IC Technology®

DESCRIPTION

The MP6516 is an H-bridge motor driver that operates from a supply voltage up to 35V and delivers a motor current up to 2.8A. Typically, the MP6516 is used to drive a DC brush motor. For the MP6516, control of each half-bridge is independent, using IN1, IEN1, IN2, and EN2 pins.

An internal current-sensing circuit provides an output voltage proportional to the load current. The MP6516 also has cycle-by-cycle current regulation and limiting. These features do not require the use of a low-ohm shunt resistor.

Full protection features include over-current protection (OCP), input over-voltage protection (OVP), under-voltage lockout (UVLO), and thermal shutdown.

The MP6516 is available in a 16-pin TSSOP-EP (5.0mmx6.4mm) with an exposed thermal pad.

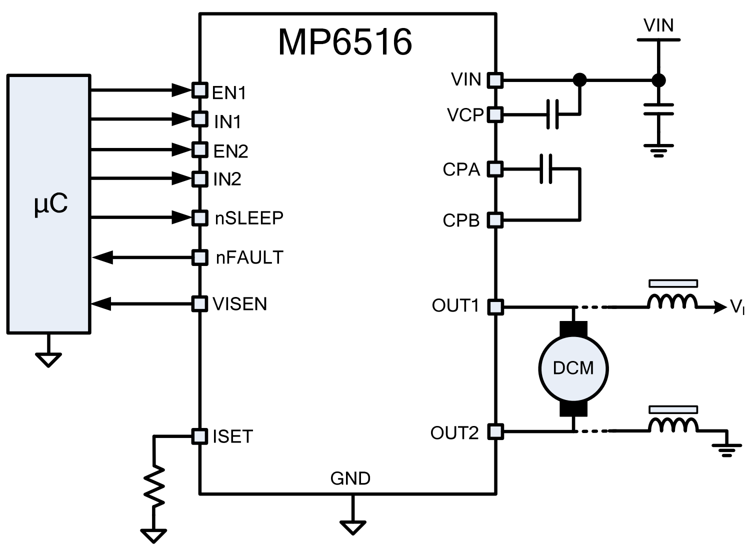
FEATURES

- Wide 5.4V to 35V Input Voltage Range
- 2.8A Peak Output Current
- ½-H control, input logic (INx, ENx)
- Internal Full H-Bridge Driver
- Cycle-by-cycle Current Regulation / Limit
- Low On Resistance (HS:250mΩ, LS:250mΩ)
- Simple, Versatile Logic Interfaces
- 3.3V and 5V Compatible Logic Supply
- Over-Current Protection (OCP)
- Over-Voltage Protection (OVP)
- Thermal Shutdown
- Under-Voltage Lockout (UVLO)
- Fault Indication Output
- Available in a Thermally Enhanced Surface-Mounted TSSOP-16 EP Package

APPLICATIONS

- Solenoid Drivers
- DC Brush Motor Drivers

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking
MP6516GF	TSSOP-16 EP	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP6516GF–Z)

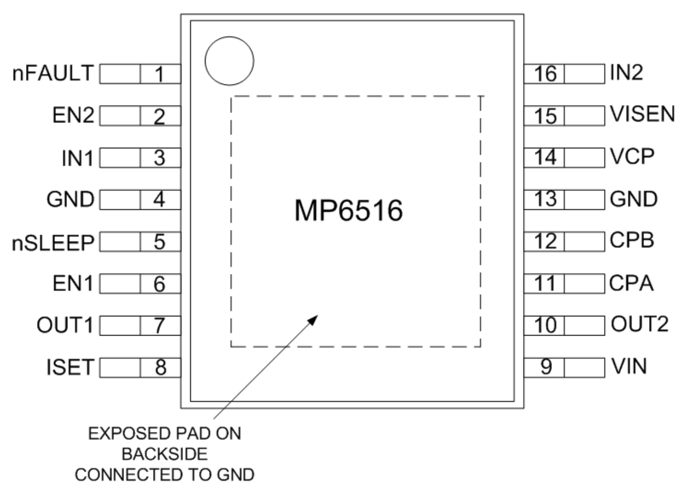
TOP MARKING

MPSYYWW
MP6516
LLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP6516: Part number
LLLLLL: Lot number

PACKAGE REFERENCE

TOP VIEW



TSSOP-16 EP

ABSOLUTE MAXIMUM RATINGS [1]

Supply voltage (VIN) ....-0.3V to 40V
OUTX voltage ($V_{OUT1/2}$) ....-0.7V to 40V
VCP, CPB ....V_{IN} to V_{IN} + 6.5V
ESD rating (HBD).. 2kV
ISET ....-0.3V to 4.5V
All other pins to GND ....-0.3V to 6.5V
Continuous power dissipation (T_A = +25°C) [2]
.... 2.77W
Storage temperature .... -55°C to +150°C
Junction temperature .... +150°C
Lead temperature (solder) .... +260°C

Recommended Operating Conditions [3]

Supply voltage (VIN) ....5.4V to 35V
Continuous output current (I_{OUT}) .... ±1.5A
Load current (I_{VISEN}) .... ±2mA
Operating junction temp. (T_J)... -40°C to +125°C

Thermal Resistance [4]

	θ_{JA}	θ_{JC}	
TSSOP-16 EP	45	10	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_A = +25°C, unless otherwise noted.

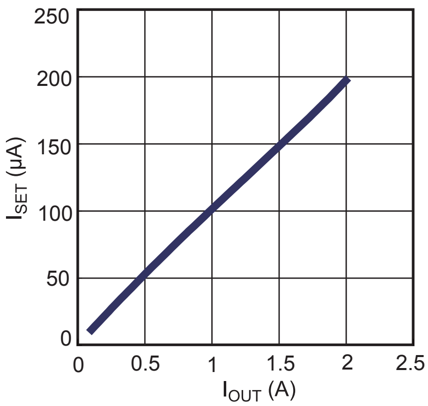
Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply						
Input supply voltage	V_{IN}		5.4	24	35	V
Quiescent current	I_Q	V_{IN} = 24V, nSLEEP = 1, no load current		1.6	2.2	mA
	I_{SLEEP}	V_{IN} = 24V, nSLEEP = 0			1	µA
Charge pump frequency	f_{CP}			680		kHz
Internal MOSFETs						
Output on resistance	R_{HS}	V_{IN} = 24V, I_{OUT} = 1A, T_J = 25°C		0.25	0.3	Ω
		V_{IN} = 24V, I_{OUT} = 1A, T_J = 85°C		0.3		Ω
	R_{LS}	V_{IN} = 24V, I_{OUT} = 1A, T_J = 25°C		0.25	0.3	Ω
		V_{IN} = 24V, I_{OUT} = 1A, T_J = 85°C		0.3		Ω
Body diode forward voltage	V_F	I_{OUT} = 1.5A			1.1	V
Control Logic						
Input logic low threshold	V_{IL}				0.8	V
Input logic high threshold	V_{IH}		2			V
Logic input current	$I_{IN(H)}$	V_{IH} = 5V	-20		20	µA
	$I_{IN(L)}$	V_{IL} = 0.8V	-20		20	µA
Internal pull down resistance	R_{PD}			515		kΩ
nFault Output (Open-Drain Output)						
Output low voltage	V_{OL}	I_O = 5mA			0.5	V
Output high leakage current	I_{OH}	V_O = 3.3V			1	µA
Protection Circuits						
UVLO rising threshold	V_{IN_RISE}		4.7	5	5.3	V
UVLO hysteresis	V_{HYS}			310		mV
Input OVP threshold	V_{OVP}		36	38	40	V
Input OVP hysteresis	ΔV_{OVP}			2000		mV
Over-current trip level	I_{OCP1}	Sinking	3.2	4	5.3	A
	I_{OCP2}	Sourcing	3.2	4	5.3	A
Over-current deglitch time (5)	t_{OCPD}			500		ns
Over-current retry time	t_{OCPR}			0.9		ms
Thermal shutdown	T_{TSD}			165		°C
Thermal shutdown hysteresis	ΔT_{TSD}			30		°C
Current Control						
Off time	t_{ITRIP}	After ITRIP		0.9		ms
ISET current	I_{ISET}		90	100	110	µA/A
Current trip voltage	V_{ITRIP}	At VISEN	1.44	1.5	1.56	V
VISEN Output						
Output voltage accuracy	ΔV_{VISEN}	V_{ISET} > 0.5V	-5		5	%

note:

5) Guaranteed by design.

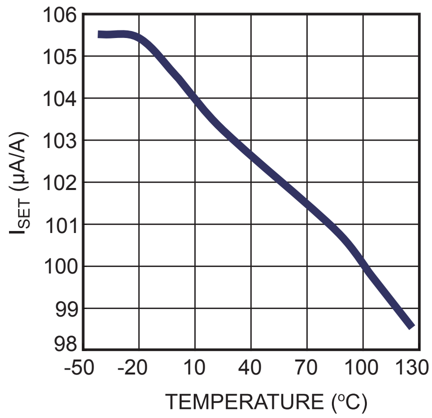
TYPICAL CHARACTERISTICS

Current Sense

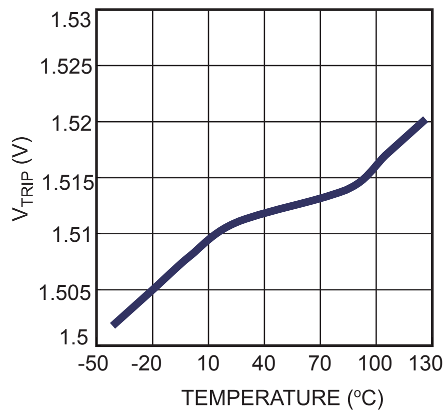


I_{SET} Ratio vs. Temperature

I_{OUT}=1A

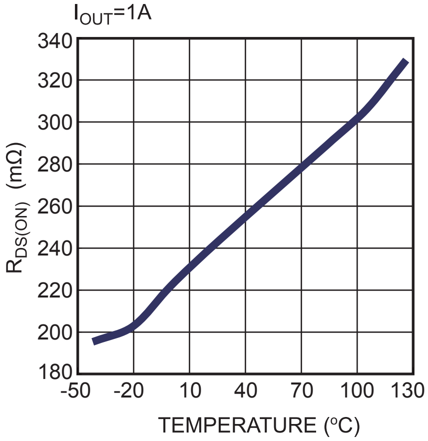


Current Trip Voltage vs. Temperature



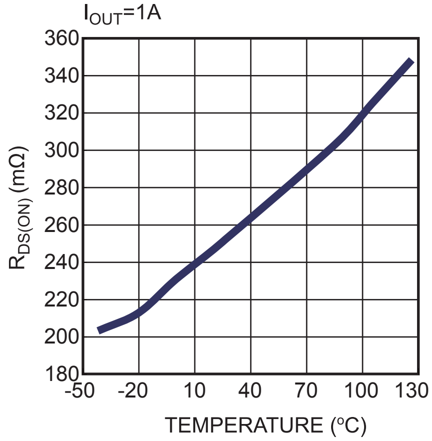
HS R_{ON} vs. Temperature

I_{OUT}=1A



LS R_{ON} vs. Temperature

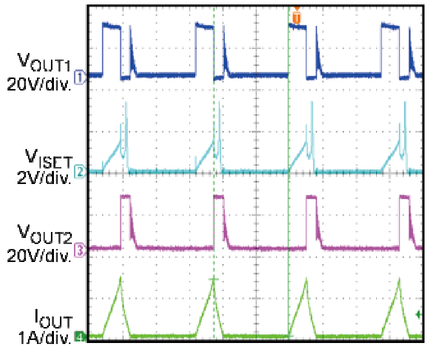
I_{OUT}=1A



TYPICAL PERFORMANCE CHARACTERISTICS

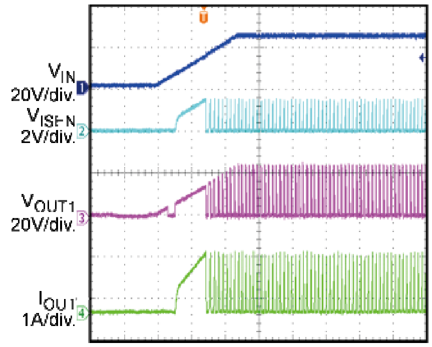
V_{IN} = 24V, I_{OUT} = 1A, T_A = 25°C, unless otherwise noted.

Steady State



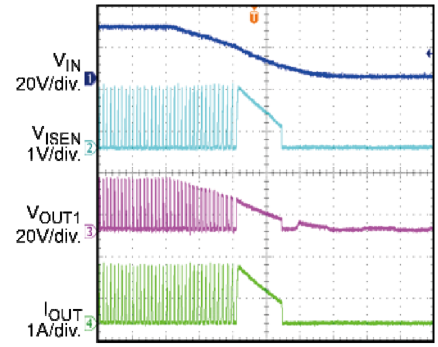
400μs/div.

Input Power Start-Up



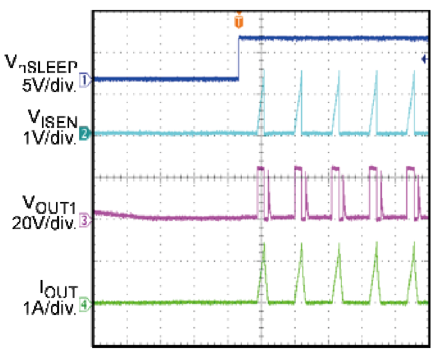
10ms/div.

Input Power Shutdown



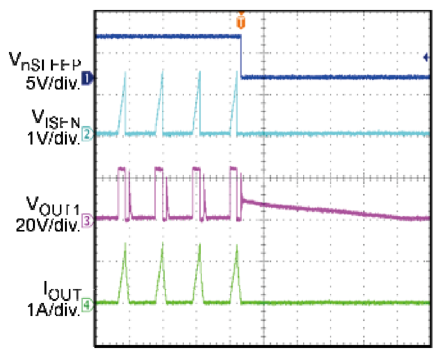
10ms/div.

Sleep Start-Up



1ms/div.

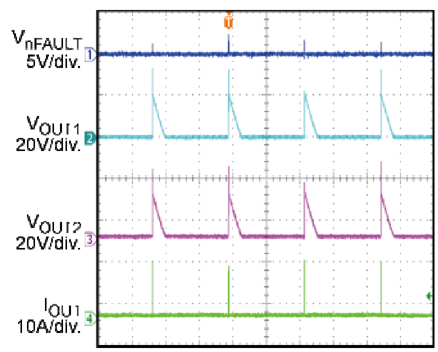
Sleep Shutdown



1ms/div.

SCP

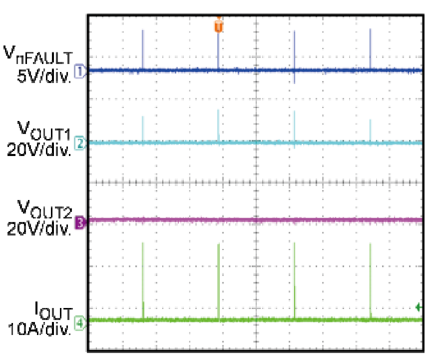
V_{IN} = 35V, EN1 = EN2 = IN1 = 5V, IN2 = 0V, OUT1 Short to OUT2



400μs/div.

SCP

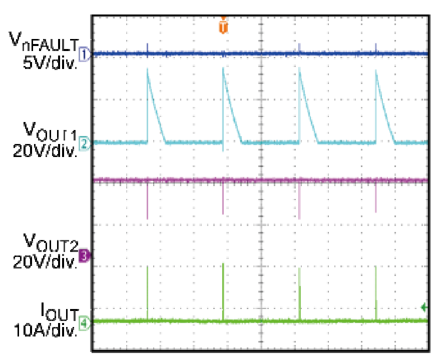
V_{IN} = 35V, EN1 = EN2 = IN1 = 5V, IN2 = 0V, OUT1 Short to GND



400μs/div.

SCP

V_{IN} = 35V, EN1 = EN2 = IN1 = 5V, IN2 = 0V, OUT2 Short to VIN



400μs/div.

PIN FUNCTIONS

Pin #	Name	Description
1	nFAULT	**Fault indication.** nFAULT is an open-drain output type. nFAULT is logic low when in a fault condition (i.e.: OCP, OTP, OVP).
2	EN2	**Output 2 enable input.** Drive EN2 high to enable OUT2. EN2 is pulled down internally.
3	IN1	**Output 1 control input.** IN1 is pulled down internally.
4, 13	GND	**System ground connection.**
5	nSLEEP	**Sleep mode input.** Drive nSLEEP to logic low to enter low-power sleep mode. nSLEEP is pulled down internally.
6	EN1	**Output 1 enable input.** Drive EN1 high to enable OUT1. EN1 is pulled down internally.
7	OUT1	**Output terminal 1.**
8	ISET	**Current programming resistor.** Connect a resistor to ground to set the current limit and VISEN output voltage.
9	VIN	**Input supply voltage.** Decouple VIN to GND with a minimum 100nF ceramic capacitor to GND.
10	OUT2	**Output terminal 2.**
11	CPA	**Charge pump flying capacitor.** Connect a 100nF ceramic capacitor between CPA and CPB.
12	CPB	
14	VCP	**Charge pump output.** Connect a 1µF capacitor to VIN.
15	VISEN	**Current sense output voltage.**
16	IN2	**Output 2 control input.** IN2 is pulled down internally.
EP	GND	**Exposed pad.** The exposed pad must be connected to ground.

BLOCK DIAGRAM

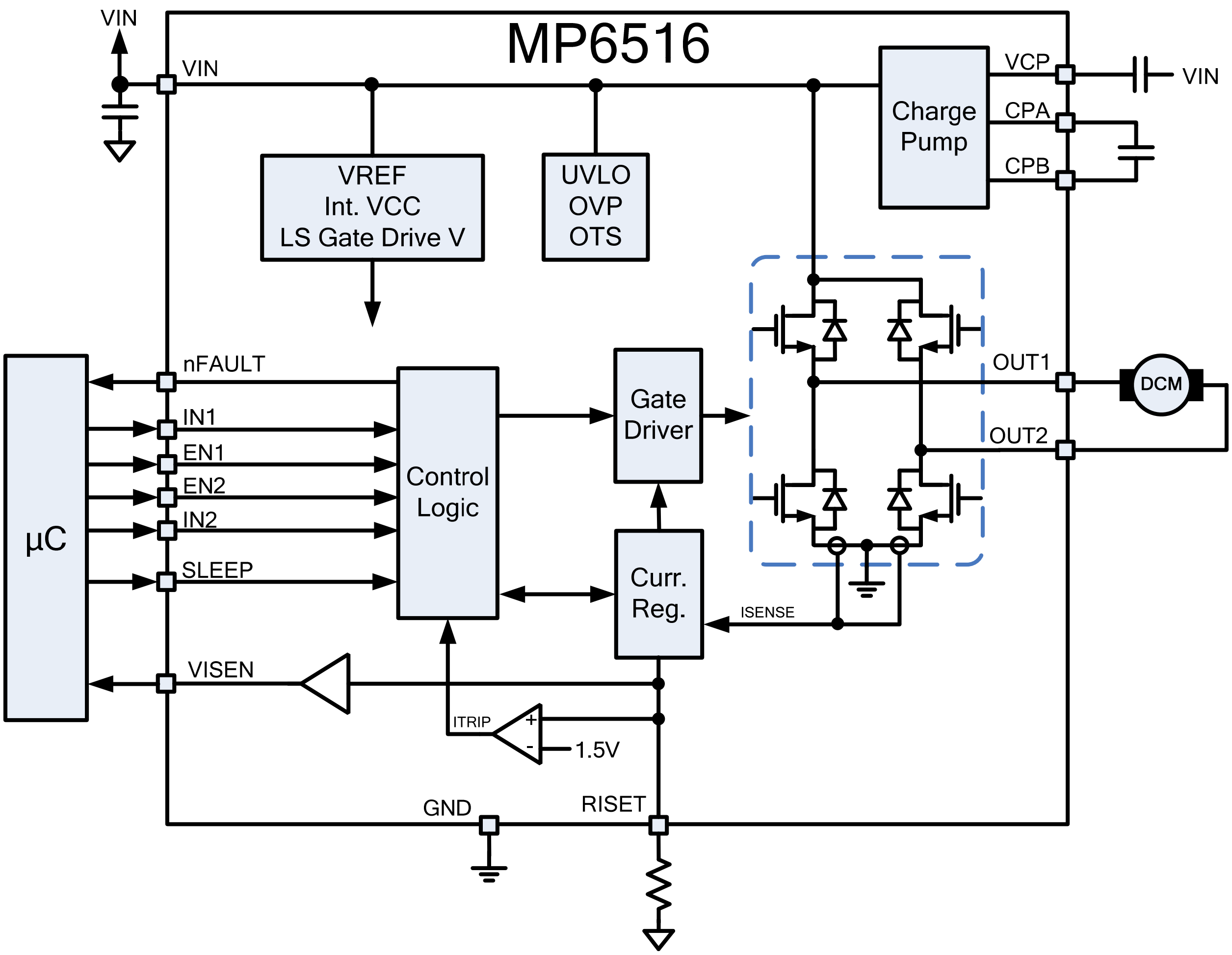


Figure 1: Functional Block Diagram

OPERATION

The MP6516 is an H-bridge motor driver that integrates four N-channel power MOSFETs with 2.8A of peak current capability. The MP6516 operates over a wide 5.4V to 35V input voltage range and is designed to drive bipolar stepper motors, DC brush motors, solenoids, or other loads.

Current Sensing

The current flowing into the two low-side MOSFETs (LS-FET) is sensed with an internal current sensing circuit. A voltage proportional to the output currents is sourced on VISEN.

VISEN output voltage scaling is set by a resistor connected between ISET and ground. For 1A of output current, 100μA of current is sourced into the resistor connected to ISET. For example, if a 10kΩ resistor is connected between ISET and ground, the output voltage on VISEN is 1V/A of output current. Current is sensed when one of the LS-FETs is turned on. The load current applied to VISEN should be kept below 2mA with no more than 500pF of capacitance.

Current Limit and Regulation

The current in the outputs is limited using constant-off-time pulse-width modulation (PWM) control circuitry. Initially, a diagonal pair of MOSFETs turns on and drives current through the load. The current increases in the load, which is sensed by the internal current-sense circuit. If the load current reaches the current trip threshold, the entire H-bridge switches to a high impedance with all MOSFETs turned off. After a fixed off-time (t_{ITRIP}), the MOSFETs are re-enabled, and the cycle repeats.

Note that the current is sensed only in the LS-FETs. If the outputs are used to drive a load that is connected to ground directly, the current regulation and current measurement do not function.

The current limit threshold is reached when VISET reaches 1.5V. For example, with a 10kΩ resistor from ISET to ground, the VISET voltage is 1V/A of the output current. Therefore, when the current reaches 1.5A, the VISET voltage reaches 1.5V, and a current trip occurs.

Blanking Time

There is often a current spike during turn-on due to the body diode's reverse-recovery current or the shunt capacitance of the load. This current spike requires filtering to prevent it from shutting down the high-side MOSFET (HS-FET) erroneously. An internal, fixed, blanking time (t_{OCPD}) blanks the output of the current sense comparator when the outputs are switched. This blanking time also sets the minimum on time for the HS-FET.

Input Logic

For the MP6516, control of each half-bridge is independent, using IN1, IEN1, IN2, and EN2 (see Table 1).

Table 1: Truth Table

ENx	INx	OUTx
0	0	Z
0	1	Z
1	0	L
1	1	H

nSLEEP Operation

Driving nSLEEP low puts the MP6516 into a low-power sleep state. In this state, all internal circuits including the gate drive charge pump are disabled, and the H-bridge outputs are turned off. All inputs are ignored when nSLEEP is active low. When waking up from sleep mode, approximately 1ms of time must pass before the outputs operate.

Fault Indicator (nFAULT)

The MP6516 provides an nFAULT pin that is driven active low if any of the protection circuits are activated. These fault conditions include over-current, over-temperature, and over-voltage. nFAULT is also driven low when a current-limit trip occurs. nFAULT is an open-drain output and requires an external pull-up resistor. When the fault condition is removed, nFAULT is pulled inactive high by the pull-up resistor.

Over-Current Protection (OCP)

The over-current protection (OCP) circuit limits the current through each MOSFET by reducing the gate drive voltage to the MOSFET. If the MOSFET remains in the current-limit condition for longer than the over-current deglitch time, all MOSFETs in the H-bridge are disabled, and nFAULT is driven low. The driver remains disabled for t_{OCP} and is re-enabled automatically. Over-current conditions are sensed on both high- and low-side devices. A short to ground, supply, or across the motor winding results in an over-current shutdown. Note that OCP does not use the current sense circuitry used for the PWM current control and is independent of the ISET resistor value.

Over-Voltage Protection (OVP)

If the input voltage applied to VIN is higher than the OVP threshold, the H-bridge output is disabled, and nFAULT is driven low. This protection is released when VIN drops to a safe level.

Input Under-Voltage Lockout (UVLO)

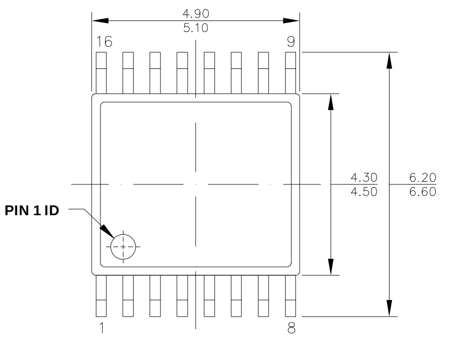
If the voltage on VIN falls below the under-voltage lockout (UVLO) threshold at any time, all circuitry in the device is disabled, and the internal logic is reset. Operation resumes when VIN rises above the UVLO threshold.

Thermal Shutdown

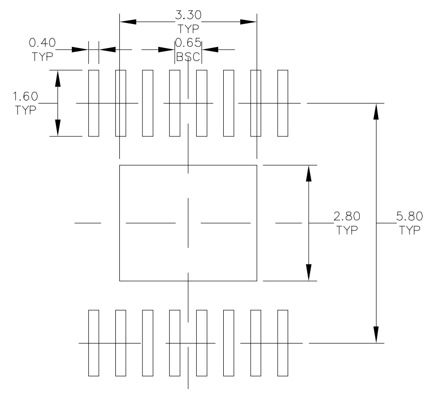
If the die temperature exceeds safe limits, all MOSFETs in the H-bridge are disabled, and nFAULT is driven low. Once the die temperature has fallen to a safe level, operation resumes automatically.

PACKAGE INFORMATION

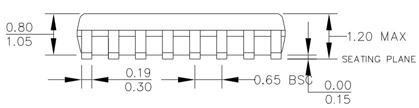
TSSOP-16 EP (5.0mmx6.4mm)



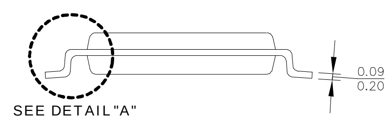
TOP VIEW



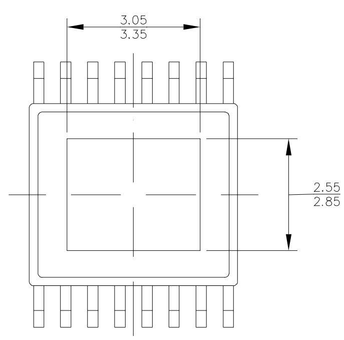
RECOMMENDED LAND PATTERN



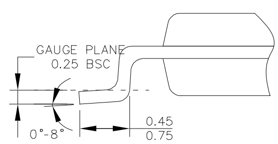
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WITDH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
6) DRAWING IS NOT TO SCALE