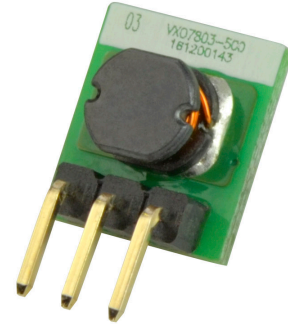


SERIES: VX078-500 | **DESCRIPTION:** NON-ISOLATED DC SWITCHING REGULATOR

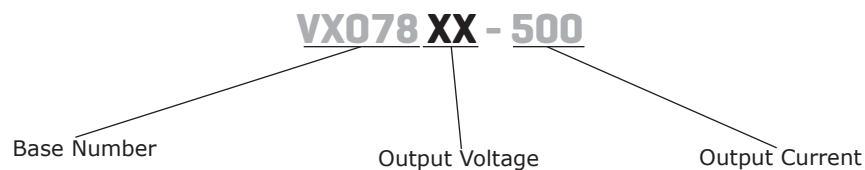
FEATURES

- wide input
- pin-out compatible with linear regulators
- open frame
- UL & CSA approved
- high efficiency up to 95%
- no-load input current as low as 0.2 mA
- wide operating temp: -40°C to +85°C
- supports negative output
- short circuit protection on the output
- EN 62368-1


MODEL

| | input voltage ¹ | | output voltage (Vdc) | output current max (mA) | output power max (W) | ripple & noise ² max (mVp-p) | efficiency ³ typ (%) |
|--------------|----------------------------|----------------|-------------------------|-------------------------------|----------------------------|---|---------------------------------------|
| | typ (Vdc) | range (Vdc) | | | | | |
| VX07803-500 | 24 | 4.75~36 | 3.3 | 500 | 1.65 | 75 | 86 |
| VX07805-500 | 24 | 6.5~36 | 5 | 500 | 2.5 | 100 | 90 |
| | 12 | 7~31 | -5 | -300 | 1.5 | 100 | 80 |
| VX078012-500 | 24 | 15~36 | 12 | 500 | 6 | 75 | 94 |
| | 12 | 8~24 | -12 | -150 | 1.8 | 75 | 84 |
| VX078015-500 | 24 | 19~36 | 15 | 500 | 7.5 | 75 | 95 |
| | 12 | 8~21 | -15 | -150 | 2.25 | 75 | 85 |

- Notes:
1. For input voltages higher than 30 Vdc, a 22 μ F / 50 V input capacitor is required.
 2. Tested at nominal input, 10~100% load, 20 MHz bandwidth, with 10 μ F electrolytic and 1 μ F ceramic capacitor on the output. At loads below 10%, the max ripple and noise of the 3.3 & 5 Vdc outputs will be 150 mVp-p, and the other outputs will be 2% Vo.
 3. Measured at min Vin, full load.
 4. All specifications are measured at Ta=25°C, humidity < 75%, nominal input voltage, and rated output load unless otherwise specified.

PART NUMBER KEY


INPUT

| parameter | conditions/description | min | typ | max | units |
|--------------------------------------|----------------------------------|------|-----|-----|-------|
| operating input voltage ¹ | for positive output applications | 4.75 | 24 | 36 | Vdc |
| | for negative output applications | 7 | 12 | 31 | Vdc |
| filter | capacitor filter | | | | |
| input reverse polarity protection | no | | | | |
| no-load input current | positive outputs | | | | |
| | 5 Vdc output model | | 5.0 | 8.0 | mA |
| | all other output models | | 0.2 | 1.5 | mA |

Note: 1. See Model section on page 1 for specific input voltage ranges.

OUTPUT

| parameter | conditions/description | min | typ | max | units |
|--------------------------------------|--|-----|------|-------|-------|
| maximum capacitive load ² | for positive output applications | | | 680 | μF |
| | for negative output applications | | | 330 | μF |
| voltage accuracy | at full load, input voltage range | | ±2 | ±4 | % |
| | 3.3 Vdc output model | | ±2 | ±3 | % |
| | all other models | | | | |
| line regulation | at full load, input voltage range | | ±0.2 | ±0.4 | % |
| load regulation | at nominal input, 10~100% load | | ±0.4 | ±0.6 | % |
| switching frequency | at nominal input voltage, full load | | | | |
| | 5 Vdc output model | 750 | | 1,250 | kHz |
| | all other output models | 550 | | 850 | kHz |
| transient recovery time | at nominal input voltage, 25% load step change | | 0.2 | 1 | ms |
| transient response deviation | at nominal input voltage, 25% load step change | | 50 | 250 | mV |
| temperature coefficient | at full load | | | ±0.03 | %/°C |

Note: 2. The maximum capacitive load was tested at nominal input voltage, full load.

PROTECTIONS

| parameter | conditions/description | min | typ | max | units |
|--------------------------|---------------------------|-----|-----|-----|-------|
| short circuit protection | continuous, auto recovery | | | | |

SAFETY AND COMPLIANCE

| parameter | conditions/description | min | typ | max | units |
|----------------------------------|---|-----------|-----|-----|-------|
| safety approvals | certified to 62368-1: EN certified to 60950-1: UL | | | | |
| EMI/EMC | EN 55032, EN 55024 | | | | |
| conducted emissions ³ | CISPR22/EN55022, class B (external circuit required, see Figure 6-b) | | | | |
| radiated emissions ³ | CISPR22/EN55022, class B (external circuit required, see Figure 6-b) | | | | |
| ESD | IEC/EN61000-4-2, contact ± 4kV, class B | | | | |
| radiated immunity | IEC/EN61000-4-3, 10V/m, class A | | | | |
| EFT/burst | IEC/EN61000-4-4, ± 1kV, class B (external circuit required, see Figure 6-a) | | | | |
| surge | IEC/EN61000-4-5, line-line ± 1kV, class B (external circuit required, see Figure 6-a) | | | | |
| conducted immunity | IEC/EN61000-4-6, 3 Vr.m.s, class A | | | | |
| MTBF | as per MIL-HDBK-217F, 25°C | 2,000,000 | | | hours |
| RoHS | 2011/65/EU | | | | |

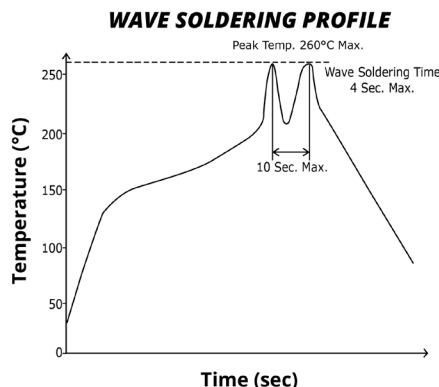
Note: 3. CISPR22/EN55022, class A for the 5 Vdc output model.

ENVIRONMENTAL

| parameter | conditions/description | min | typ | max | units |
|-----------------------|------------------------|-----|-----|-----|-------|
| operating temperature | see derating curve | -40 | | 85 | °C |
| storage temperature | | -55 | | 125 | °C |
| storage humidity | non-condensing | 5 | | 95 | % |

SOLDERABILITY

| parameter | conditions/description | min | typ | max | units |
|----------------|----------------------------|-----|-----|-----|-------|
| wave soldering | see wave soldering profile | | | 260 | °C |



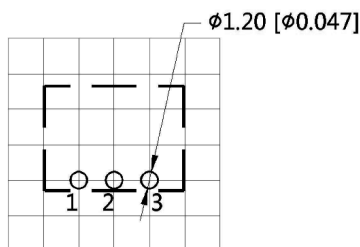
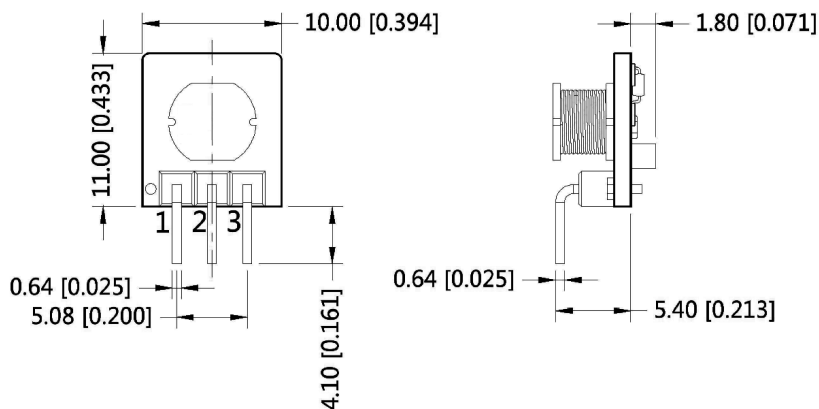
MECHANICAL

| parameter | conditions/description | min | typ | max | units |
|------------|---|-----|-----|-----|-------|
| dimensions | 10.00 x 7.20 x 11.00 [0.394 x 0.283 x 0.433 inch] | | | | mm |
| weight | | | 1.0 | | g |

MECHANICAL DRAWING

units: mm [inch]
 tolerance: ± 0.50 [± 0.020]
 pin diameter tolerance: ± 0.10 [± 0.004]

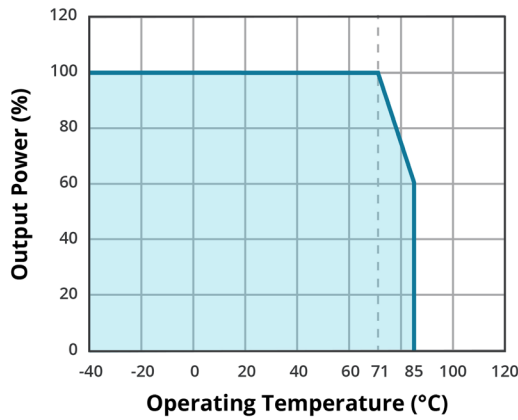
| PIN CONNECTIONS | | |
|-----------------|---------|---------|
| PIN | +OUTPUT | -OUTPUT |
| 1 | +VIN | +VIN |
| 2 | GND | -VOUT |
| 3 | +VOUT | GND |



Note : Grid 2.54*2.54mm
 Recommended PCB Layout
 Top View

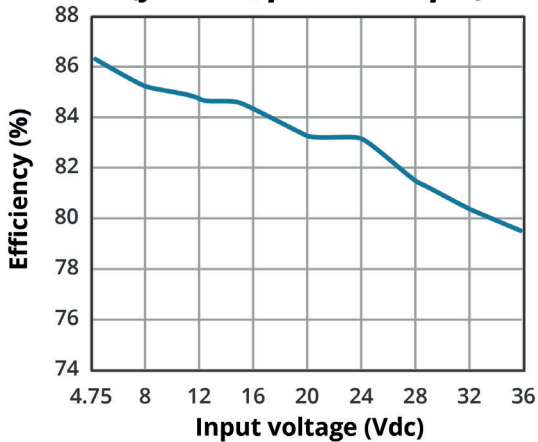
DERATING CURVE

TEMPERATURE DERATING CURVE

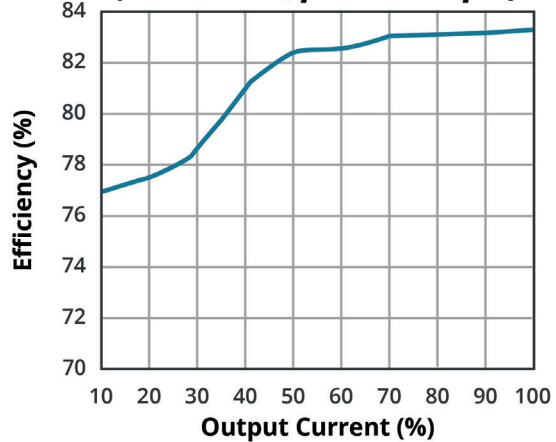


EFFICIENCY CURVES

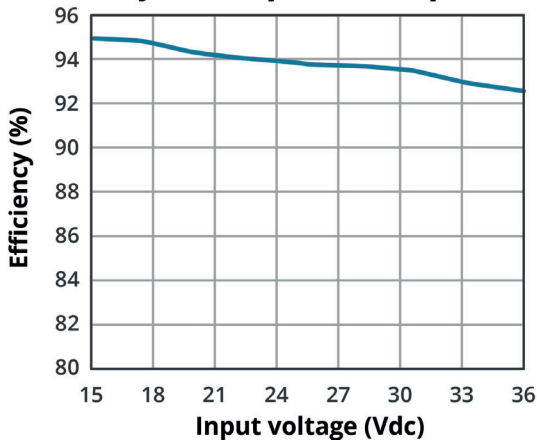
**EFFICIENCY VS INPUT LOAD
VX07803-500
(full load, positive output)**



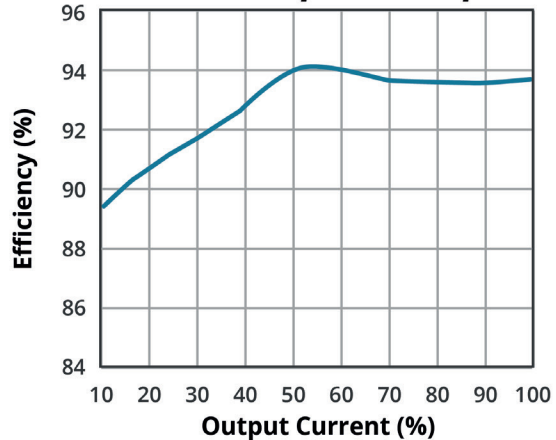
**EFFICIENCY VS OUTPUT LOAD
VX07803-500
(nominal Vin, positive output)**



**EFFICIENCY VS INPUT LOAD
VX078012-500
(full load, positive output)**

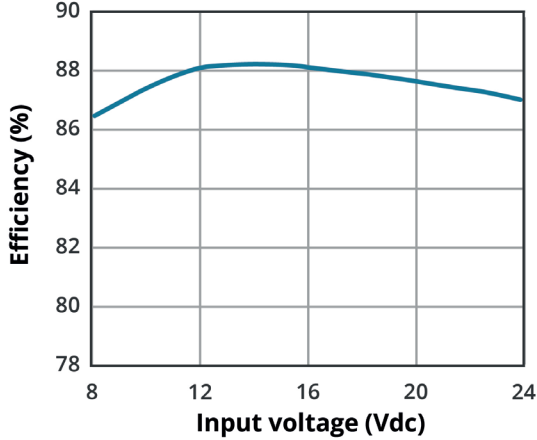


**EFFICIENCY VS OUTPUT LOAD
VX078012-500
(nominal Vin, positive output)**

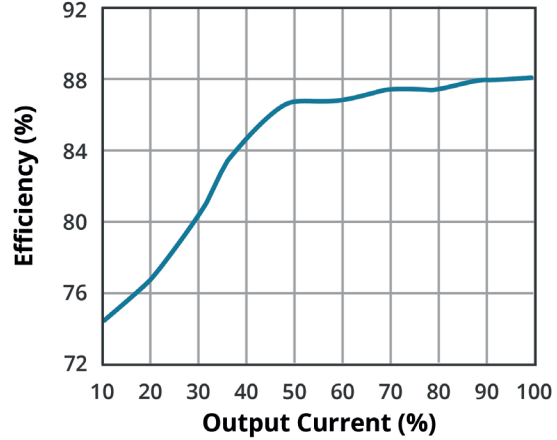


EFFICIENCY CURVES (CONTINUED)

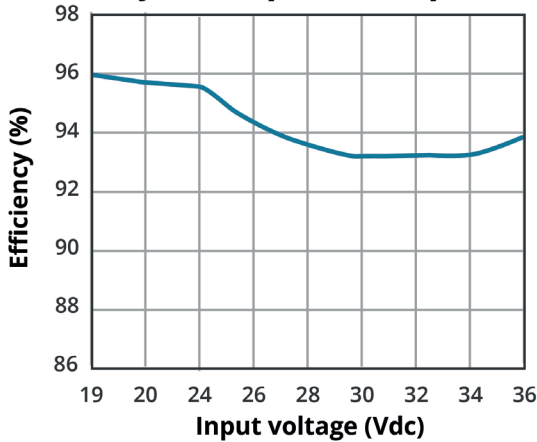
**EFFICIENCY VS INPUT LOAD
VX078012-500
(full load, negative output)**



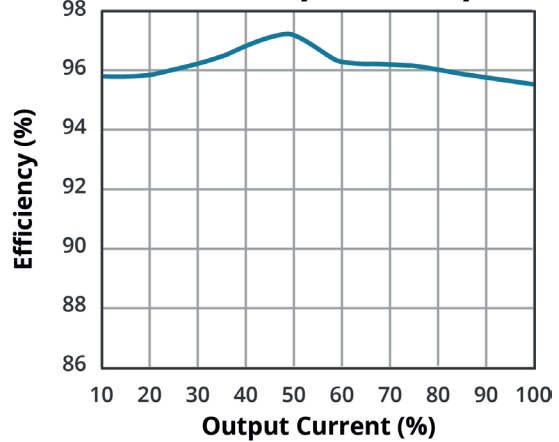
**EFFICIENCY VS OUTPUT LOAD
VX078012-500
(nominal Vin, negative output)**



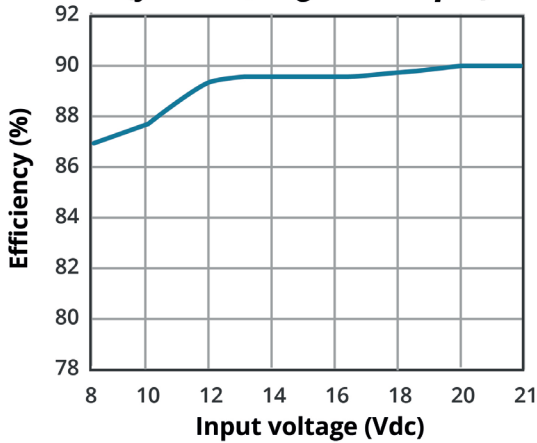
**EFFICIENCY VS INPUT LOAD
VX078015-500
(full load, positive output)**



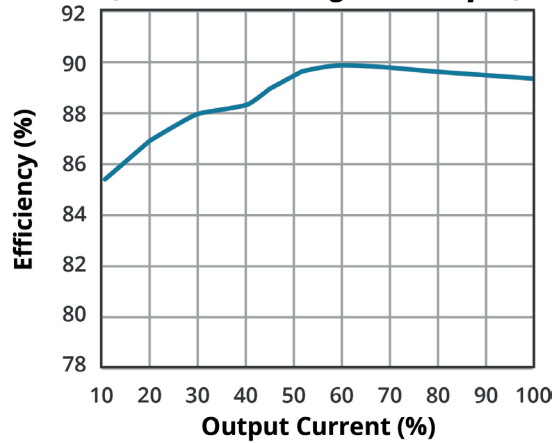
**EFFICIENCY VS OUTPUT LOAD
VX078015-500
(nominal Vin, positive output)**



**EFFICIENCY VS INPUT LOAD
VX078015-500
(full load, negative output)**



**EFFICIENCY VS OUTPUT LOAD
VX078015-500
(nominal Vin, negative output)**



TYPICAL APPLICATION CIRCUIT

Figure 1

Positive Output Application Circuit

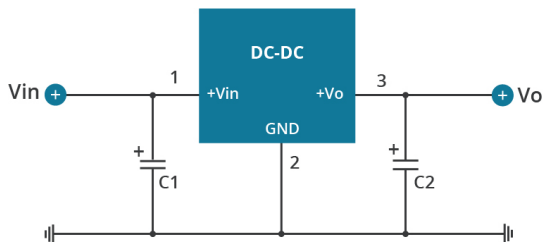


Figure 3

Positive and Negative Output Paralleling Application Circuit

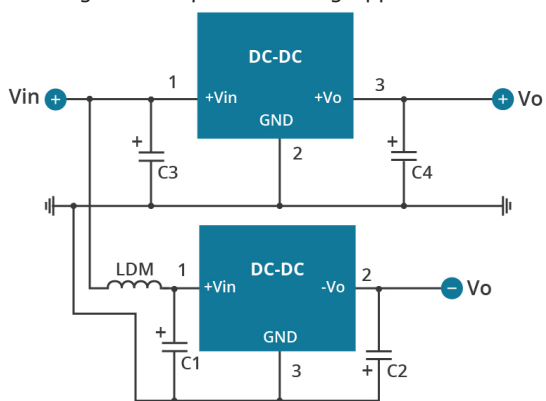


Figure 4

Positive Output Ripple Reduction Circuit

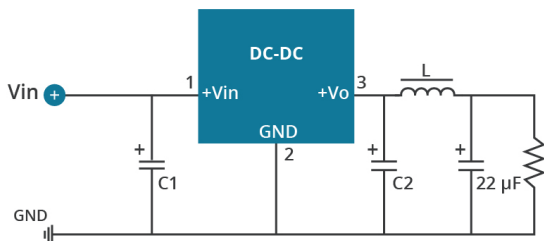


Figure 2

Negative Output Application Circuit

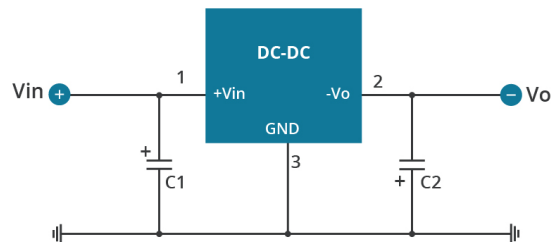


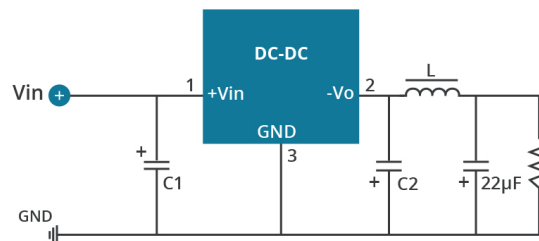
Table 1

External Capacitor Table

| Model Number | C1, C3 (ceramic capacitor) | C2, C4 (ceramic capacitor) |
|--------------|-------------------------------|-------------------------------|
| VX07803-500 | 10 μF/50 V | 22 μF/10 V |
| VX07805-500 | 10 μF/50 V | 22 μF/10 V |
| VX078012-500 | 10 μF/50 V | 22 μF/25 V |
| VX078015-500 | 10 μF/50 V | 22 μF/25 V |

Figure 5

Negative Output Ripple Reduction Circuit



EMC RECOMMENDED CIRCUIT

Figure 6

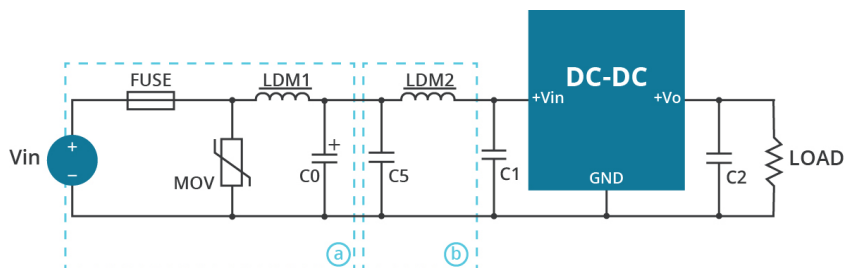


Table 2

| Recommended external circuit components | |
|---|--|
| FUSE | choose according to actual input current |
| MOV | S20K30 |
| LDM1 | 82 μH |
| C0 | 680 μF/50 V |
| C1, C2 | see Table 1 |
| C5 | 4.7 μF/50 V |
| LDM2 | 12 μH |

- Note:
1. C1 & C2 (C3 & C4) are required and should be connected as close to the module pins as possible.
 2. To reduce the output ripple further, it is recommended to connect an "LC" filter at the output terminal with a recommended value of 10~47 μH for the L component. (See Figures 4 & 5).
 3. When using application circuit in Figure 3, a 10 μH LDM component is recommended to reduce the interference.

REVISION HISTORY

| rev. | description | date |
|------|--|------------|
| 1.0 | initial release | 05/19/2017 |
| 1.01 | logo & packaging updates | 02/21/2020 |
| 1.02 | features and safety line updated | 01/14/2021 |
| 1.03 | derating curve, efficiency curves and circuit figures updated | 09/14/2021 |
| 1.04 | negative output application circuit updated | 04/26/2022 |
| 1.05 | application circuits updated | 04/04/2023 |
| 1.06 | switching frequency, no load input current, ripple & noise, and emissions updated for 5 Vdc output model | 05/23/2023 |

The revision history provided is for informational purposes only and is believed to be accurate.



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