

IPD25CN10NG-VB Datasheet N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A) ^a	Q _g (Typ.)		
100	0.0185 at V _{GS} = 10 V	45	38 nC		

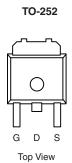
FEATURES

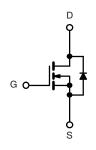
- TrenchFET® Power MOSFET
- 100 % $\rm R_{\rm g}$ and UIS Tested





- · Primary Side Switch
- Isolated DC/DC Converter





N-Channel MOSFET

Parameter		Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	100	V		
Gate-Source Voltage		V_{GS}			± 20
	T _C = 25 °C		45 ^a		
Continuous Proin Current (T. – 150 °C)	T _C = 100 °C		30	1	
Continuous Drain Current (T _J = 150 °C)	T _A = 25 °C	I _D	9.2 ^b		
	T _A = 100 °C		6.8 ^b	_	
Pulsed Drain Current		I _{DM}	140	A	
Continuous Source-Drain Diode Current	T _C = 25 °C		45 ^a		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2 ^b		
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	35		
Avalanche Energy	L=0.1 IIII	E _{AS}	101	mJ	
Maximum Power Dissipation	T _C = 25 °C		136.4		
	T _C = 100 °C	ь	68.2	l w	
	T _A = 25 °C	P _D	3p		
	T _A = 100 °C		1.5 ^b		
Operating Junction and Storage Temperature Ra	T _J , T _{stg}	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^b	Steady State	R _{thJA}	40	50	°C/W
Maximum Junction-to-Case	Sieauy State	R _{thJC}	0.85	1.1	C/VV

Notes:

- a. Package limited.
- b. Surface mounted on 1" x 1" FR4 board.



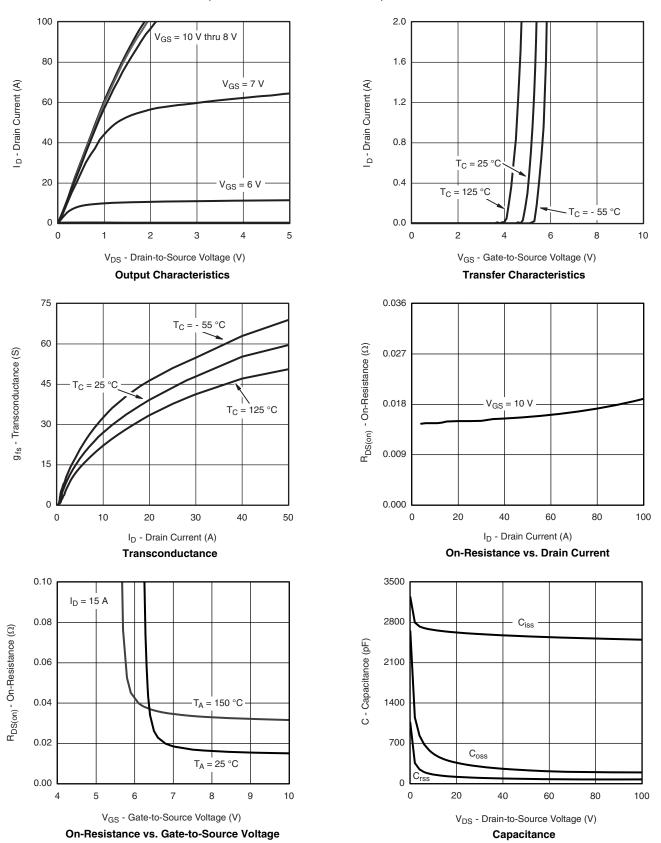
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L = 250 uA		110		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA		- 12.5			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$			5	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Oata Wallana D. J. O.	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μА	
Zero Gate Voltage Drain Current		V _{DS} = 100 V, V _{GS} = 0 V, T _J = 125 °C			50		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 15 A		0.0185		Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 15 A		33		S	
Dynamic ^b						•	
Input Capacitance	C _{iss}			2400		pF	
Output Capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		230			
Reverse Transfer Capacitance	C _{rss}			80			
Total Gate Charge	Qg			38	70	nC	
Gate-Source Charge	Q _{gs}	$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A}$		14			
Gate-Drain Charge	Q _{gd}			12			
Gate Resistance	R _g	f = 1 MHz		1.6	2.5	Ω	
Turn-On Delay Time	t _{d(on)}			12	20		
Rise Time	t _r	$V_{DD} = 50 \text{ V, R}_{1} = 1 \Omega$		10	20		
Turn-Off Delay Time	t _{d(off)}	$I_D \cong 50 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		18	35	ns ns	
Fall Time	t _f			8	15		
Drain-Source Body Diode Characteris	stics			_			
Continuous Source-Drain Diode	I _S	T _C = 25 °C			35	_	
Pulse Diode Forward Current ^a	I _{SM}	Ţ.			100	_ A	
Body Diode Voltage	V _{SD}	I _S = 15 A		0.85	1.5	V	
Body Diode Reverse Recovery Time t _{rr}				80	120	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	1		160	240	nC	
Reverse Recovery Fall Time	t _a	$I_F = 50 \text{ A}, \text{ dI/dt} = 100 \text{ A/}\mu\text{s}, T_J = 25 ^{\circ}\text{C}$		57		ns	
Reverse Recovery Rise Time	t _b			23			

Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

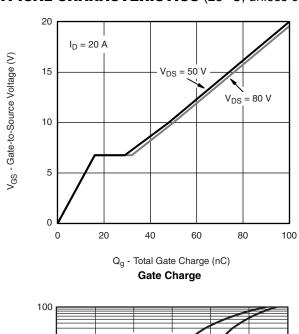
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

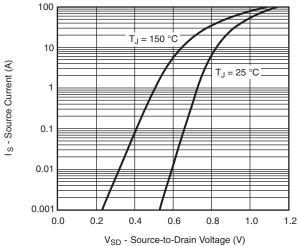


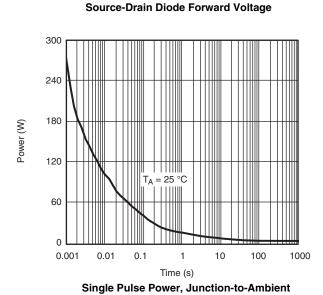


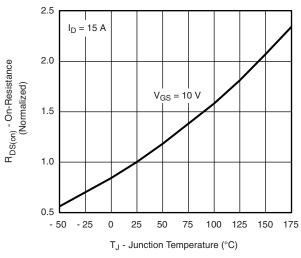
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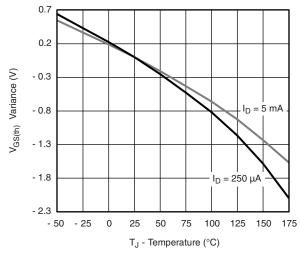




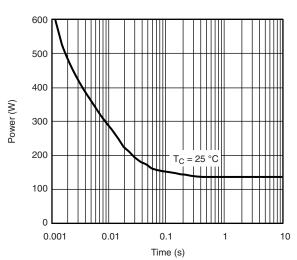






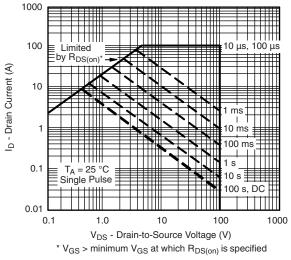




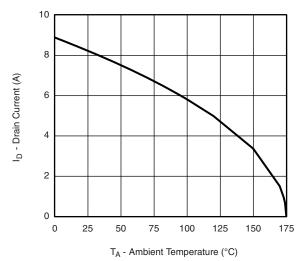


Single Pulse Power, Junction-to-Case

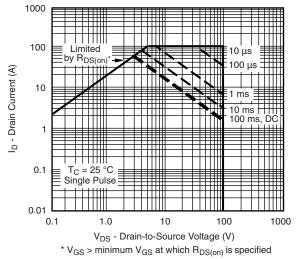


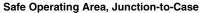


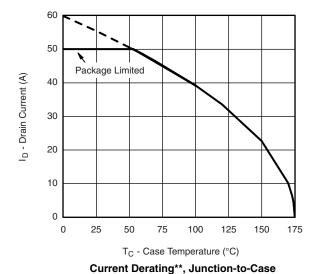




Current Derating**, Junction-to-Ambient

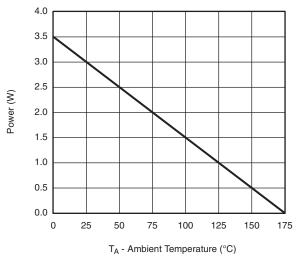


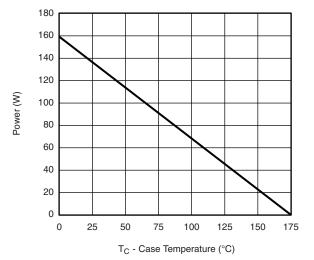




^{**} The power dissipation P_D is based on $T_{J(max.)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





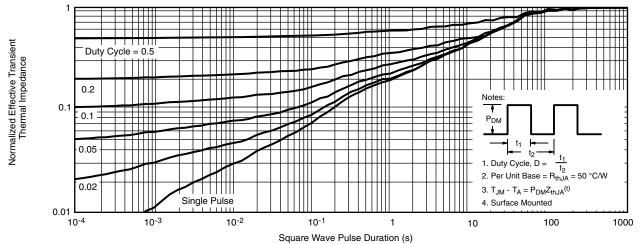


Power Derating**, Junction-to-Ambient

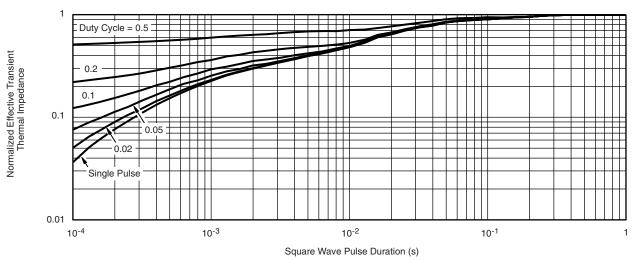
Power Derating**, Junction-to-Case

^{**} The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case



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