16V Input, 6A Step-down DC-DC Power SoC with Integrated Inductor

FEATURES

- Wide Input Voltage from 4.5V to 16V
- Adjustable Output Voltage from 0.6V to 13V
- Continuous Output Current
  - Output < 3.3V, 6A Continuous Output Current
  - Output ⩾ 3.3V, 5A Continuous, 6A Peak Output Current
- Two selectable switching frequencies: 600kHz and 1.2MHz
- Selectable light load mode
  - Power Saving Mode (PSM) for good light load efficiency
  - Forced Continuous Conduction Mode (FCCM) for better EMI performance
- Stable with low ESR Ceramic Capacitors
- Pre-Biased Start-Up
- Power Good (PG) Indicator
- Internal Soft-Start Time of 2.8ms
- Cycle-by-Cycle Current Limit Protection
- Hiccup Mode for Short Circuit and Over-Load Protection
- Thermal Shutdown Protection
- LGA-19 (3mm×3.1mm×1.7mm) Package
- Pb-Free RoHS Compliant

DESCRIPTION

The M1206 is a 6A step-down switching mode Power SoC (System on Chip) with integrated power MOSFETs, inductor and BST capacitor in an LGA-19 package. The input voltage ranges from 4.5V to 16V, and the frequency of Power SoC can be fixed at either 600kHz or 1.2MHz.

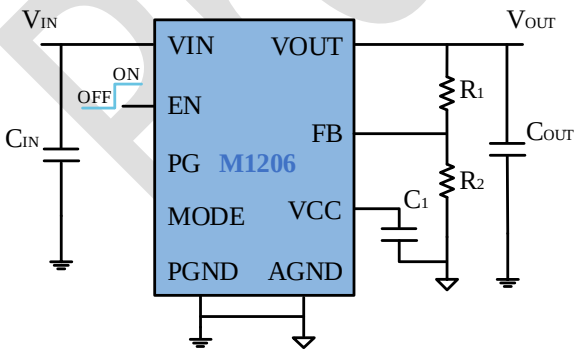
The M1206 provides high efficiency, fast transient response and good loop stability with Constant On Time (COT) control mode. It can select either Power Saving Mode (PSM) or Forced Continuous Conduction Mode (FCCM) for light load with excellent load regulation and line regulation.

The M1206 can indicate faults by PG and provides rich protection features including OCP, SCP and OTP.

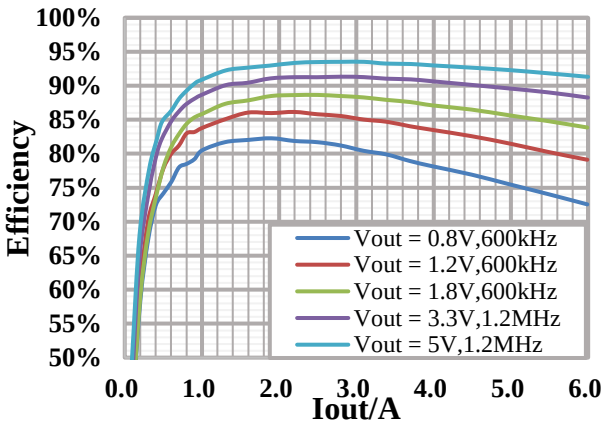
APPLICATIONS

- PoL Power Supply
- Data Centers
- Solid-State and Hard Disk Drives
- Industrial & Medical Systems

TYPICAL APPLICATION&EFFICIENCY



(Vin=12V，FCCM)



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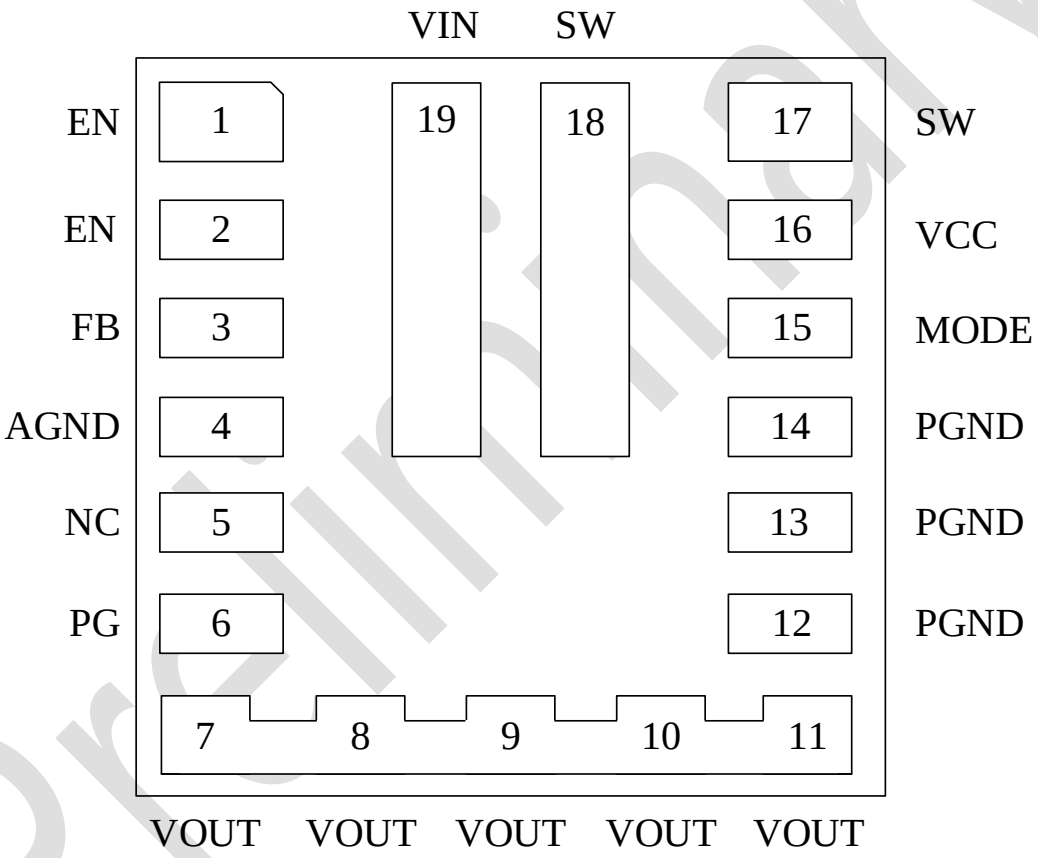
ORDERING INFORMATION

PART NUMBER	TOP MARKING	PACKAGE	MOQ	MSL
M1206DLFF	M1206 YWWLLL	LGA-19 (3mm×3.1mm×1.7mm)	3000/ Tape & Reel	3

NOTES: Y: Year, WW: Week, LLL: Lot Number.

PACKAGE REFERENCE

TOP VIEW



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PIN FUNCTIONS

PIN #	NAME	DESCRIPTION
1,2	EN	**Enable Control.** Pull this pin low to shut the chip down. Pull it high to enable the chip.
3	FB	**Feedback.** Connect this pin with an external resistor divider from the output to AGND to set the output voltage.
4	AGND	**Analog Ground.** This pin must be connected to PGND at a single point. See Layout Guideline for details.
5	NC	**Not Connected.**
6	PG	**Power Good.** The output of PG is an open drain, a pull-up resistor to power source is needed if used.
7,8,9,10,11	VOUT	**Output Voltage.** Connect these pins to the load. Output capacitors are recommended to be placed between VOUT and PGND.
12,13,14	PGND	**Power Ground.**
15	MODE	**Operation Mode Selection.** Place a resistor between MODE pin and GND to set the switching frequency and FCCM/PSM. The value of the resistor is showed at Table 2.
16	VCC	**LDO Output.** Place a 1uF output capacitor between VCC and GND.
17,18	SW	**Internal SW Pad.**
19	VIN	**Input Voltage.** Connect the input supply to this pin. Connect input capacitors between VIN and PGND. Place a 0.1uF decoupling input capacitor close to the SOC.

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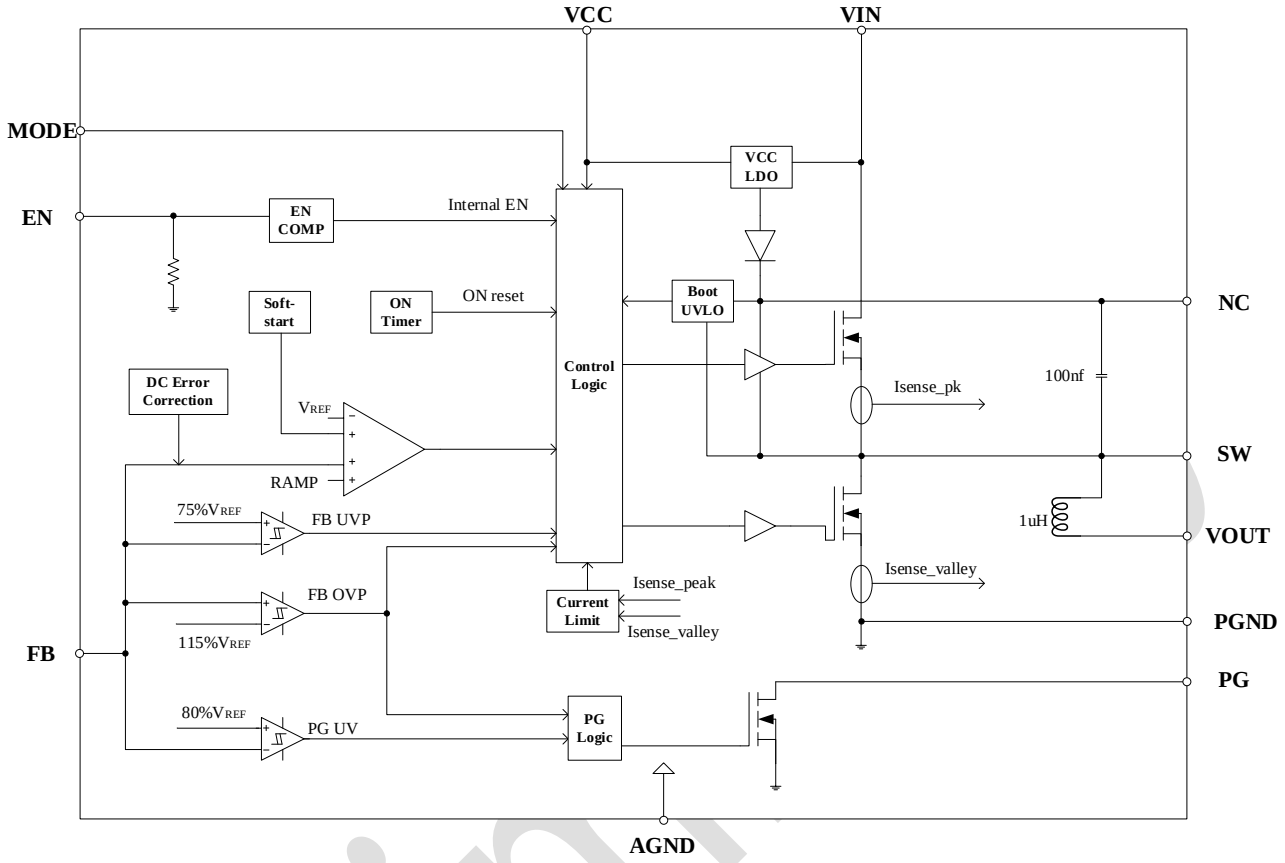
FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

	SYMBOL	MIN	MAX	UNIT
Voltage at Pins	V_{IN}	−0.3	20	V
Voltage at Pins	V_{SW}	−0.7	V_{IN}+0.7	V
Voltage at Pins	V_{SW}(<10ns)	-4	21	V
Voltage at Other Pins		−0.3	6	V
Junction Temperature Range	T_J	−40	125	℃
Storage Temperature Range	T_S	−55	150	℃
Peak Solder Reflow Body Temperature			245	℃

ESD Ratings

ESD	STANDARD	VALUE
Human Body Mode(HBM)	ANSI/ESDA/JEDEC JS-001-2017	2000V
Charge Device Mode(CDM)	ANSI/ESDA/JEDEC JS-002-2018	2000V

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	MAX	UNIT
Input Voltage Range	V_{IN}	4.5	16	V
Output Voltage Range	V_{OUT}	0.6	13	V
Output Current	I_{OUT}		6	A
Junction Temperature Range	T_J	−40	125	℃

THERMAL RESISTANCE

	SYMBOL	MIN	MAX	UNIT
Junction to Ambient	θ_{JA} Notes 2)		32	℃/W
Junction to Case	θ_{JC} Notes 2)		1	℃/W

NOTES:

1) The maximum allowable continuous power dissipation at particular ambient temperature (T_A) is calculated by $P_D(max)=(T_J(max)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature rise, thus the power module will go into thermal shutdown.
2) Measured on EVB, 4-layer 2oZ.

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V， T_A=25℃, unless otherwise noted.

PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		4.5		16	V
VIN under Voltage Lockout Threshold	VIN_{UVLO}	V_{IN} Increasing		4.1	4.3	V
VIN under Voltage Lockout Threshold	VIN_{UVLO}	V_{IN} Decreasing		3.6		V
VIN under Voltage Lockout Hysteresis				500		mV
VCC Regulator	VCC	VIN>5.2V, I_VCC=0uA		5		V
Shutdown Current	I_{SD}	V_{IN}=16V		1	3	μA
Quiescent Current (No Switching)	I_{Q1}	No Load, No switching, V_{FB}=0.63V，PSM		290	325	μA
EN On Threshold		V_{EN} Increasing	1.1	1.25	1.4	V
EN Off Threshold		V_{EN} Decreasing	0.9	1.05	1.2	V
Enable Threshold Hysteresis				0.2		V
Feedback Voltage	V_{FB_REF}		591	600	609	mV
Feedback leakage	I_{LK_FB}	V_{EN} = 1V, V_{FB} = 2V			0.1	μA
Valley Current Limit				6.7		A
Switching Frequency	F_{SW}	MODE = GND/Float		600		kHz
		MODE = 150kΩ/510kΩ		1200		kHz
Soft-Start time	T_{SS}		1.8	2.8	3.8	ms
PG High Threshold	V_{PGH_R}	Output UVP rising threshold	75	80	85	%
	V_{PGH_F}	Output OVP falling threshold		105		%
PG Low Threshold	V_{PGL_R}	Output OVP rising threshold	110	115	120	%
	V_{PGL_F}	Output UVP falling threshold		75		%
Thermal Shutdown				160		℃
Thermal Shutdown Hysteresis				20		℃

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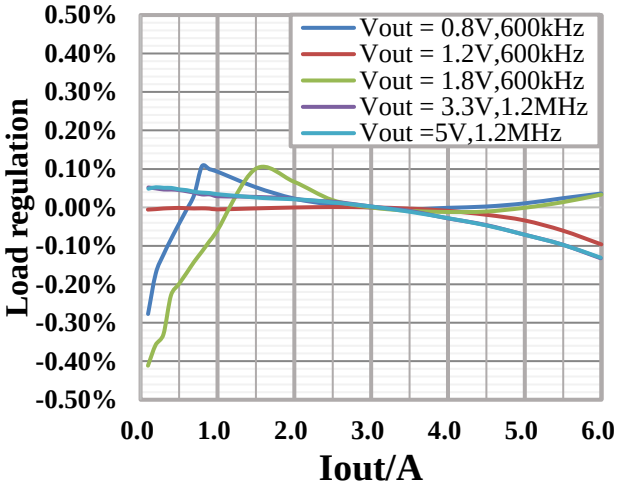
TYPICAL PERFORMANCE CHARACTERISTICS

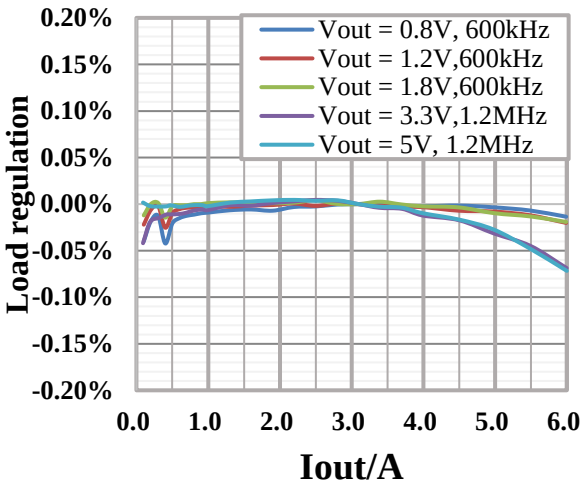
Load Regulation

V_{IN}=12V, V_{OUT}=0.8V/1.2V/1.8V/3.3V/5V,
I_{OUT}=0A~6A, PSM



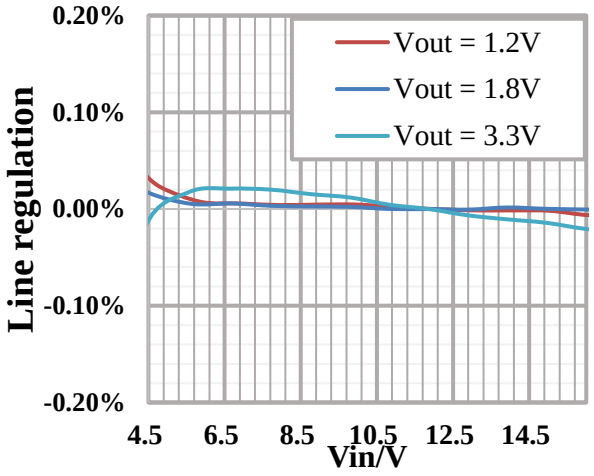
Load Regulation

V_{IN}=12V, V_{OUT}=0.8V/1.2V/1.8V/3.3V/5V,
I_{OUT}=0A~6A, FCCM



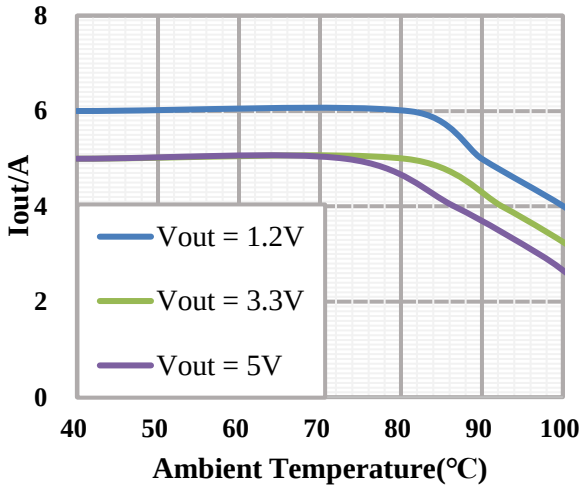
Line Regulation

When V_{OUT}=1.2V/1.8V, I_{OUT}=6A,
When V_{OUT}=3.3V, I_{OUT}=5A,
V_{IN}=4.5V~16V, Frequency = 600kHz



Thermal Derating

V_{IN} = 12V, V_{OUT}=1.2V/3.3V/5V
Frequency = 600kHz



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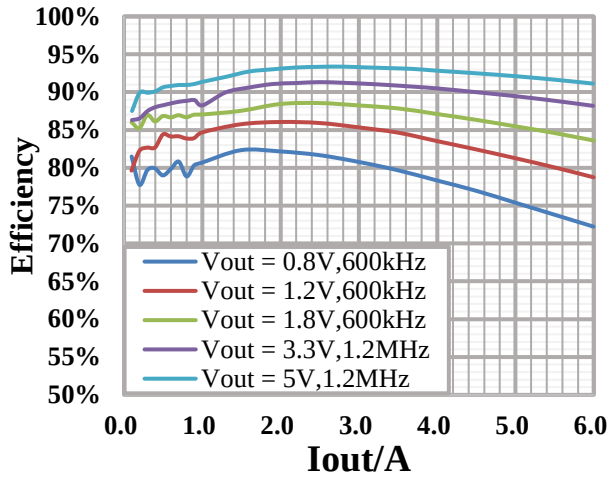
TYPICAL PERFORMANCE CHARACTERISTICS

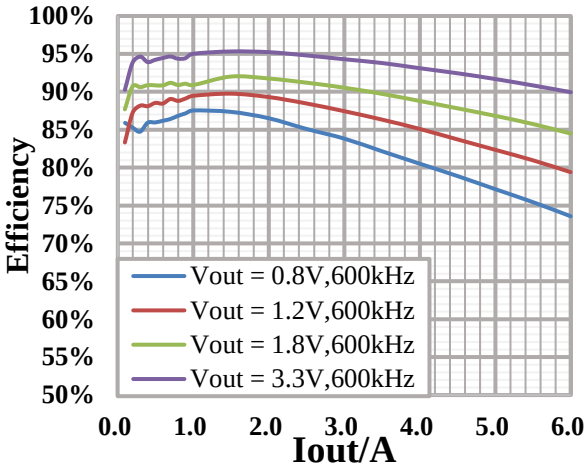
Efficiency

V_{IN}=12V, V_{OUT}=0.8V/1.2V/1.8V/3.3V/5V,
I_{OUT}=0A~6A, PSM



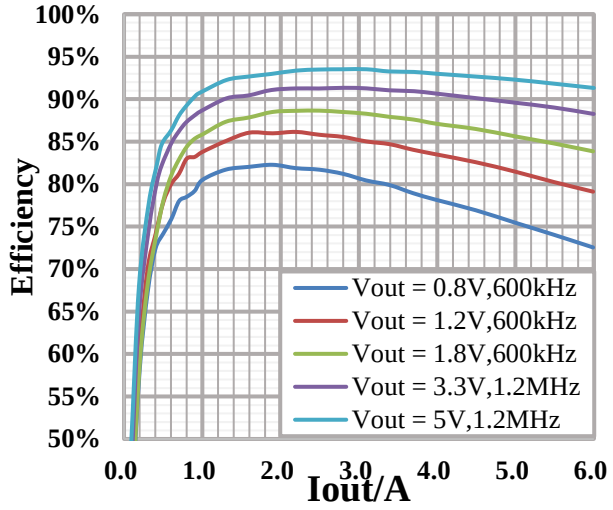
Efficiency

V_{IN}=5V, V_{OUT}=0.8V/1.2V/1.8V/3.3V,
I_{OUT}=0A~6A, PSM



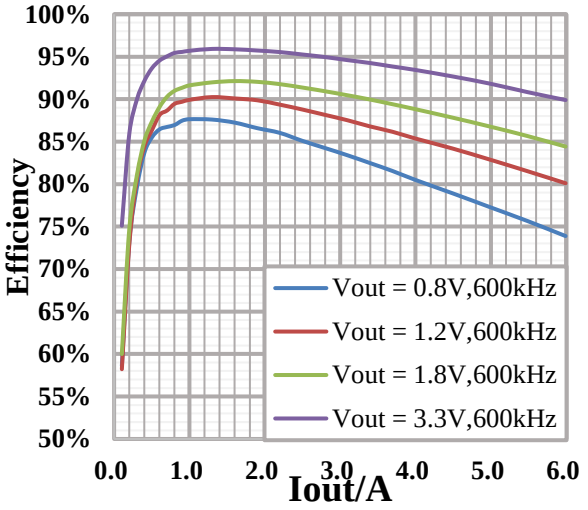
Efficiency

V_{IN}=12V, V_{OUT}=0.8V/1.2V/1.8V/3.3V/5V,
I_{OUT}=0A~6A, FCCM



Efficiency

V_{IN}=5V, V_{OUT}=0.8V/1.2V/1.8V/3.3V,
I_{OUT}=0A~6A, FCCM



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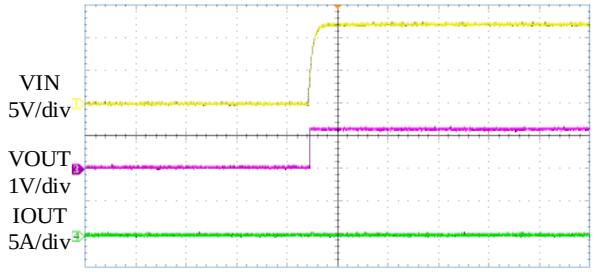
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=12V and V_{OUT}=1.2V, T_A=25℃, FCCM, 600kHz, unless otherwise noted.

VIN Start-up

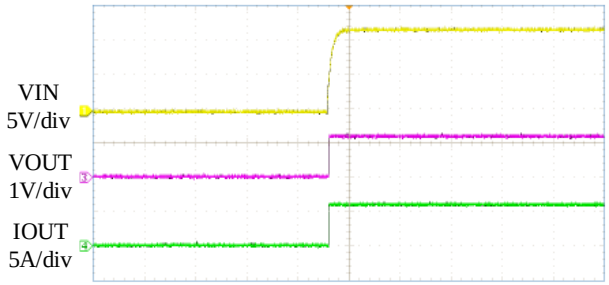
I_{OUT}=0A



400ms/div

VIN Start-up

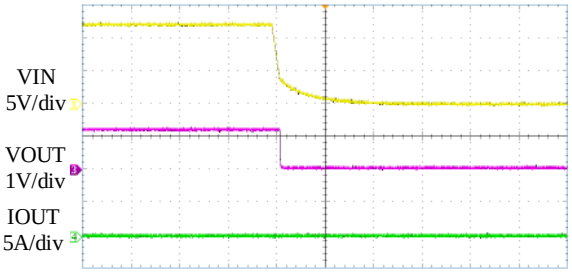
I_{OUT}=6A



400ms/div

VIN Shutdown

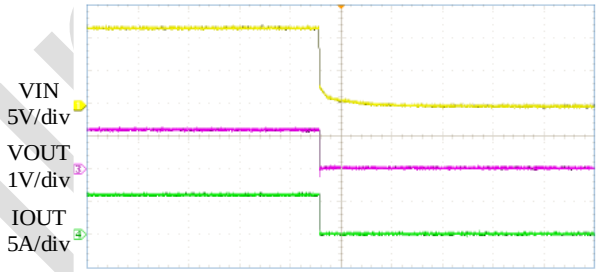
I_{OUT}=0A



400ms/div

VIN Shutdown

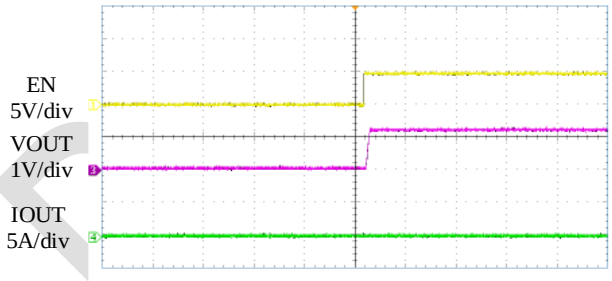
I_{OUT}=6A



400ms/div

EN Start-up

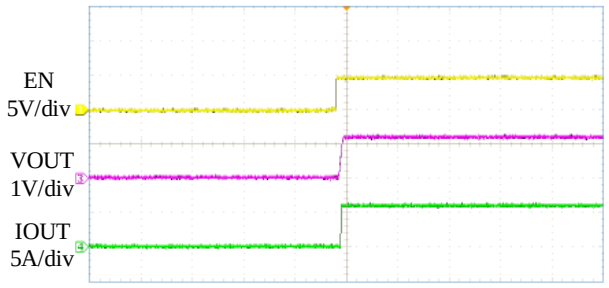
I_{OUT}=0A



40ms/div

EN Start-up

I_{OUT}=6A



40ms/div

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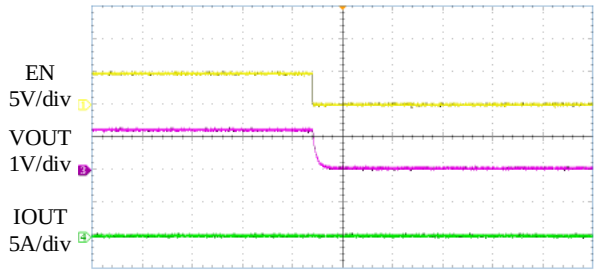
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=12V and V_{OUT}=1.2V, T_A=25℃, FCCM, 600kHz, unless otherwise noted.

EN Shutdown

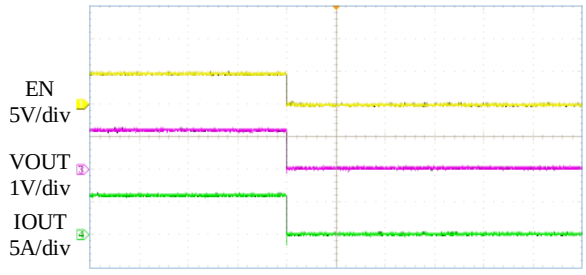
I_{OUT}=0A



40ms/div

EN Shutdown

I_{OUT}=6A



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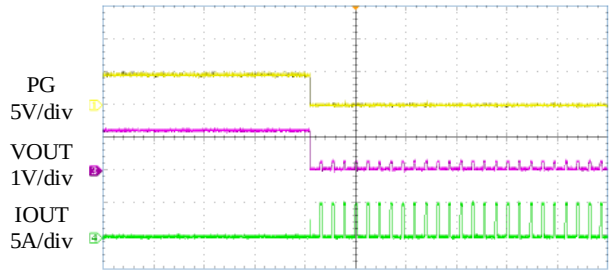
SCP Entry

I_{OUT}=0A



100ms/div

SCP Entry

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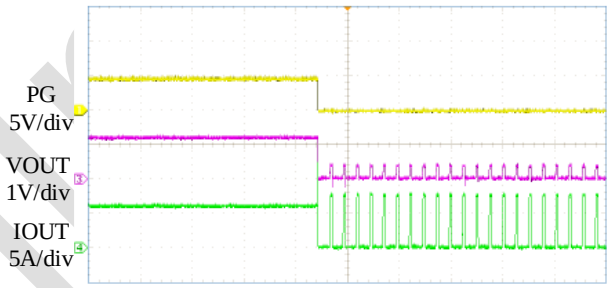
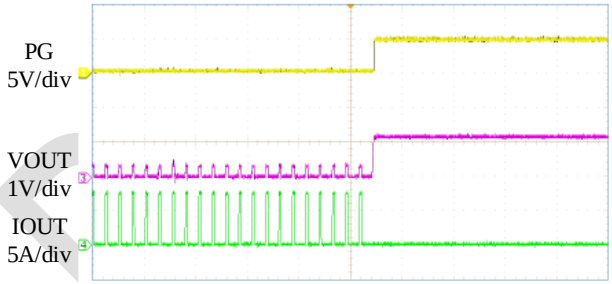


100ms/div

SCP Recovery

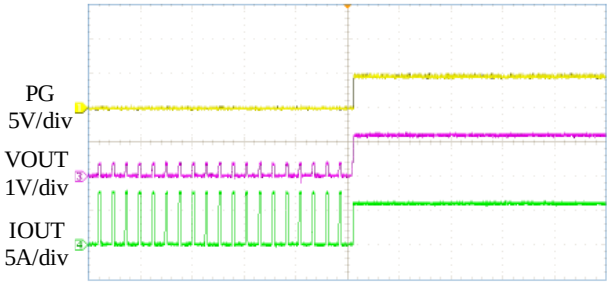
I_{OUT}=0A



100ms/div

SCP Recovery

I_{OUT}=6A



100ms/div

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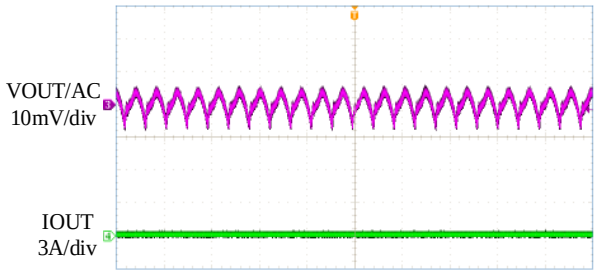
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN}=12V and V_{OUT}=1.2V, T_A=25℃, C_{out} = 3×22uF, FCCM, 600kHz, unless otherwise noted.

VOUT Ripple

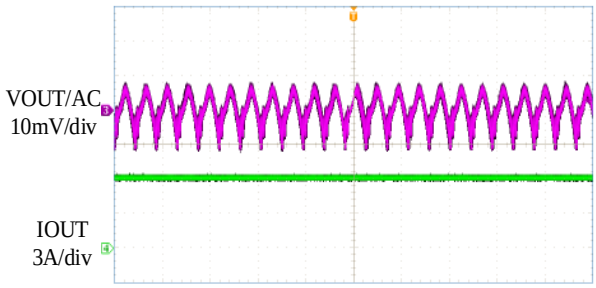
I_{OUT}=0A



4us/div

VOUT Ripple

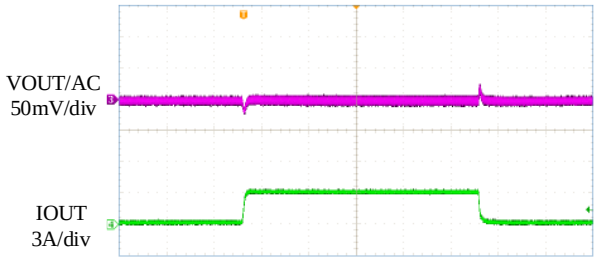
I_{OUT}=6A



4us/div

Load Transient

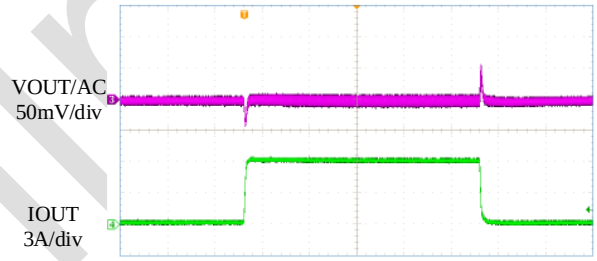
I_{OUT}=0A to 3A, 2.5A/μs



200μs/div

Load Transient

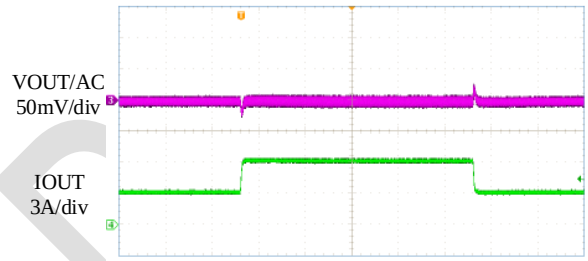
I_{OUT}=0A to 6A, 2.5A/μs



200μs/div

Load Transient

I_{OUT}=3A to 6A, 2.5A/μs



200μs/div

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OPERATION

The M1206 is a 6A synchronous step-down switching mode Power SoC with integrated High-Side and Low-Side power MOSFETs, inductor and BST capacitor in an LGA-19 package. VCC capacitor, FB resistor divider, input and output capacitors are needed to complete the design over 4.5V to 16V input voltage range. The M1206 supports output voltage of 0.6V to 13V and the frequency of Power SoC can be fixed at either 600kHz or 1.2MHz.

M1206 works on COT control mode that offers excellent transient response over the wide input range. It can select Power Saving Mode (PSM) or Forced Continuous Conduction Mode (FCCM) for light load with excellent load regulation and line regulation. And M1206 has an internal 2.8ms soft-start timer.

M1206 provides fully integrated protection features including OCP, SCP and OTP and all these faults can be indicated by PG. The details about these protection functions are presented below.

OVER CURRENT PROTECTION (OCP)

M1206 has both valley current limiting (typical 6.7A) and peak current limiting (typical 8A). The Low-Side and High-side MOSFET sense their current when ON. If high-side MOSFET current exceeds the peak current limit, it is turned off and the low-side MOSFET is turned on. The high-side MOSFET turns on again after output voltage decreases below the reference voltage.

If low-side MOSFET current exceeds the valley current limit when output voltage decreases below the reference voltage, the low-side MOSFET continues to turn on until the start of the next cycle.

If there is overload for a period of time, the peak and valley current protection maintain and the FB voltage decrease below UVP Threshold, then M1206 enters hiccup mode to stop switching for a pre-determined period of time and automatically soft-start up again. Soft-start limits inrush current and avoids output voltage overshoot.

VIN Under-Voltage Lockout (VIN UVLO)

VIN UVLO protects the M1206 from operating at insufficient VIN voltage. When VIN rises above rising threshold (typical 4.1V), M1206 soft-starts. When M1206 is operating then VIN falls below falling threshold (typical 3.6V), the SOC shutdowns.

Output Over-Voltage Protection (OVP) & Under-Voltage Protection (UVP)

M1206 monitors V_{FB}. When V_{FB} rises and becomes higher than 115% of target voltage, OVP is indicated by PG, meanwhile Low-Side MOSFET turns on until its current decreases below the negative current limit, then Low-Side MOSFET turns off and remains for 5us to turn on again.

When V_{FB} drops below 75% of target voltage, UVP is indicated by PG and the SOC enters hiccup protection.

OVER TEMPERATURE PROTECTION (OTP)

M1206 will stop switching when the junction temperature exceeds 160 ℃. The device will power up again when the junction temperature drops below 140℃.

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USER GUIDE

Output Voltage

The output voltage is set by an external feedback resistor divider according to the typical application circuit on Page 1. The top feedback resistor R_1 can impact the loop stability. R_1 is recommended to be between 2kΩ and 20kΩ. For any chosen R_1, the bottom feedback resistor R_2 can be calculated as:

$$R_2=R_1\frac{V_{FB}}{V_{OUT}-V_{FB}}$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1：FB Resistor Values for Common Output Voltages.

V_{OUT}(V)	R_1(kΩ)	R_2(kΩ)	C_{FF} (pF)
3.3	5.1	1.1	82
2.5	5.1	1.6	82
1.8	5.1	2.49	82
1.5	5.1	3.3	82
1.2	5.1	5.1	82
1.0	5.1	7.5	82
0.8	5.1	15	82

And a feedforward capacitor C_{FF} is recommended for better load transient response.

Input Capacitor Selection

The input current of a step-down converter is discontinuous with a sharp slope, therefore an input filter capacitor is necessary. For better performance, low ESR ceramic capacitor with X5R or X7R dielectrics are highly preferred because of their lowest temperature variations. The RMS current of the input capacitor is calculated by:

$$I_{CIN\_RMS}=I_{OUT}\sqrt{D(1-D)}$$

where D is the Duty Cycle, when the current is continuous, $D=V_{OUT}/V_{IN}$; I_{OUT} is the output load current. Accordingly, when D is 0.5, the highest RMS current is approximately:

$$I_{CIN\_RMS}=\frac{1}{2}\times I_{OUT}$$

Thereby, it is recommended to choose the capacitor with the RMS current rating higher than 1/2 I_{OUT}.

The power dissipation of the input capacitor can be estimated with the RMS current and the ESR.

Electrolytic or tantalum capacitors can also be used. A small size ceramic capacitor between 10nF and 0.1μF is recommended to be placed close to VIN and PGND. The input voltage ripple caused by the capacitors can be calculated as:

$$\Delta V_{CIN}=\frac{I_{OUT}}{F_{SW}\cdot C_{IN}}\cdot\frac{V_{OUT}}{V_{IN}}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

in which, F_{SW} is switching frequency.

Output Capacitor Selection

Output capacitors are required to keep stable output voltage. To minimize the output voltage ripple, low ESR ceramic capacitors should be used. The output voltage ripple can be estimated as:

$$\Delta V_{OUT}=\frac{V_{OUT}}{8F_{SW}^2C_{OUT}L}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

With the internal fixed inductor L of 1μH.

If electrolytic or tantalum capacitors are used, the output voltage ripple will be dominated by their ESR,

$$\Delta V_{OUT}=R_{ESR}\cdot\frac{V_{OUT}}{F_{SW}L}\cdot\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Enable Control

When input voltage is above the under-voltage-lock-out threshold, M1206 can be enabled by pulling up the EN pin above 1.25V and will be disabled if the EN pin is below 1.05V, but under 5V. There are two ways to drive M1206:

- EN can be driven by external logical signal to enable/disable M1206.
- For tying EN to VIN application, such as the typical application circuit on figure 3, the EN voltage is divided by the external resistors R_{PULL_UP} and R_{PULL_DOWN} from VIN. The V_{EN} is calculated:

$$V_{EN}=\frac{R_{PULL\_DOWN}}{R_{PULL\_UP}+R_{PULL\_DOWN}}\cdot VIN$$

For example, if VIN=12V, the R_{PULL_UP} is 300 kΩ, the R_{PULL_DOWN} is 100 kΩ, so the V_{EN} is 3V.

Mode Selection

M1206 can work on FCCM or PSM under light load

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condition by selecting different resistors connected with Mode pin. The switching frequency is also programmed by this pin. Table 2 shows the values of the resistors for different operating modes and switching frequency.

Table 2: Light Load Mode selection

Mode	Mode PIN Resistor
PSM, F_{SW} = 600kHz	0Ω to GND
PSM, F_{SW} = 1.2MHz	150kΩ to GND
FCCM, F_{SW} = 600kHz	Float
FCCM, F_{SW} = 1.2MHz	510kΩ to GND

Power Good Indicator

M1206 has an open drain PG indicator. PG will be pulled up if output voltage is within 80%~105% of regulation, otherwise PG is pulled down by internal NMOS. A 100kΩ pullup resistor is required to a suitable pullup voltage, which is lower than 5V.

Pre-Biased Start-Up

The M1206 is designed for start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the internal BST voltage is refreshed and charged, and the voltage on the soft-start is charged as well. If the internal BST voltage exceeds its rising voltage threshold and the soft-start voltage exceeding the sensed voltage at FB, the part begins working normally.

PCB Layout Guide

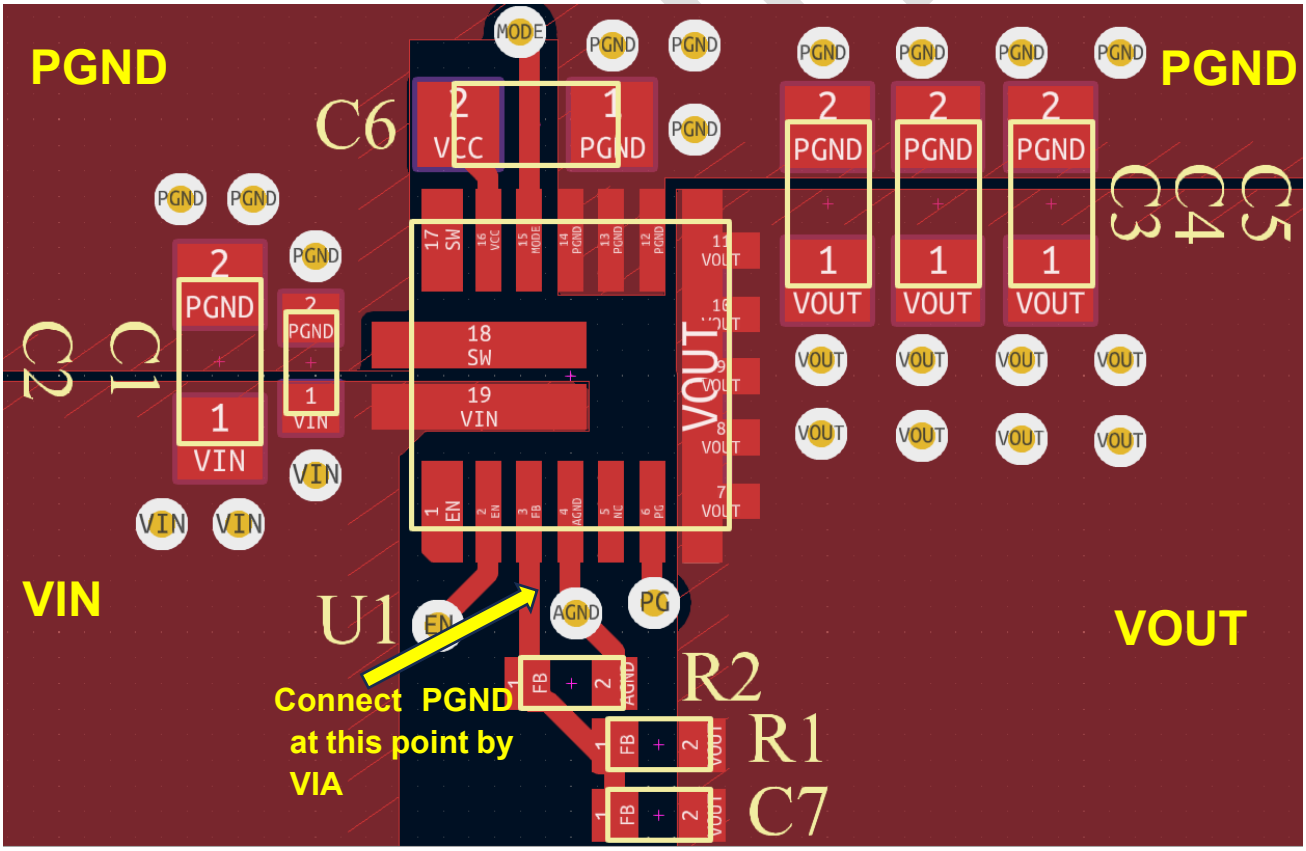

Figure 1. Recommended Layout

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Figure 2：Suitable way of connecting AGND and PGND (at Inner Layer)

For better electrical and thermal performance, some PCB layout guidelines should be considered as below

1. Use wide and short traces for the high-current paths (GND, VIN and VOUT). It minimizes the PCB conduction loss and thermal stress.
2. Place the input decoupling capacitor close to VIN and PGND.
3. Place a 1uF VCC capacitor as close to SOC as possible.
4. Keep the feedback network close to FB but away from the SW. Connect the bottom resistor to FB and AGND.
5. The PGND and AGND must be connected at a point, and the trace from AGND to PGND should be wide and short for better noise protection. Avoid to let the trace pass through the underside of SOC.

Figure 1 gives a recommended example of layout. Figure 2 shows details of how AGND is suitably connected to PGND.

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TYPICAL APPLICATION

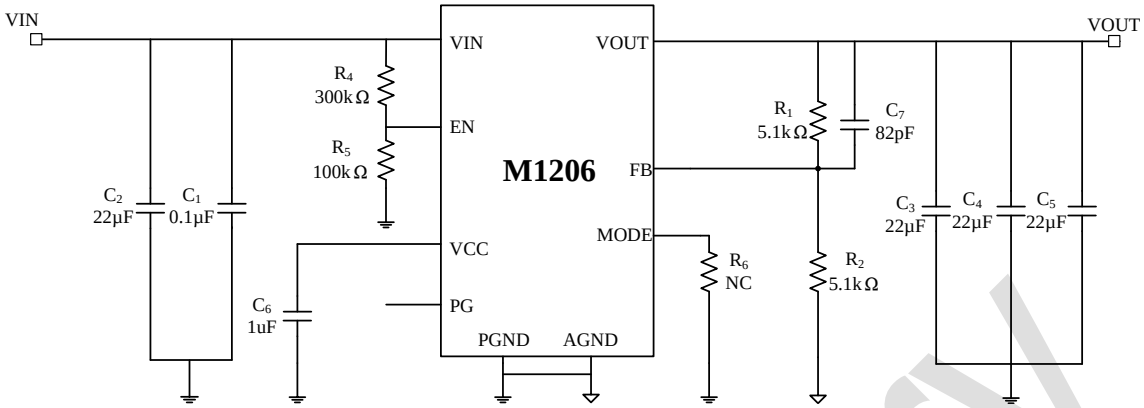

Figure 3. Typical Application Circuits of M1206 for 1.2V Output

Table 3：M1206 Reference Design for 12V Input

VOUT	CIN	COUT	VOUT RIPPLE	R_1	R_2	C_{ff}	R_6	operating mode
5V	2×22uF	3×22uF	24.6mV(5A)	5.1 kΩ	0.68 kΩ	82 pF	150 kΩ	PSM 1.2MHz
		2×22uF	35.2mV(5A)				510 kΩ	FCCM 1.2MHz
3.3V	1×22uF	3×22uF	14.2mV(5A)	5.1 kΩ	1.1 kΩ	82 pF	150 kΩ	PSM 1.2MHz
		2×22uF	22.1mV(5A)				510 kΩ	FCCM 1.2MHz
1.8V	1×22uF	3×22uF	21.6mV(6A)	5.1 kΩ	2.49 kΩ	82 pF	0	PSM 600kHz
		2×22uF	32.4mV(6A)				NC	FCCM 600kHz
1.2V	1×22uF	3×22uF	17.6mV(6A)	5.1 kΩ	5.1 kΩ	82 pF	0	PSM 600kHz
		2×22uF	24.2mV(6A)				NC	FCCM 600kHz

NOTES:

CIN is the sum of the input capacitors, COUT is the sum of the output capacitors, please refer to Figure 3 for parameters of other components.

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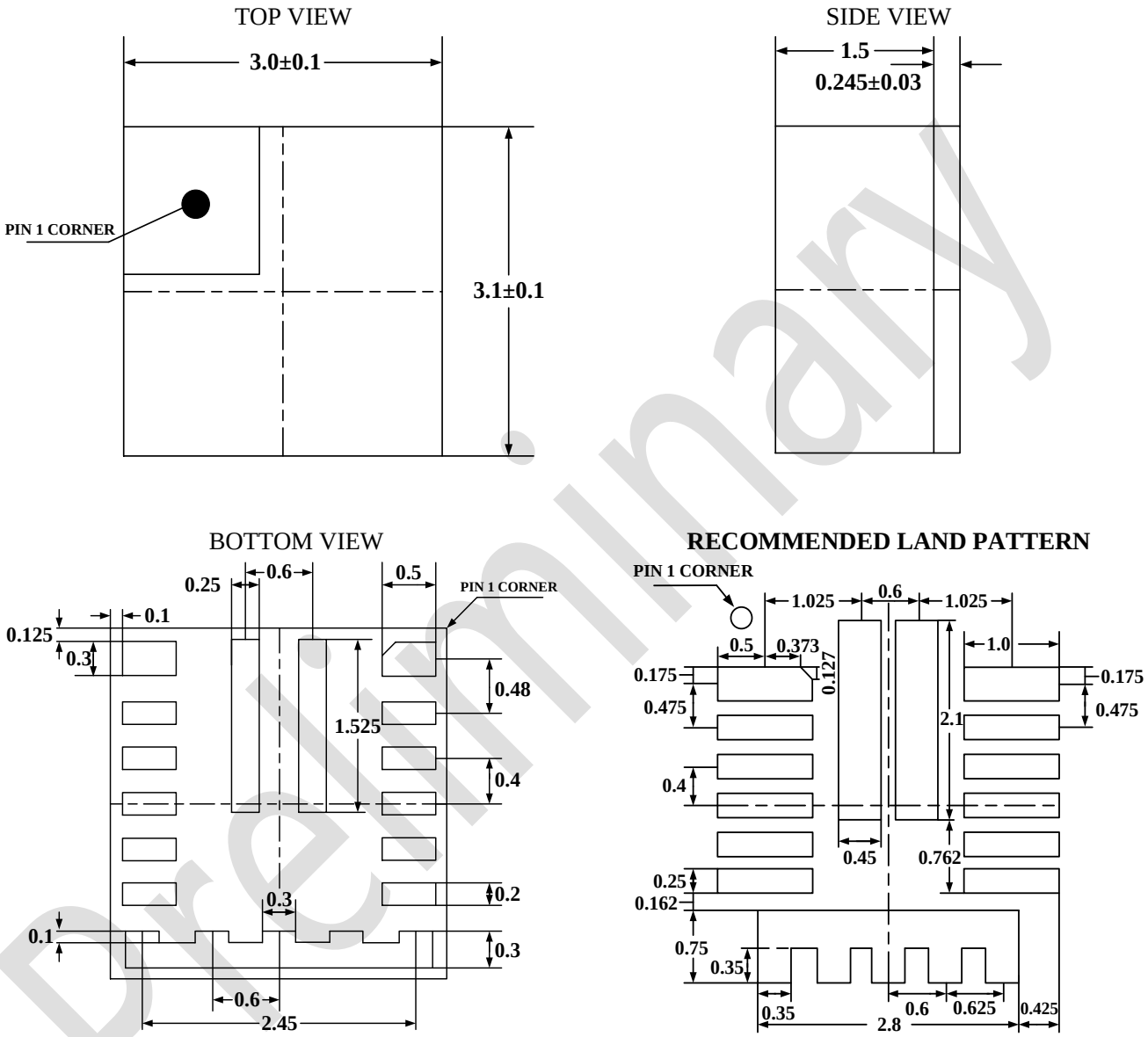
PACKAGE INFORMATION

LGA-19 (3mm×3.1mm×1.7mm) Package



NOTES:

All dimensions are in MM.

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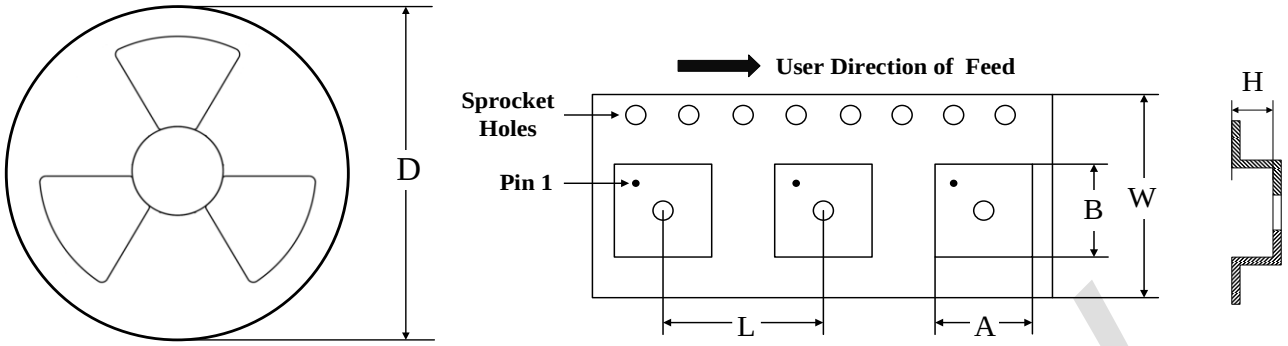
CARRIER INFORMATION



PART NUMBER	PACKAGE	QUANTITY /REEL	D	A	B	L	W	H
M1206DLFF	LGA-19 (3mm×3.1mm×1.7mm)	3000	13 in	3.25mm	3.25mm	8mm	12mm	2.06mm

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