

### FEATURES

- 输入电压: 45 V<sub>AC</sub> to 220 V<sub>AC</sub> ( 50Hz-60Hz )
- 静态工作电流: 200μA ( 典型 )
- 电磁干扰 ( EMC ) 防护能力:
  - ≥10V/m (无外部滤波)
  - ≥18V/m (有外部滤波)
- 适用于检测 A 型和 AC 型漏电信号
- 漏电延迟: 外部可调(滤波后再延迟);
- 0.5 毫秒雷击与浪涌脉冲检测
- 漏电脉冲连续性检测
- 高输入灵敏度: V<sub>r</sub> = 4.95mV ( 典型 )
- 各种类型的漏电信号的跳闸一致性好
- OS 输出为 3 个 30mS:100mS 脉冲驱动信号
- 符合国标 GB16916, GB16917 和 GB14048 标准
- 宽的温度范围 ( Ta = -40 ~ +125℃ )
- 8-lead SOP

### APPLICATIONS

- 塑壳式断路器
- 高速漏电保护装置
- 防漏电插座
- 带有漏电保护的小家电

### GENERAL DESCRIPTION

SS54123B 是一款具有低功耗和极佳高频漏电流抑制特性的高可靠 A 型和 AC 型漏电保护器专用芯片, 用于检测火线和零线上的漏电信号。当有漏电信号产生时, 零电流互感器(ZCT)检测到电信号, 漏电信号可以是直流、AC 型和 A 型(包括 0°、90° 和 135° 漏电信号), 漏电信号经过差动放大器放大, 并经过精密整流后, 获得完整的正、负半波的波形。当漏电流的 RMS 值大于规定的额定电流(RMS)阈值时, 芯片输出引脚快速输出高电平信号驱动外部可控硅, 使电网与用户端断开连接, 从而实现漏电保护; 当断路器不能正常跳闸时, 内部数字处理器将输出占空比为 30mS:100mS 的脉冲控制信号, 从而保证断路器彻底关断, 有效地保护触电危险。

本芯片可稳定通过 GB14048 中 10V/m 电磁干扰、5KHz/100KHz EFT 群脉冲、雷击浪涌、周波跌落、工频磁场等等可靠性实验。

### TYPICAL APPLICATION CIRCUIT

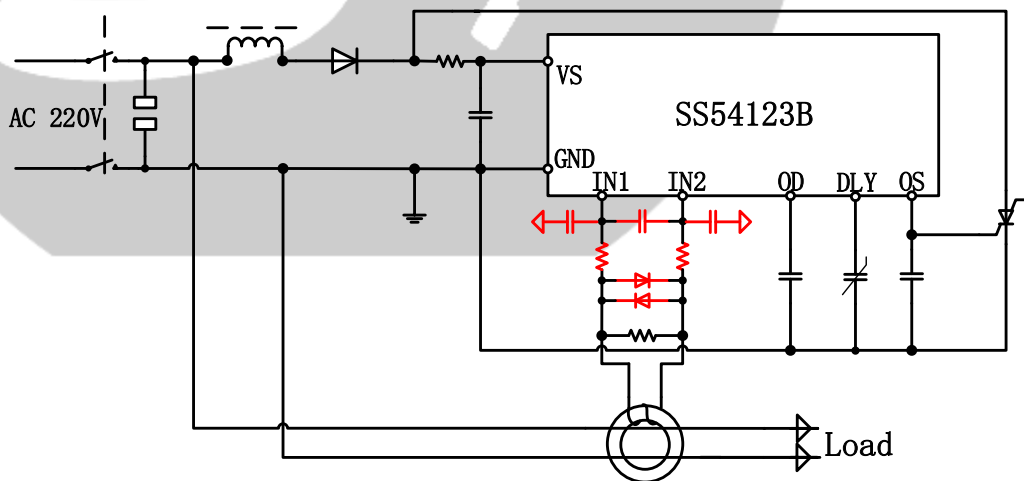


Figure 1. Typical Application Circuit

Rev. A

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## SPECIFICATIONS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
电源端稳压电压 1	$V_{S1}$	钳位二极管电压@钳位电流 $I_S=1\text{mA}$ ; 常温		12		V
电源端稳压电压 2	$V_{S2}$	钳位二极管电压@钳位电流 $I_S=1\text{mA}$ ; 全温区	11		13	V
供电电流(功耗 1)	$I_{S1}$	$V_S=8\text{V}; I_{N1}-I_{N2}=0\text{mV}$ ; 常温	168		252	$\mu\text{A}$
供电电流(功耗 2)	$I_{S2}$	$V_S=8\text{V}; I_{N1}-I_{N2}=0\text{mV}$ ; 全温区	150		295	$\mu\text{A}$
OS 输出驱动电压	$V_{OS\_LV}$	$V_S=12\text{V}; I_{N1}-I_{N2}=20\text{mV}$		5	5.5	V
OS 输出驱动电流 1	$I_{OS\_LV1}$	$OS=0.8\text{V}; I_{N1}-I_{N2}=20\text{mV}$ ; 常温	250		850	$\mu\text{A}$
OS 输出驱动电流 2	$I_{OS\_LV2}$	$OS=0.8\text{V}; I_{N1}-I_{N2}=20\text{mV}$ ; 全温区	130		1550	$\mu\text{A}$
漏电动作电压	$V_T$	$ I_{N1}-I_{N2} ; C_{OD}=150\text{nF}$	4.75	4.95	5.25	mV
漏电比较电压	$V_{REFSC}$		1.25	1.5	1.75	V
延迟注入电流	$I_{DLY}$	$V_{OA}=1.6\text{V}; I_{N1}-I_{N2}=20\text{mV}$	2.7	3	3.3	$\mu\text{A}$
延迟比较电压	$V_{REFCDLY}$			1.5		V
漏电信号锁存时间	$T_{ON}$	$I_{N1}-I_{N2}=20\text{mV}$	28			ms
OS 驱动脉冲个数		$V_S=8\text{V}; I_{N1}-I_{N2}=20\text{mV}$			3	

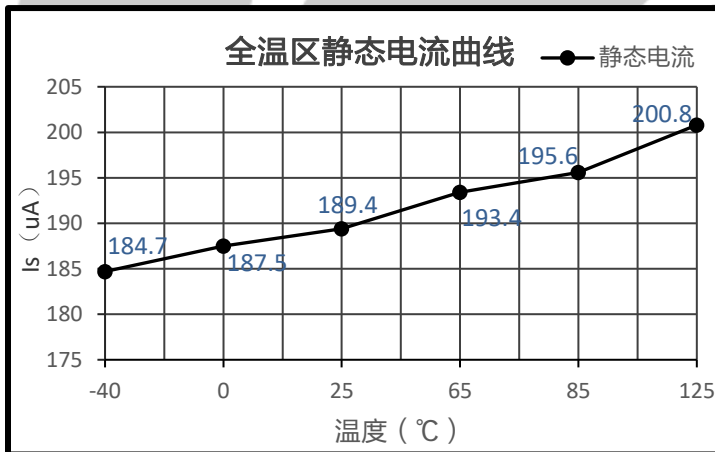


Figure 2.  $I_S$  Curve In- $40^\circ\text{C} \sim 125^\circ\text{C}$

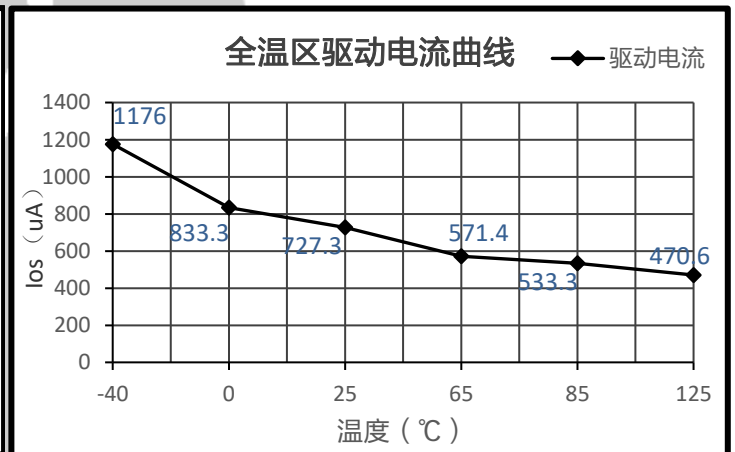


Figure 3.  $I_{OS}$  Curve In- $40^\circ\text{C} \sim 125^\circ\text{C}$

## ABSOLUTE MAXIMUM RATING

table 2.

Parameter	Rating
I <sub>SMAX</sub>	8mA
V <sub>s</sub> to GND	-0.3V to +24V
O <sub>S</sub> to GND	-0.3V to +6V
Input Voltage to GND	-0.3V to +6V
Output Voltage to GND	-0.3V to +6V
Storage Temperature Range	- 65°C to +150°C
Operating Junction Temperature Range	- 40°C to +125°C
Operating Ambient Temperature Range	- 40°C to +85°C
Soldering Conditions	JEDEC J-STD-020

注意, 超出上述绝对最大额定值可能会导致器件永久性损坏。这只是额定应力值, 不涉及器件在这些或任何其他条件下超出本技术规格指标的功能性操作。长期在绝对最大额定值条件下工作会影响器件的可靠性。

### THERMAL DATA

绝对最大额定值仅适合单独应用, 但不适合组合使用。结温高于限制值时, 会损坏 SS54123B。监控环境温度并不能保证 T<sub>J</sub> 不会超出额定温度限值。在功耗高、热阻差的应用中, 可能必须降低最大环境温度。

在功耗适中、PCB 热阻较低的应用中, 只要结温处于额定限值以内, 最大环境温度可以超过最大限值。器件的结温 (T<sub>J</sub>) 取决于环境温度 (T<sub>A</sub>)、器件的功耗 (P<sub>D</sub>) 和封装的结到环境热阻 (θ<sub>JA</sub>)。

最高结温 (T<sub>J</sub>) 由环境温度 (T<sub>A</sub>) 和功耗 (P<sub>D</sub>) 通过下式计算:

$$T_J = T_A + (P_D \times \theta_{JA})$$

封装的结到环境热阻 (θ<sub>JA</sub>) 基于使用 4 层板的建模和计算方

法, 主要取决于应用和板布局。在功耗较高的应用中, 需要特别注意热板设计。θ<sub>JA</sub> 的值可能随 PCB 材料、布局和环境条件不同而异。θ<sub>JA</sub> 的额定值基于 4" × 3" 的 4 层电路板。有关板结构的详细信息, 请参考 JESD 51-7 和 JESD 51-9。

Ψ<sub>JB</sub> 是结到板热特性参数, 单位为 °C/W。封装的 Ψ<sub>JB</sub> 基于使用 4 层板的建模和计算方法。JESD51-12 “报告和使用电子封装热信息指南” 中声明, 热特性参数和热阻不是一回事。Ψ<sub>JB</sub> 衡量沿多条热路径流动的器件功率, 而 θ<sub>JB</sub> 只涉及一条路径。因此, Ψ<sub>JB</sub> 热路径包括来自封装顶部的对流和封装的辐射, 这些因素使得 Ψ<sub>JB</sub> 在现实应用中更有用。最高结温 (T<sub>J</sub>) 由板温度 (T<sub>B</sub>) 和功耗 (P<sub>D</sub>) 通过下式计算:

$$T_J = T_B + (P_D \times \Psi_{JB})$$

有关 Ψ<sub>JB</sub> 的详细信息, 请参考 JESD51-8 和 JESD51-12。

### THERMAL RESISTANCE

θ<sub>JA</sub> 和 Ψ<sub>JB</sub> 针对最差条件, 即器件焊接在电路板上以实现表贴封装。

Table 3. Thermal Resistance

Package Type	θ <sub>JA</sub>	θ <sub>JC</sub>	Unit
8-Lead SOP	96	55	°C/W

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

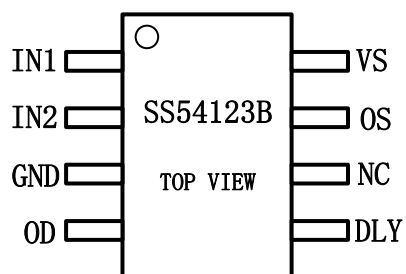


Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	IN1	运放同相输入管脚
2	IN2	运放反相输入管脚
3	GND	芯片地
4	OD	滤波、触发延时可调输出管脚
5	DLY	延迟管脚，外接延迟电容
6	NC	悬空
7	OS	可控硅触发输出管脚
8	VS	电源管脚

## THEORY OF OPERATION

SS54123B 是一款高性能、高可靠 A 型和 AC 型漏电保护器专用芯片，用于检测火线和零线上的漏电信号。采用小于 12V 电源供电，最小 SCR 驱动电流 250μA。在无驱动时静态电流典型值低至 160μA，因此 SS54123B 可使用小功率分流电阻，降低了系统成本。

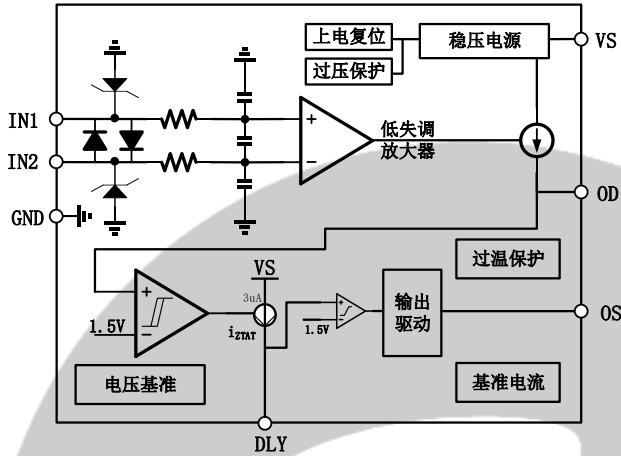


Figure 5. SS54123B Block Diagram

SS54123B 内部包含稳压电路、基准电路、差分放大电路、精密整流器、比较电路、延迟控制电路，过压保护，过温保护、振荡器、上电复位和可控硅驱动器等。通过连接外部零序电流互感器(ZCT)和高压微功率可控硅进行工作。

当有漏电信号产生时，零电流互感器(ZCT)检测到电信号，漏电信号经过差动放大器放大，并经过精密整流后，获得完整的正负半波的波形。当漏电流的 RMS 值大于规定的额定电流(RMS)阈值时，芯片输出引脚快速输出高电平信号驱动外部可控硅，使电网与用户端断开连接，从而实现漏电保护；当断路器不能正常跳闸时，内部数字处理器将输出占空比为 30mS:100mS 的脉冲控制信号，从而保证断路器彻底关断，有效地避免触电危险。

### DLY 工作原理

DLY 是输出延时控制端口。通过连接外部的电容，并调节电容大小，可以产生不同的输出控制信号延迟。

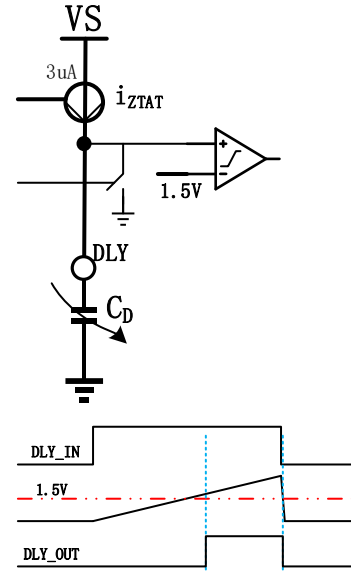


Figure 6. RC Time set circuit diagram

$$T_D = \frac{C_D \times V_{REF}}{I_D}$$

当  $V_{REF} = 1.5V$ ， $C_D = 3.42\mu F(1\mu F + 2.2\mu F + 0.22\mu F)$ ， $I_D = 3\mu A$  时，

$T_D \approx 1.71s$

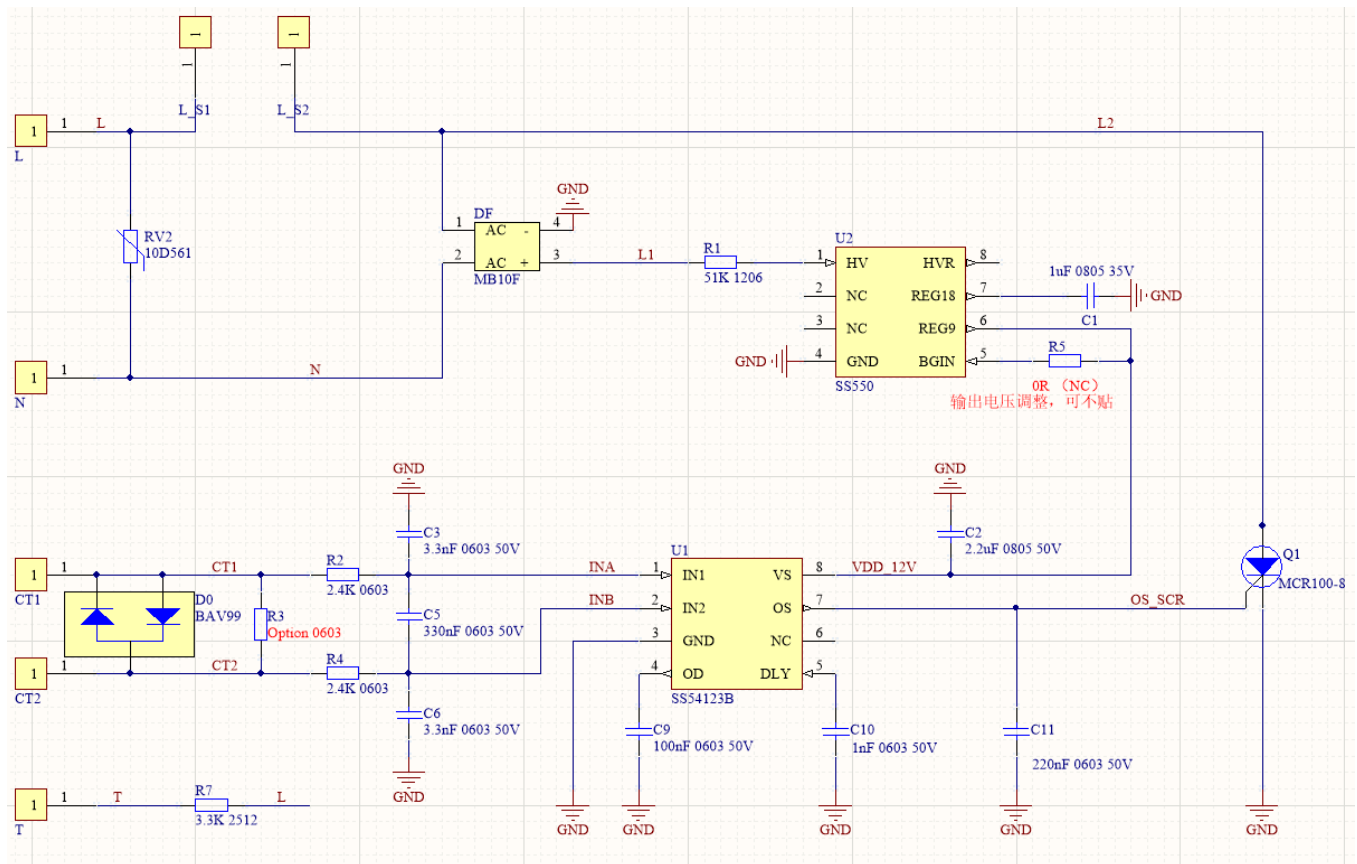
当  $V_{REF} = 1.5V$ ， $C_D = 1.83\mu F(1.5\mu F + 0.33\mu F)$ ， $I_D = 3\mu A$  时，

$T_D \approx 0.915s$

当  $V_{REF} = 1.5V$ ， $C_D = 0.8\mu F(0.47\mu F + 0.33\mu F)$ ， $I_D = 3\mu A$  时，

$T_D \approx 0.4$

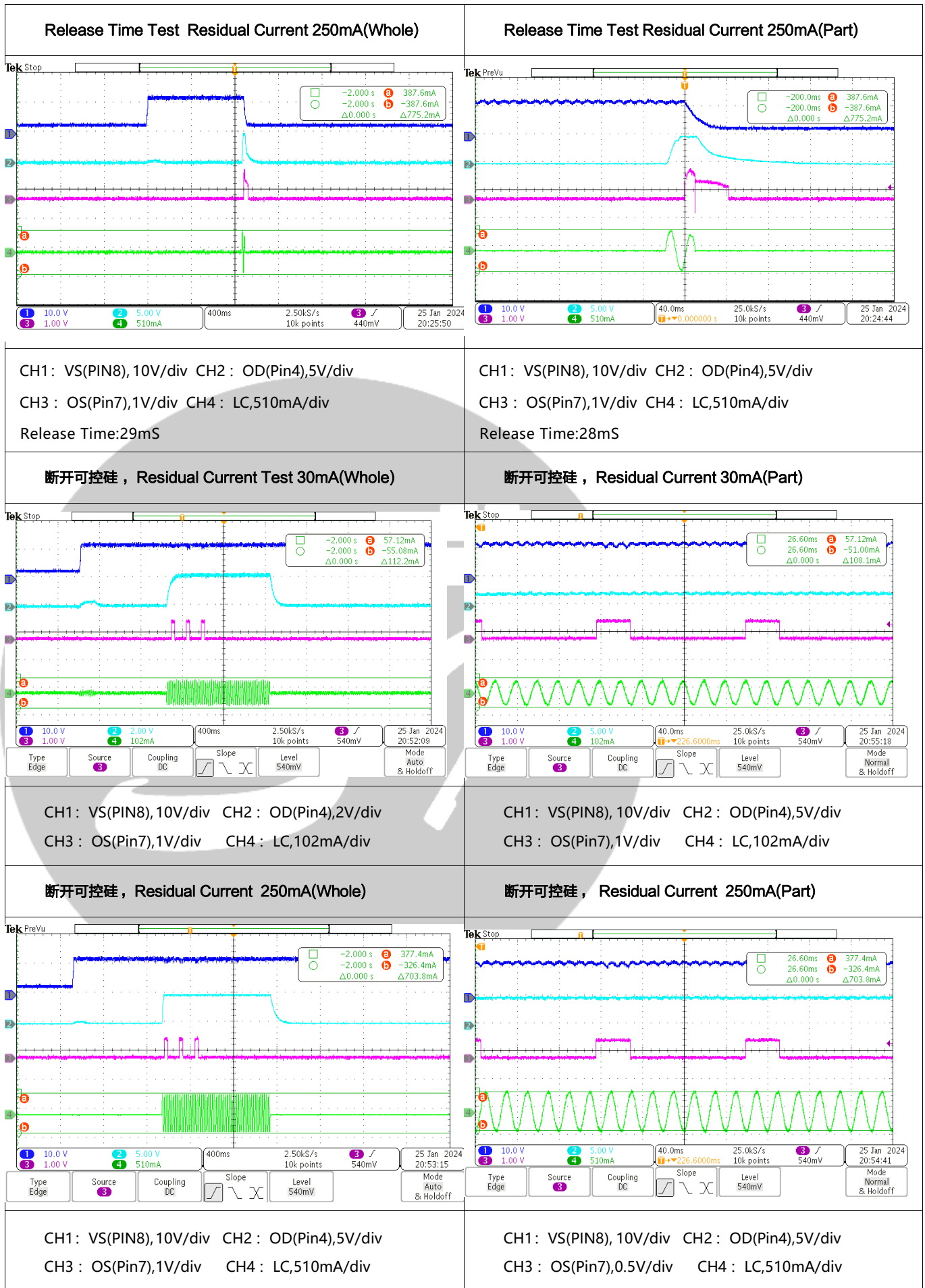
电路应用图：



# TYPICAL PERFORMANCE CHARACTERISTICS

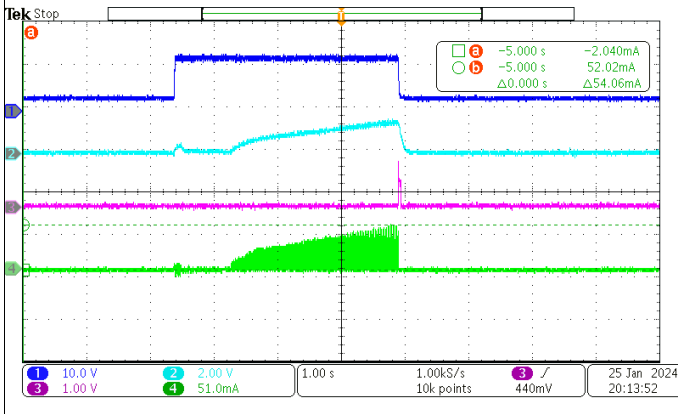
Unless otherwise specified, TA = 25°C

<p><b>Residual Current 15mA</b></p>	<p><b>Residual Current 15mA</b></p>
<p>CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div CH3: OS(Pin7), 1V/div CH4: LC, 20.4mA/div</p>	<p>CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div CH3: OS(Pin7), 1V/div CH4: CT2(Pin2), 2V/div</p>
<p><b>Residual Current Test 30mA(Whole)</b></p>	<p><b>Residual Current Test 30mA(Part)</b></p>
<p>CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div CH3: OS(Pin7), 1V/div CH4: LC, 51mA/div Leakage Current: 19.76mA Time = 1.4S</p>	<p>CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div CH3: OS(Pin7), 1V/div CH4: LC, 51mA/div Leakage Current: 19.76mA Time = 1.4S</p>
<p><b>Release Time Test Residual Current 30mA(Whole)</b></p>	<p><b>Release Time Test Residual Current 30mA(Part)</b></p>
<p>CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div CH3: OS(Pin7), 1V/div CH4: LC, 51mA/div Release Time: 59mS</p>	<p>CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div CH3: OS(Pin7), 1V/div CH4: LC, 51mA/div Release Time: 59mS</p>



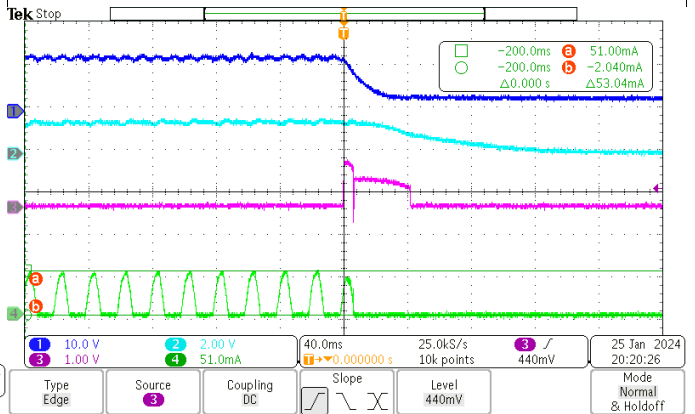


**A0, Residual Current Test 42mA(Whole)**



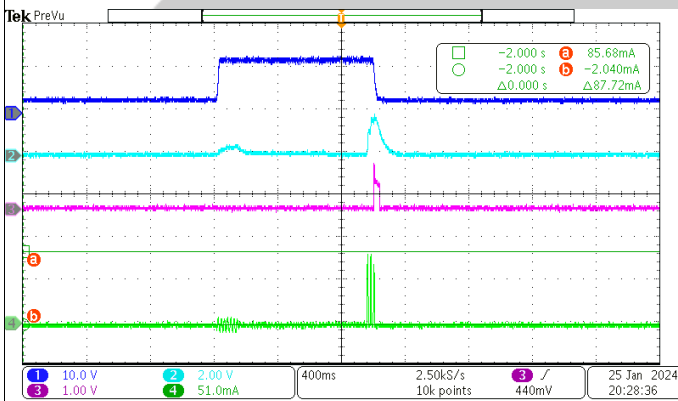
CH1: VS(PIN8),10V/div CH2: OD(Pin4),2V/div  
 CH3: OS(Pin7),1V/div CH4: LC,51mA/div  
 Leakage Current:25.73mA Time=2.63S

**A0, Residual Current Test 42mA(Part)**



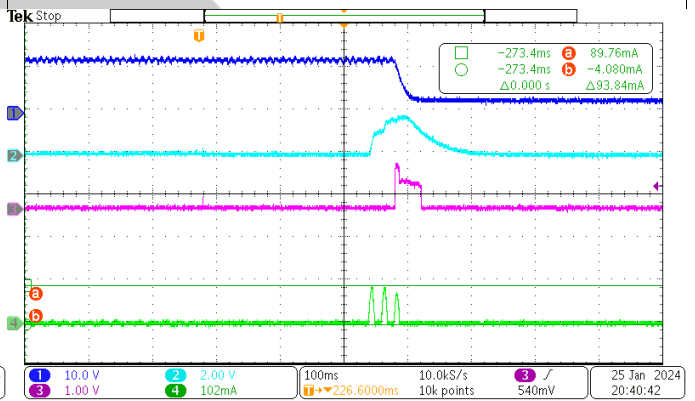
CH1: VS(PIN8),10V/div CH2: OD(Pin4),2V/div  
 CH3: OS(Pin7),1V/div CH4: LC,51mA/div  
 Leakage Current:25.73mA Time=2.63S

**A0, Release Time Test Residual Current 42mA(Whole)**



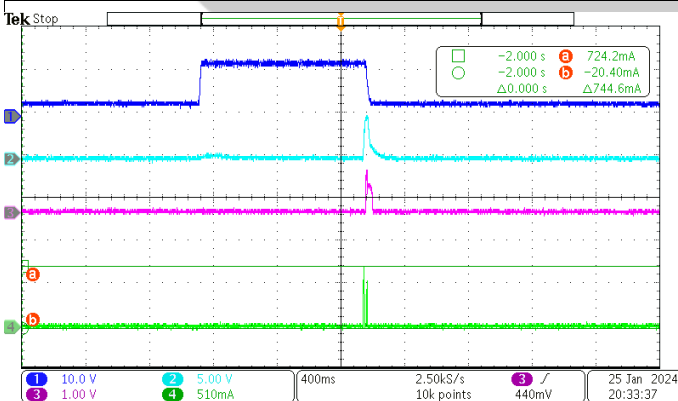
CH1: VS(PIN8),10V/div CH2: OD(Pin4),2V/div  
 CH3: OS(Pin7),1V/div CH4: LC,51mA/div  
 Release Time:48mS

**A0, Release Time Test Residual Current 42mA(Part)**



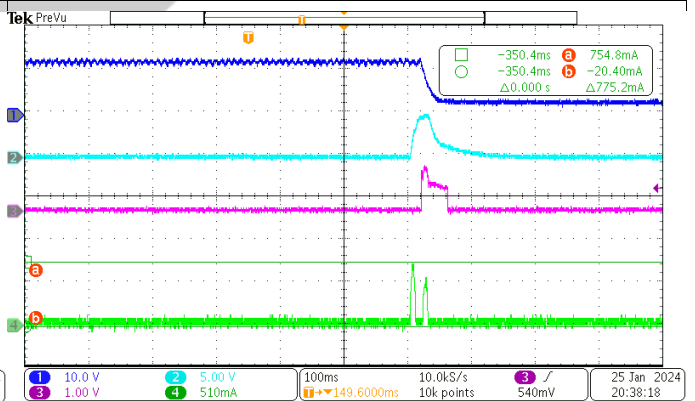
CH1: VS(PIN8),10V/div CH2: OD(Pin4),2V/div  
 CH3: OS(Pin7),1V/div CH4: LC,102mA/div  
 Release Time:49mS

**A0, Release Time Test Residual Current 350mA(Whole)**



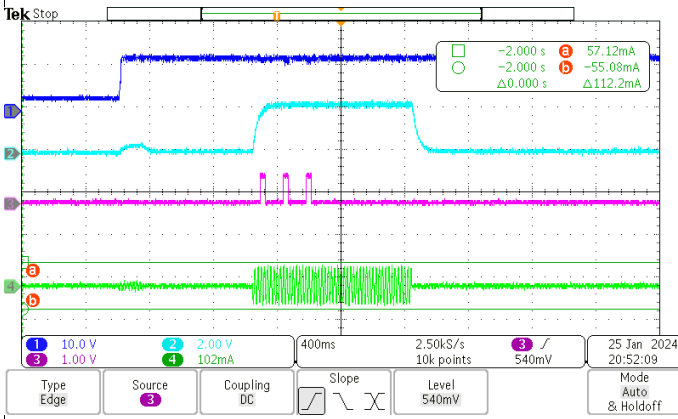
CH1: VS(PIN8),10V/div CH2: OD(Pin4),5V/div  
 CH3: OS(Pin7),1V/div CH4: LC,510mA/div  
 Release Time:28mS

**A0, Release Time Test Residual Current 350mA(Part)**



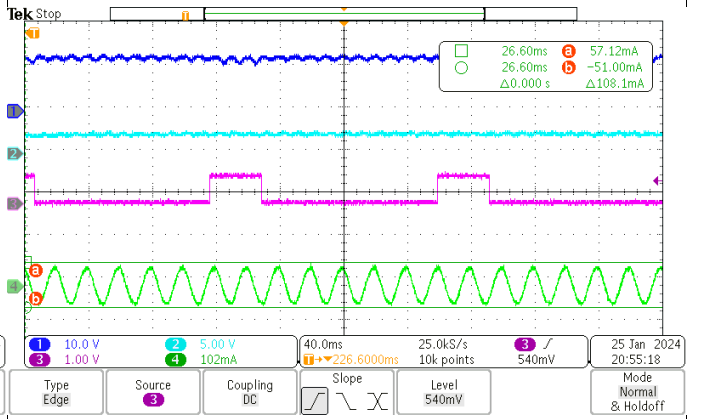
CH1: VS(PIN8),10V/div CH2: OD(Pin4),5V/div  
 CH3: OS(Pin7),1V/div CH4: LC,510mA/div  
 Release Time:28mS

A0, 断开可控硅, Residual Current Test 42mA(Whole)



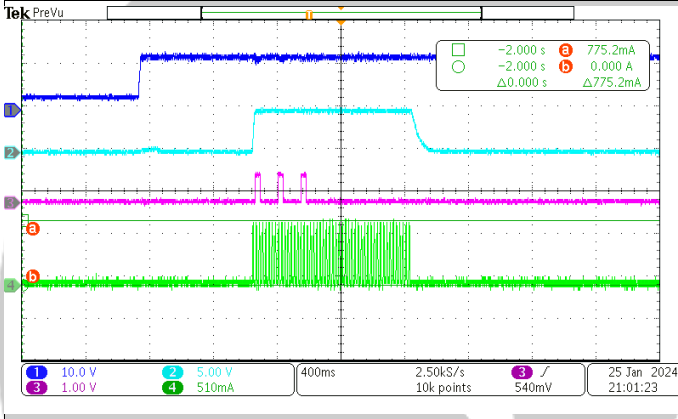
CH1: VS(PIN8),10V/div CH2: OD(Pin4),2V/div  
CH3: OS(Pin7),1V/div CH4: LC,102mA/div

A0, 断开可控硅, Residual Current 42mA(Part)



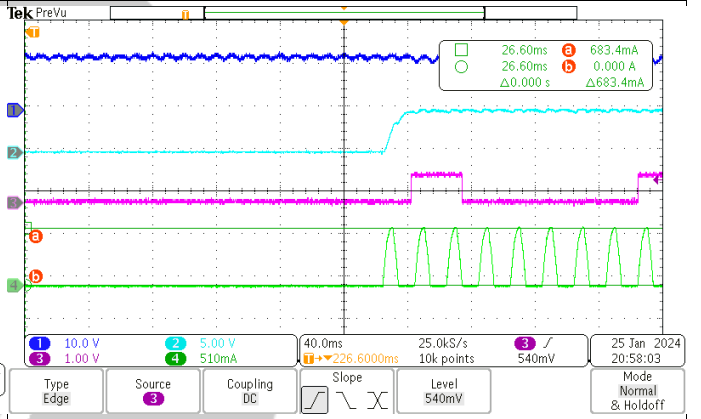
CH1: VS(PIN8), 10V/div CH2: OD(Pin4),2V/div  
CH3: OS(Pin7),0.5V/div CH4: LC,102mA/div

A0, 断开可控硅, Residual Current 350mA(Whole)



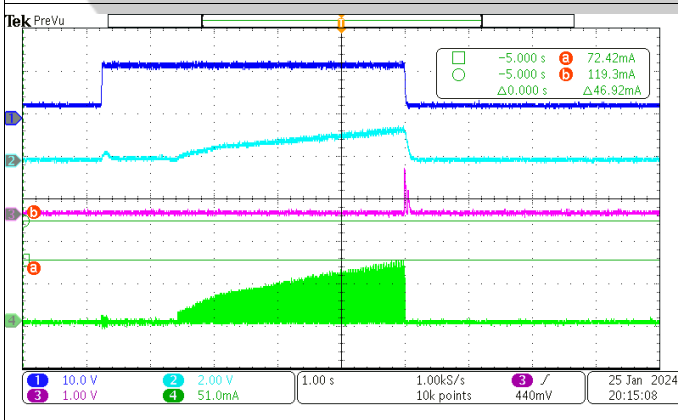
CH1: VS(PIN8),10V/div CH2: OD(Pin4),5V/div  
CH3: OS(Pin7),1V/div CH4: LC,510mA/div

A0, 断开可控硅, Residual Current 350mA(Whole)



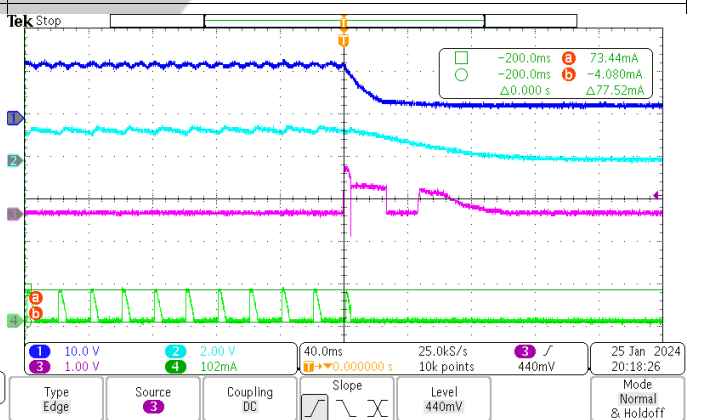
CH1: VS(PIN8), 10V/div CH2: OD(Pin4),5V/div  
CH3: OS(Pin7),1V/div CH4: LC,510mA/div

A90, Residual Current Test 42mA(Whole)



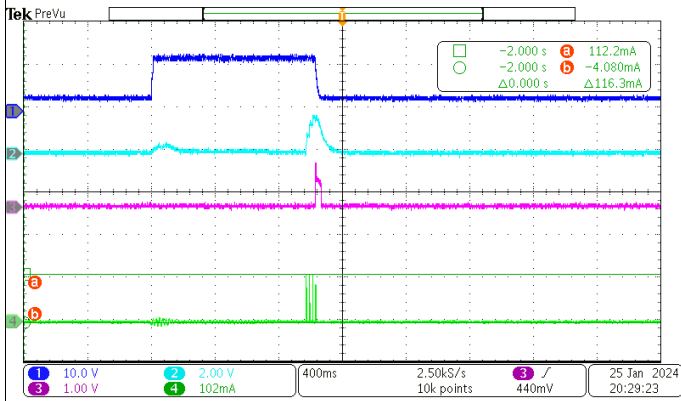
CH1: VS(PIN8),10V/div CH2: OD(Pin4),2V/div  
CH3: OS(Pin7),1V/div CH4: LC,51mA/div  
Leakage Current:26.92mA Time=3.62S

A90, Residual Current Test 42mA(Part)



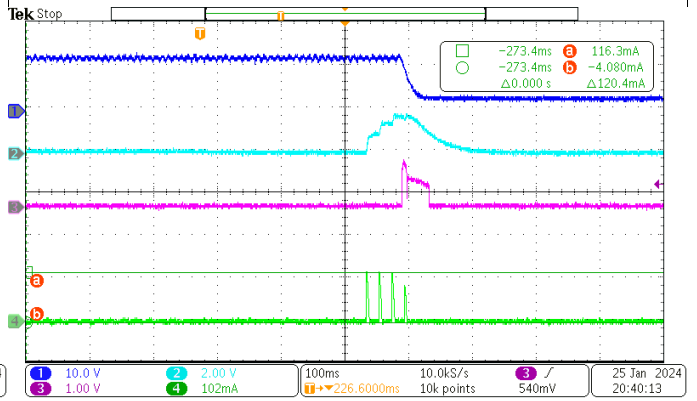
CH1: VS(PIN8), 10V/div CH2: OD(Pin4),2V/div  
CH3: OS(Pin7),1V/div CH4: LC,102mA/div  
Leakage Current:26.92mA Time=3.62S

A90, Release Time Test Residual Current 42mA(Whole)



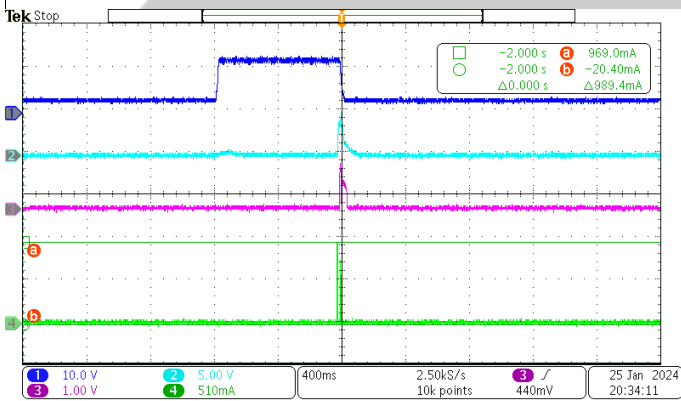
CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 102mA/div  
 Release Time: 64mS

A90, Release Time Test Residual Current 42mA(Part)



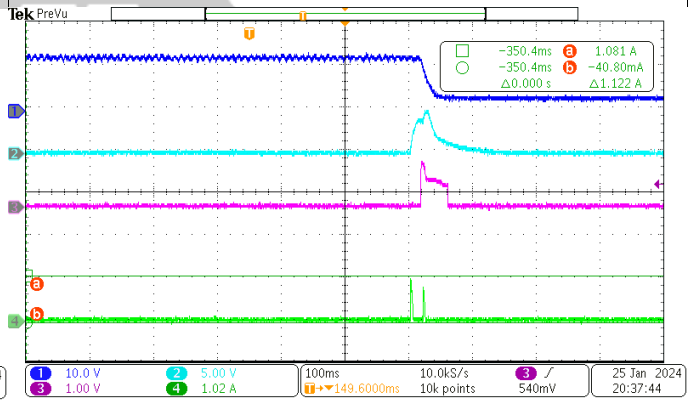
CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 102mA/div  
 Release Time: 64mS

A90, Release Time Test Residual Current 350mA(Whole)



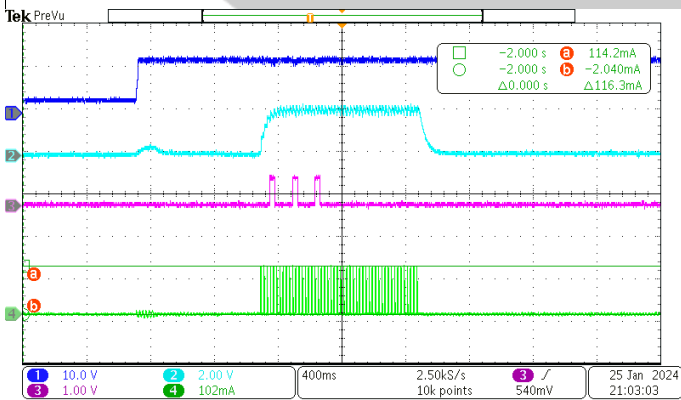
CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 200mA/div  
 Release Time: 25mS

A90, Release Time Test Residual Current 350mA(Part)



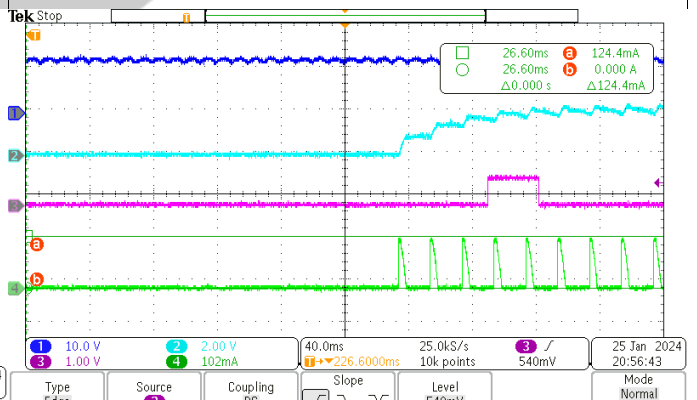
CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 5V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 1020mA/div  
 Release Time: 24mS

A90, 断开可控硅, Residual Current Test 42mA(Whole)



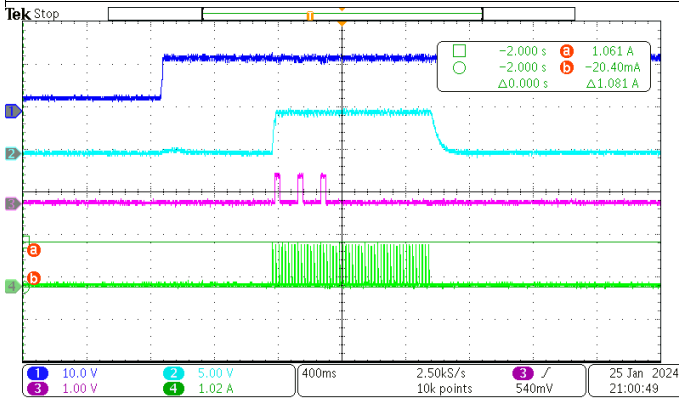
CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 102mA/div

A90, 断开可控硅, Residual Current 42mA(Part)

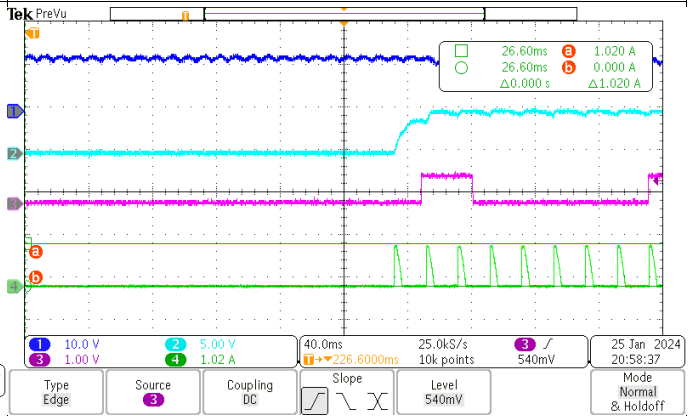


CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 102mA/div

A90, 断开可控硅, Residual Current 350mA(Whole)



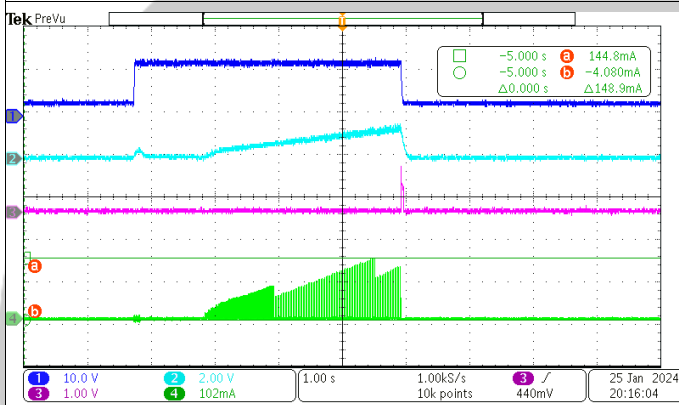
A90, 断开可控硅, Residual Current 350mA(Whole)



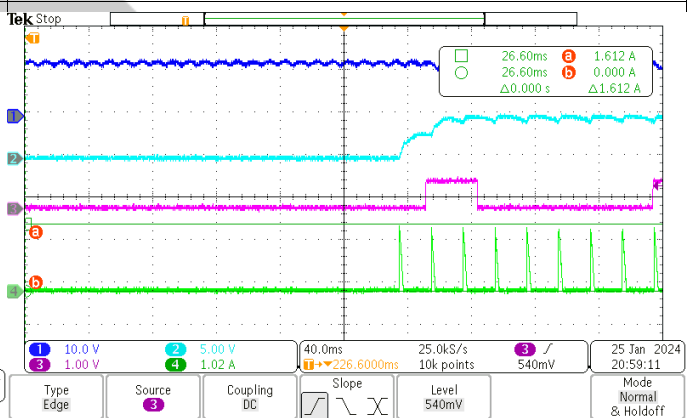
CH1: VS(PIN8),10V/div CH2: OD(Pin4),5V/div  
CH3: OS(Pin7),1V/div CH4: LC,1020mA/div

CH1: VS(PIN8),10V/div CH2: OD(Pin4),5V/div  
CH3: OS(Pin7),1V/div CH4: LC,1020mA/div

A135, Residual Current Test 42mA(Whole)



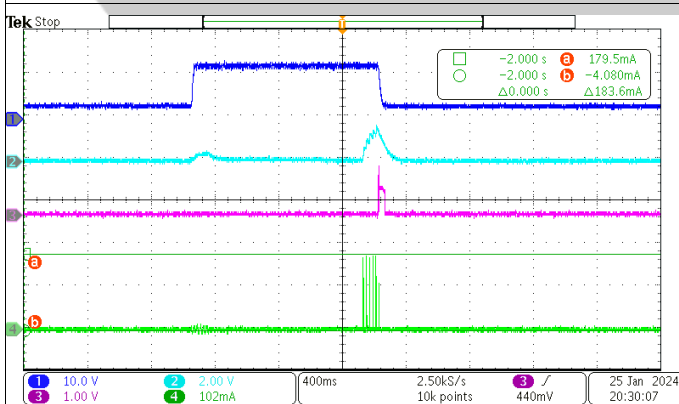
A135, Residual Current Test 42mA(Part)



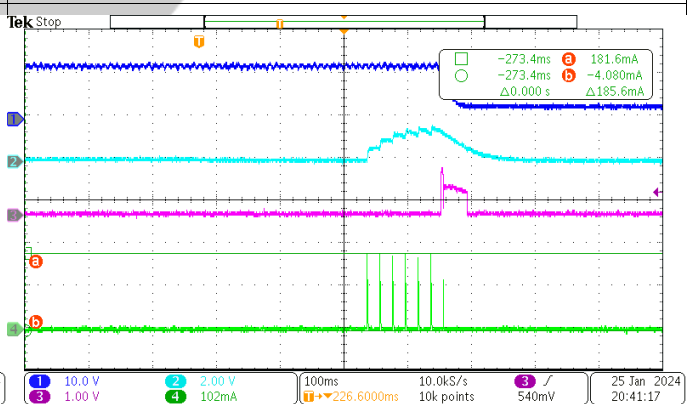
CH1: VS(PIN8),10V/div CH2: OD(Pin4),5V/div  
CH3: OS(Pin7),1V/div CH4: LC,102mA/div  
Leakage Current:34.9mA Time=3.12S

CH1: VS(PIN8),10V/div CH2: OD(Pin4),5V/div  
CH3: OS(Pin7),1V/div CH4: LC,1020mA/div  
Leakage Current:34.69mA Time=3.14S

A135, Release Time Test Residual Current 42mA(Whole)



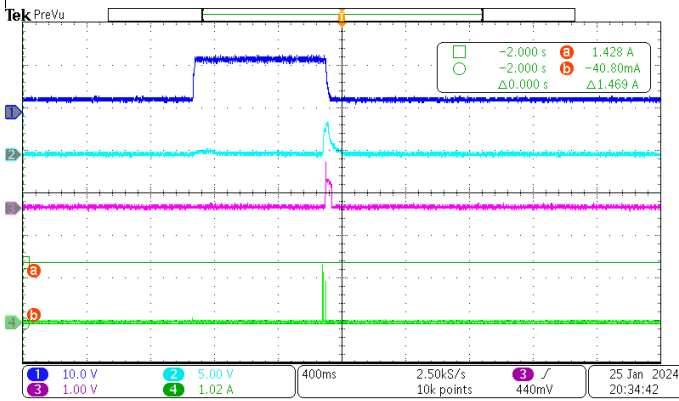
A135, Release Time Test Residual Current 42mA(Part)



CH1: VS(PIN8),10V/div CH2: OD(Pin4),2V/div  
CH3: OS(Pin7),1V/div CH4: LC,102mA/div  
Release Time:84mS

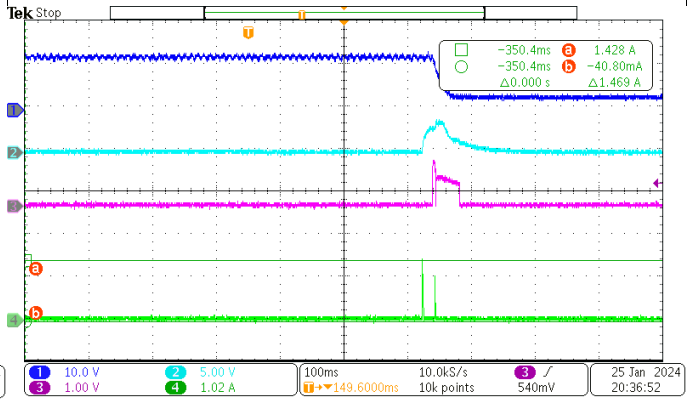
CH1: VS(PIN8),10V/div CH2: OD(Pin4),2V/div  
CH3: OS(Pin7),1V/div CH4: LC,102mA/div  
Release Time:86mS

A135, Release Time Test Residual Current 350mA(Whole)



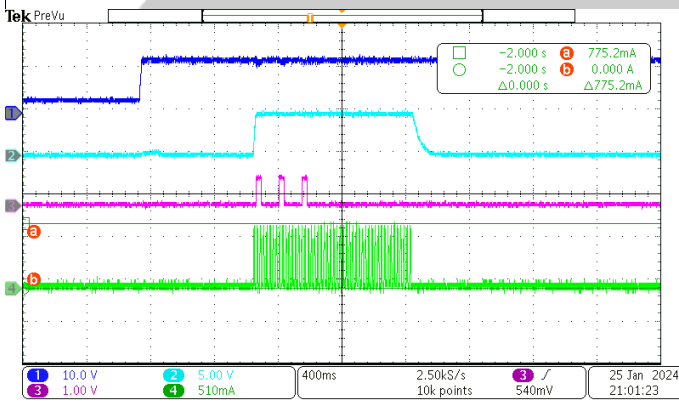
CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 5V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 1020mA/div  
 Release Time: 22ms

A135, Release Time Test Residual Current 350mA(Part)



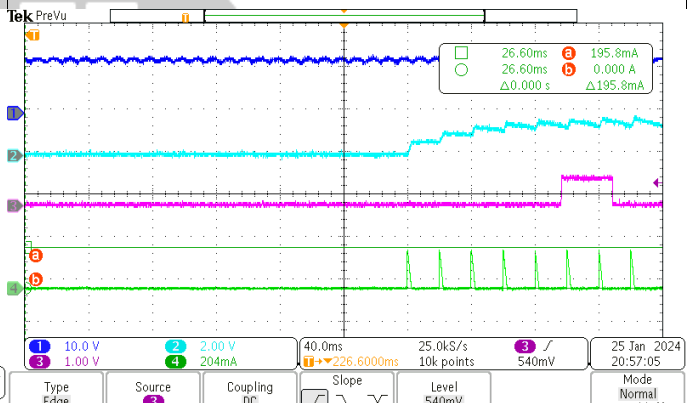
CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 5V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 1020mA/div  
 Release Time: 21ms

A135, 断开可控硅, Residual Current Test 42mA(Whole)



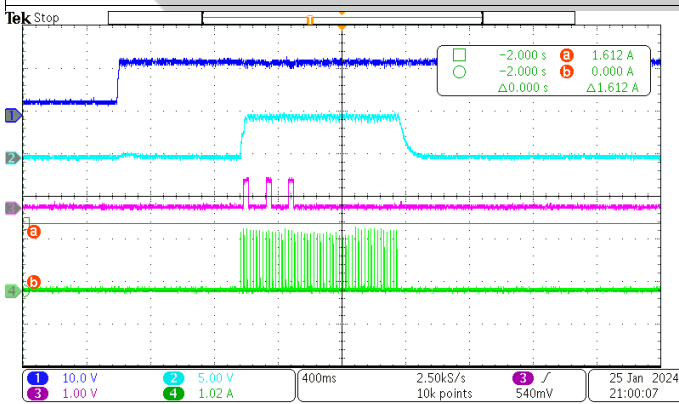
CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 5V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 510mA/div

A135, 断开可控硅, Residual Current 42mA(Part)



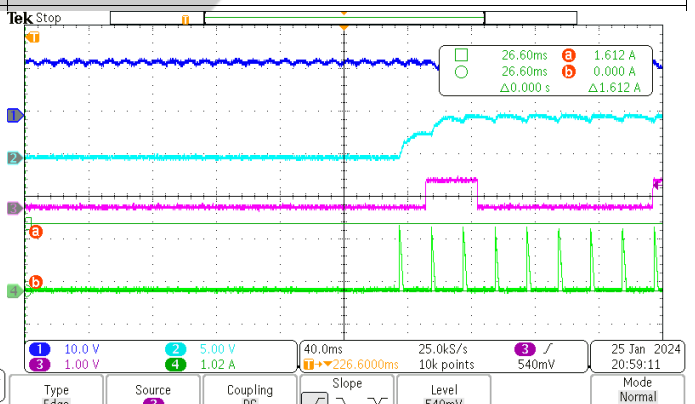
CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 2V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 204mA/div

A135, 断开可控硅, Residual Current 350mA(Whole)



CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 5V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 1020mA/div

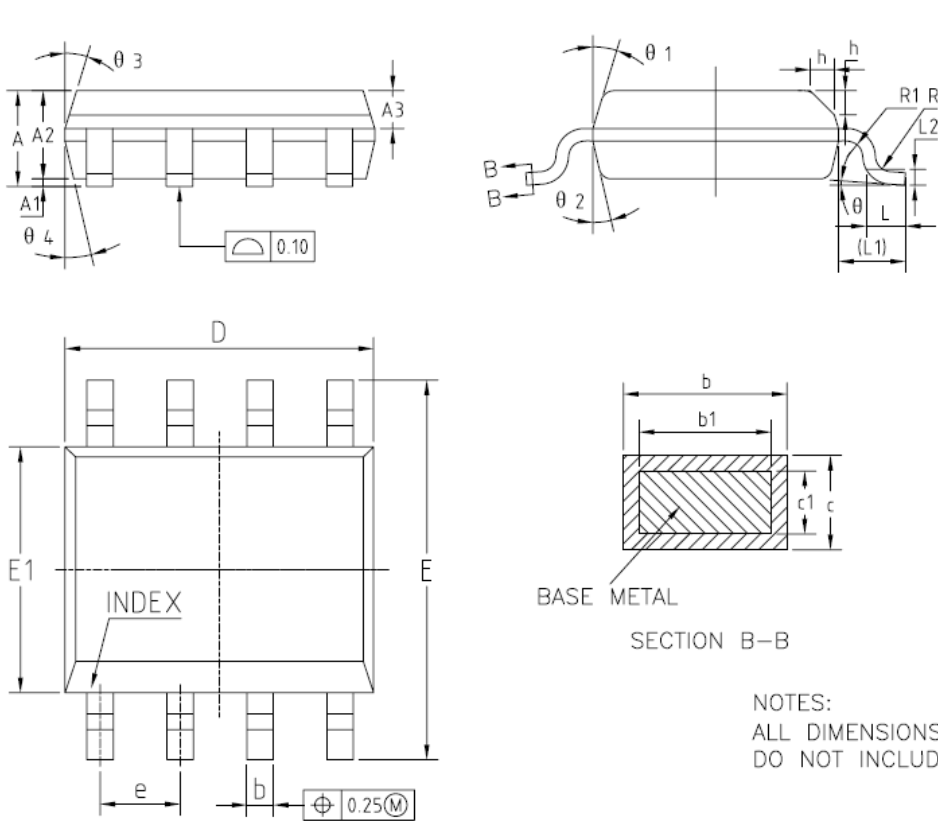
A135, 断开可控硅, Residual Current 350mA(Whole)



CH1: VS(PIN8), 10V/div CH2: OD(Pin4), 5V/div  
 CH3: OS(Pin7), 1V/div CH4: LC, 1020mA/div

Note 1: 断开可控硅测试是指断开供电与可控硅之间连接通路

# OUTLINE DIMENSIONS



COMMON DIMENSIONS  
(UNITS OF MEASURE=MILLIMETER)

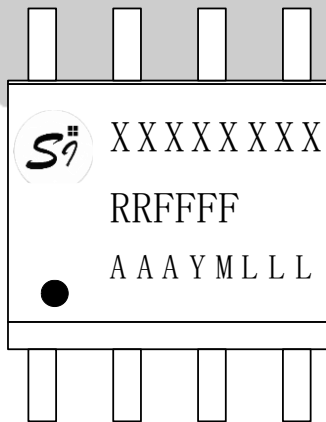
SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	—	0.51
b1	0.37	0.42	0.47
c	0.17	—	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	—	1.27BSC	—
L	0.45	0.60	0.80
L1	—	1.04REF	—
L2	—	0.25BSC	—
R	0.07	—	—
R1	0.07	—	—
h	0.30	0.40	0.50
theta	0°	—	8°
theta 1	15°	17°	19°
theta 2	11°	13°	15°
theta 3	15°	17°	19°
theta 4	11°	13°	15°

NOTES:  
ALL DIMENSIONS MEET JEDEC STANDARD MS-012 AA  
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 7. 8-Lead Small Outline Package [SOP]  
Dimensions show IN2 millimeters

# ORDERING GUIDE

型号	封装形式	温度范围	MK code	包装方式	卷盘尺寸
SS54123B	SOP8	-40°C to +125 °C	SS54123B G3PPDA AAAAYMLLL	3000/盘	13 寸卷盘



- 1、SI =Logo;
- 2、• =Pin1;
- 3、XXXXXXXX =Device name ;
- 4、RR =Product version;
- 5、FFFF =FuNction;
- 6、AAA =Company Encode;
- 7、YM =Year&Month;
- 8、LLL =Trace No.

注：本公司保留不预先通知而修改此文件的权利

## 版本信息

版本号	发布日期	页数	章节或图表	更改说明
1.0	2023.3	15		首次发布
1.1	2023.12	15		1、更新应用原理图与测试波形不一致说明见 Note1 2、更新测试波形； 3、更新丝印； 4、更新电气参数及温度曲线
1.2	2024.4	15		更新应用电路

